mfx3 plus

Service Manual

Software Version 14 & 15

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THE BENCHMARK IN DIGITAL AUDIO

Contents

1. Introduction

1.1 Important Notice

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1.2 Document Registration

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1.3 Important Information

1.3.1 EMC Standards

The Fairlight MFX 3plus Rack and MFX3plus Console conform to EMC Directive 89/336/EEC standard, Class A EN55022 EN50082.1.1995, and may affect domestic electronic equipment.

Installers should be aware of the requirements under the EMC Directive that complete installations must conform to the specification and not just the individual pieces of equipment.

For further information on correct EMC procedures please refer to the following titles:

Noise Reduction Techniques In Electronic Systems by Henry W .Ott

EMC by Tim Williams.

1.3.2 Fuse Ratings

To reduce the risk of fire, replace only with the same manufacture, type and rating of fuse as originally fitted. Only U.L. listed or recognised fuses are to be used.

Rack Fuse Rating: 125v @ 6.3 Amps

240v @ 3.15 Amps

Fuses are 5 x 20 Fast Blow

1.3.3 Mains Cables

All external cables are to be of U.L. listed or recognised type only.

1.3.4 Cleaning

Never use alcohol based cleaners or solvents when cleaning the MFX3plus Console or MFX3plus rack. A mild soap based solution is recommended. Always ensure that no water or cleaning agent is permitted to drip inside the Console or Rack enclosure. Similarly, do not spray cleaning agents directly onto the MFX Console or Rack.

It may be necessary after a priod of time to clean the air-flow path outside and inside the Rack enclosue. Failure to remove dust build up, especially arund the fans and EMC grills, may result in overheating.

2.0 Pre-Installation & Cabling Considerations

The following information is presented to ensure a smooth and timely installation and commissioning of the Fairlight MFX3^{plus} system.

2.1 Pre-Installation Checklist

- Is all relevant building work completed ie. timber, concrete, plaster, brickwork? Building work is a source of dust and moisture, both which can seriously affect system operation and reliability.

- Is the flooring complete, ie. carpeting, tiling, ducting? All work generating vibration, moisture or dust, must be completed before the installation can be considered. The warranty may be invalidated, and the system mean time before failure may be reduced, if this is not strictly adhered to.

- Have all mains cables and breakers been installed, in both the machine room and studio? It is recommended that the same power source be used for both the main-frame and the console. This can be achieved by installing a power run from the machine room mains to the studio (or wherever the console will be located), as the power source for the console.

- Have you received the pre-install connector kit? The installation manual contains all pinout information required to allow cable assembly.

- Is the studio and machine room wiring installation complete?

- Are all cables terminated and is all cable ducting accessible?

- Has the studio earthing been installed, are all earthing cables identifiable?

- Are all signal cables earthed at one end only? To avoid earth loops it is recommended that all signal cable shields be connected to ground at one end only.

- Has the air conditioning system been running for one to two days prior to installation? Air conditioning must be operating prior to installation in order to purge dust from the rooms and air conditioning ducts.

- Has the loading placed on the air conditioning by the system installation been considered? A clean, dust free and low humidity environment with an ambient temperature of 19° C or lower is recommended.

- Will all external system interfacing have been completed? All Multitrack sends and returns, audio and video tie lines, sync sources and video distribution cabling should be completed.

- Are all audio and video tape machines installed and tested?

- Are all video monitors installed and tested?

Notes:

1. Please do not attempt to power up any part of the MFX 3plus system without prior approval. Powering up and testing are an integral part of the commissioning exercise, and are critical in ensuring a smooth problem free installation.

2. Always observe Anti Static precautions when handling electronic assemblies.

2.2 Cabling Considerations

Poor cabling can be the bane of a good system. Earth loops, floating inputs and outputs and extended runs are just some of the issues to be addressed when planning an installation.

2.2.1 MFX Control Cable

The MFX Control Cable connects the MFX Console to the Mainframe unit. The cable carries RS232, RS422 and MIDI signals and is limited to a maximum length of 20 metres. The Mainframe is supplied with a 10 metre cable. Ensure sufficient slack is left at the Console end to ensure movement of the Console does not cause undue stress on the connector, or cause the connector to partially disconnect, which can damage the serial drivers. When fitting or reconnecting the cable ensure that power is off at either the Mainframe or the Console.

2.2.2 Sony 9-Pin Cable

The 9-Pin cable connects the Mainframe to a Sony 9-pin protocol machine. It is an RS232 cable with three main connections, being Tx, Rx and ground. The recommended maximum length for this cable is 30 metres. The Mainframe is supplied with a 5 metre cable. Again it is recommended that power be switched off at one end when connecting to protect the drivers.

2.2.3 Video Cable

The Video cable connects the VGA output from the Mainframe to the attached Monitor. It is basically a 15-way shielded 50 Ohm cable with high density D-type connectors at each end. A maximum length of 20 metres is typical. The Fairlight Mainframe is supplied with a 10 metre cable which has been found to be suitable for the majority of monitors. An optional modified SVGA buffer unit may be used to extend the cable lenght if necessary.

2.2.4 SCSI Cable

The SCSI cable connects the Mainframe to external SCSI devices. It is a 50-way shielded cable with moulded connectors at each end and a metal shield in each connector. Each Cable should be no longer than 1 metre in length. The total length of all external SCSI cables connected to a Mainframe should be less than 4 meters. Avoid using cables with connectors of all plastic manufacture as these do not typically seat on all SCSI devices and have been found to be unreliable. Avoid inexpensive 'budget' SCSI cables to ensure reliability of operation.

2.2.5 SCSI Terminator

Use an Active SCSI Terminator to terminate the last device in the SCSI chain.

2.2.5 LTC Cable

Cables used in connecting LTC to and from the MFX system should preferably be wired as pin 2 hot, pin 1 gnd and pin 3 cold. Where an unbalanced source is used, it is required that pin 3 be shorted to ground to prevent noise entering the system.

2.2.6 Audio Cable

Standard shielded audio cable is suitable. Pin 2 is hot, pin 1 gnd and pin 3 cold. Unbalanced sources should have pin 3 shorted to pin 1.

2.2.7 Digital Cable

Digital cables connected to the MFX system must be of the correct 110 Ohm impedance. Alternatively, the AES signals can be routed through a video distribution amplifier for long runs and multiple distributions. As a limited amount of research has been performed on this form of distribution some experimentation may be required.

3.0 Space and Cooling

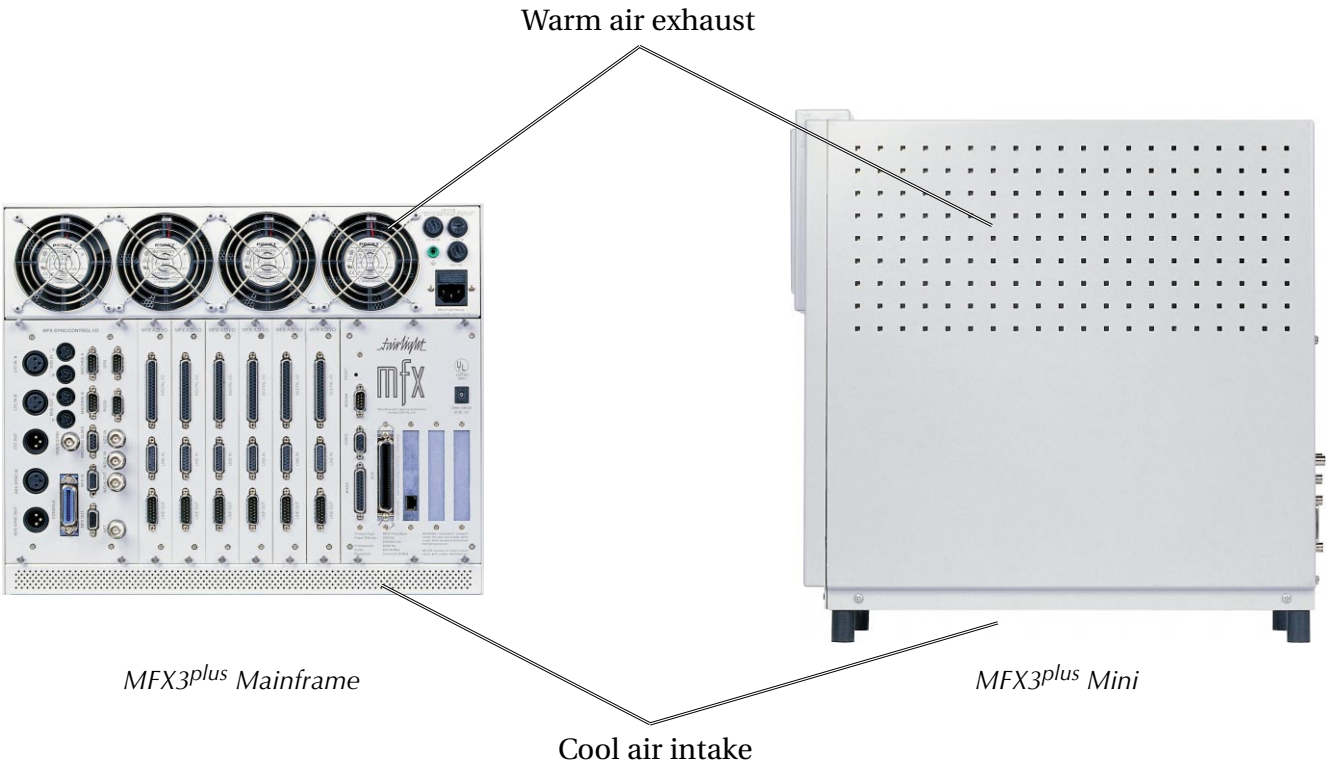
It is recommended that the Mainframe be installed in an air conditioned machine room. The Mainframe system is designed to fit a standard 19 inch rack enclosure whereas the Mini is designed for free standing installation in a machine room or studio. For access requirements it is adviseable that at least 2U of space is left above and below the Mainframe to facilitate the easy placement of cards or external hard disk drives when updating software or firmware. This will also offer improved air flow for cooling. Clearance must also be provided at the rear of the Mainframe so as not to restrict the flow of cooling air – at least 120mm space is the recommended minimum. For service purposes it is recommended that easy access to the rear of the Mainframe is provided at all times.

The Mainframe is 36.5cm (8U) high, 47 cm deep and weighs approximately 45kg. When being installed, it is recommended three persons perform the installation.

The power source for the Mainframe should be filtered. When large variations occur to the mains supply voltage an uninteruptable power supply (UPS) is mandatory. Line voltage is typically not a major issue however variations do become critical at lower operating line voltages. If system crashes and lock-ups are occurring it is recommended a mains line monitor is connected to the mains supply to evaluate the quality of power available.

Avoid installing the Mainframe:
- where air flow is poor or restricted
- in dusty or damp areas or close to heat sources
- in unstable enclosures or areas subject to vibration
- in close proximity to strong magnetic or electrical fields
- in areas with poor service access
- to an unfiltered mains supply

Being a compact unit, cooling in the Mini is very important. Cooling is provided by five 60mm fans mounted horizontally with a sixth 60mm fan dedicated to the NFS350 switch mode power supply. It is vitally important that the power supply fan is always be checked for correct operation when a new system is installed and regularly as part of routine maintenance.



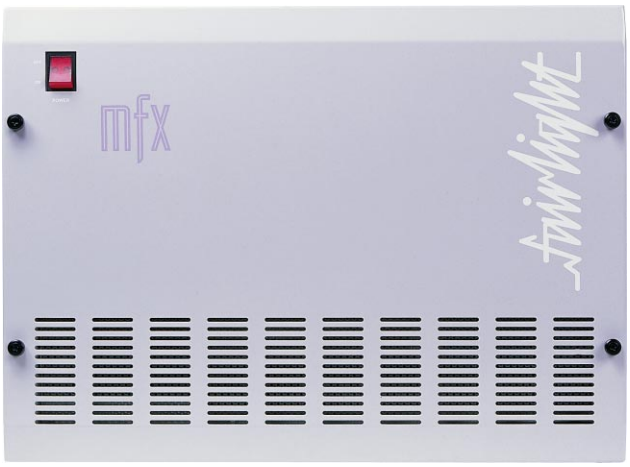
4.0 The MFX3plus Mainframe and Mini

4.1 The Mainframe

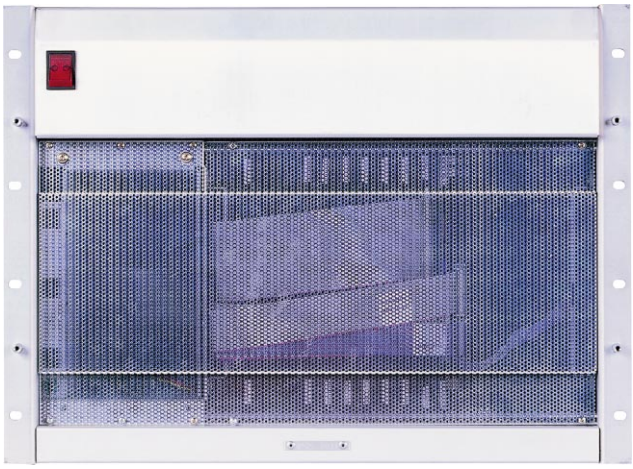
The Fairlight MFX3plus 19 inch Mainframe configuration offers a maximum of 24 input/ output tracks in both the digital and analogue domain, with all storage provided by SCSI hard drives. Systems can be configured from 4 input/4 output through to 24 input/24 output by the installation of the appropriate hardware and software. The 19 inch Mainframe supports one internal 3.5 inch hard drive in the rear SCSI section (typically the boot drive) and optionally, up to three 3.5 inch devices in the front drive mount section. Drives mounted in the front section should be spaced apart for cooling purposes. Due to cooling requirements for drives it is recommended that where possible drives be mounted in external boxes rather than in the Mainframe itself.

Gaining access to the digital cards is achieved by removing the four screws at the top & bottom of the front dress panel. Removing the dress panel will provide access to the RF screen panel which can be removed by further mounting screws. Once the RF screen is removed, access is gained to the digital cards. Depending on system configuration there will either be one to six ESPDCC (Digital Channel Card) cards fitted in the digital section. All digital cards are fitted with extraction handles, at the top and bottom of the front of the cards. These handles typically carry the card part number and revision on the top handle and the serial number on the bottom handle. For correct revision information please refer to the ECN manual available from the Technical Support Department.

When a Mainframe has been transported it is possible that the digital cards have become loose in their slots. For this reason it is advisable that the digital cards are re-seated firmly into position prior to powering up the system. All cables should similarly be checked to ensure they are firmly seated into their respective connectors.



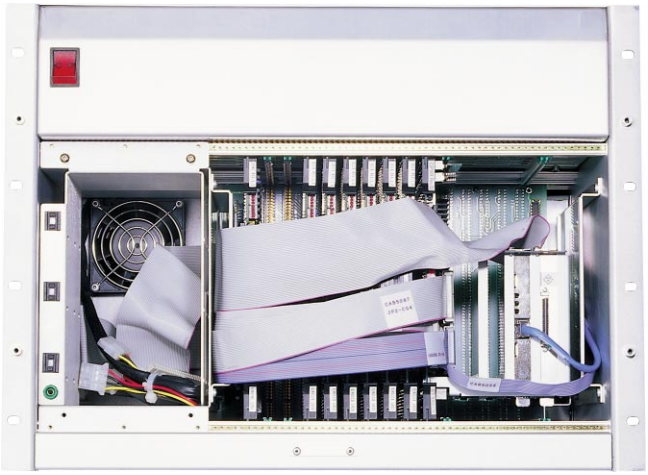
MFX3plus Mainframe Front View



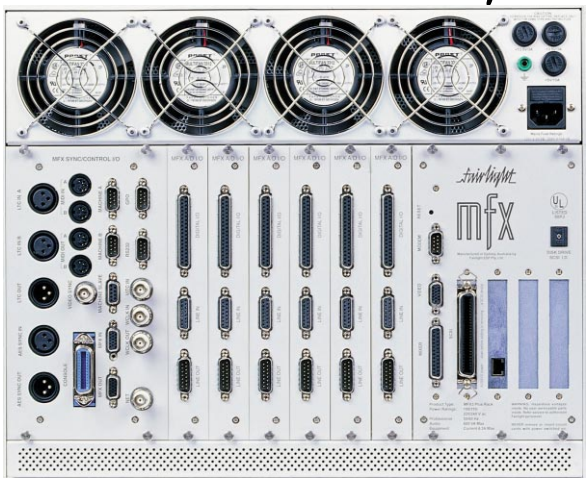
Front View with Dress Panel Removed

To the left of the digital card cage there is a SCSI device mounting area. The SCSI and Power cables are installed during manufacture and three SCSI ID switches are provided on the drive mounting plate.

The boot SCSI drive is typically fitted in the rear SCSI panel. Space is provided for one 3.5 inch drive, equipped with all cables and SCSI ID switch. The video buffer board is also fitted to this panel, which converts the digital VGA signal to the analog format required by most VGA monitors. Access to this panel is achieved by removing the six retaining screws.



Front View with RF Screen Removed



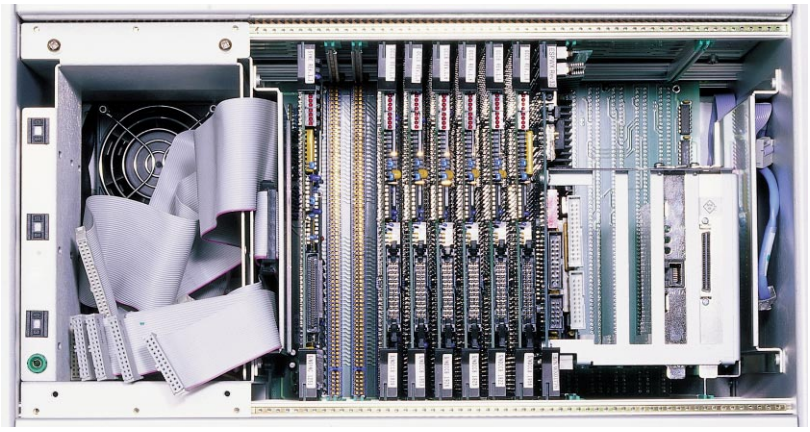
Mainframe Rear View

Located to the left of the rear SCSI panel are six slots for ESPDIO/AIO cards. Depending on the configuration of the MFX3^{plus} system ordered, blanking plates are fitted if fewer than six ESPDIO/AIO cards are present. When fitted, the ESPDIO/AIO cards are securely held in place by thumb screws and as such do not require reseating after transport.

Located to the left of the ESPDIO/AIO cards is the SYNC I/O module, which occupies the width of four ESPDIO/AIO cards and is held in position by four thumb screws. In addition to the edge connectors on the SYNC I/O module, two flying lead cable assemblies are connected directly to the module. A 10-way cable carries RS232 serial data from the QWERTY side of the Console, while a dual 30-way cable provides all the bidirectional syncronization information. Care should be excercised when removing the SYNC I/O module, ensuring the two flying lead cables are disconnected before attempting to fully withdraw the SYNC I/O module from the Mainframe. Similarly, when refitting the SYNC I/O module care should be taken to prevent damage to the cables.

Power in the Mainframe system is derived from an internal switch mode power supply. The power supply is a Computer Products™ NFS350, which supplies power for all the electronics and the rear SCSI internal boot drive. Power for the front mounted internal SCSI drives is provided by an optional Computer Power NFS110 supply. Both supplies carry a UL and CSA approval and feature automatic shutdown circuitry in the event of a short circuit or overload condition. The mains fuses for these units are fitted to the rear of the Rack with the appropriate labeling for supplies. Both supplies are auto switching at the input and as such only the mains fuse requires changing when switching between 110V and 240V ranges.

Cooling in the rack is provided for by four 80mm fans which should be checked at regular intervals for correct operation. An anti-static connector is provided at the rear panel. When servicing the Mainframe the technician should always be grounded via this connector to avoid static discharge damage.



Detail of Mainframe showing SCSI Drive Bay and Digital Card Cage

Slot Number	Part Number	Description
1	ESPSYN	Sync Card
2	ESPMX1	Digital Mixing Card - FAME
3	ESPMX1	Digital Mixing Card - FAME
4	ESPDCC	Digital Channel Card
5	ESPDCC	Digital Channel Card
6	ESPDCC	Digital Channel Card
7	ESPDCC	Digital Channel Card
8	ESPDCC	Digital Channel Card
9	ESPDCC	Digital Channel Card
10	ESPTSR	Turbo SCSI Card
11	ESPWX	Wave Executive Card/Color Graphics Card

MFX3plus 19 inch Mainframe Digital Card Cage Slot Assignment

4.2 The Mini

The Fairlight MFX3plus Mini configuration offers a maximum of 8 input/output tracks in both the digital and analogue domains operating from either a SCSI Magneto-Optical (MO) or hard drive. Systems can be configured as 4input/4 output or 8 input/8 output, or alternatively 4 input/8 output, depending on the hardware and software installed. It has internal device mounting capabilities for one 3.5" hard drive and a 5.25" devices such as an Optical drive or an Exabyte drive.

Gaining access to the digital cards is achieved by removing the two screws at the bottom of the front panel and then lifting this panel out and upwards such that it slips out of the two top mounting slots. If there is not an Optical or Exabyte drive fitted then there will typically be two 3.5" blanking panels to the right of the power supply. If an Optical or Exabyte drive is fitted extreme care should be taken when removing the front panel such that damage to the drive front panel is avoided. Depending on system configuration there will either be one or two ESPDCC (Digital Channel Card) cards fitted in the digital section. All digital cards are fitted with extraction handles at the top and bottom of the front of the cards. These handles typically carry the card part number and revision on the top handle and the serial number on the bottom handle. Labelled from left to right, the cards should carry the following part numbers.

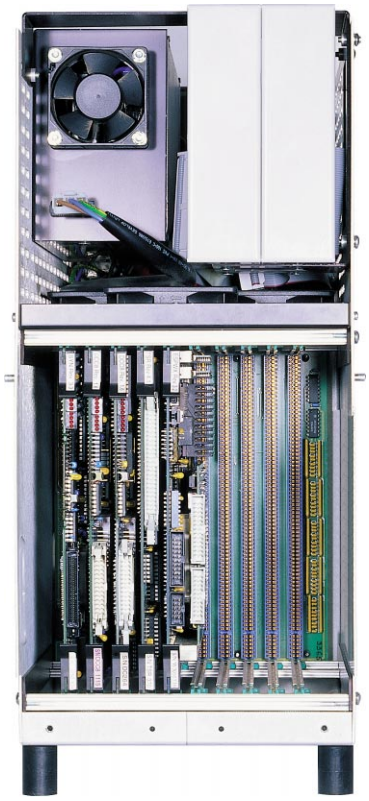
Slot Number	Part Number	Description
1	ESPSYN	Sync Card
2	ESPDCC	Digital channel Card
3	ESPDCC	Digital Channel Card
4	ESPTSR	Turbo SCSI card
5	ESPWX/CG4	Wave Executive / Color Graphics Card

MFX3plus Mini Digital Card Cage Slot Assignment

For correct revision information please refer to the ECN manual available from the Technical Support Department.

When an MFX3plus Mini has been transported it is possible that the digital cards have become loose in their slots. Thus it is advisable that these cards be seated firmly into position prior to powering up the system. Cables should also be checked to ensure they are firmly seated into their respective connectors.

The MFX3plus Mini weighs approximately 15 Kg and measures 21.3 cm wide, 47 cm deep and 46 cm high.



Mini Front View with Cover Removed

Mini Rear View

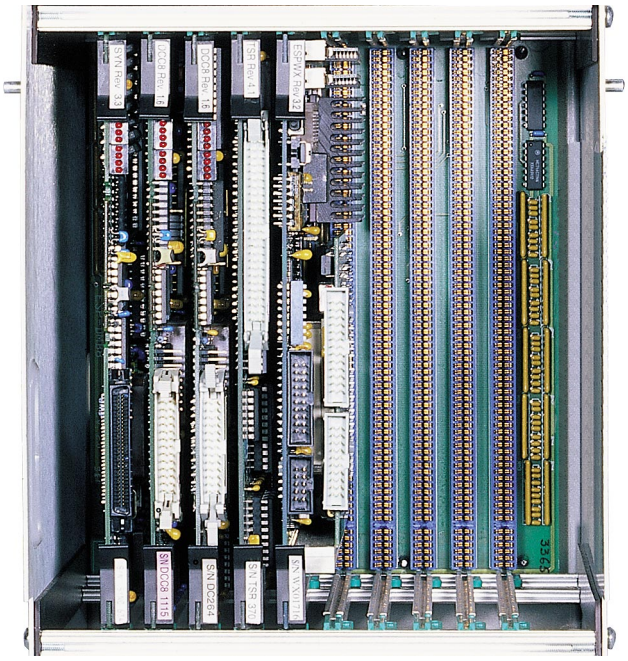
The outer case of the Mini can be removed by first removing the two screws located at the bottom of each side of the case. Once the cover is removed access is gained to the power supply, digital card cage and internal drives. Internal mounting space is provided for one 3.5 inch hard disk (typically the boot drive) toward the rear of the cabinet and opposite the power supply, and one 5.25 inch or 3.5 inch devics at the upper front of the cabinet adjacent the power supply. All necessary cables for SCSI data, ID and power are pre-installed during manufacture. Please note that while it is possible to fit two 3.5 inch devices in the front section, only one SCSI ID connection is provided. A video translator card is fitted to the rear panel of the unit which converts digital VGA data to the analog format currently employed by most VGA monitors.

Mini Top View with Cover Removed

The rear of the Mini cabinet contains the Input/Output Sync Module and the ESPDIO/AIO digital/analog input/output cards. From right to left the cards should be as follows:

Slot 1	ESPDIO/AIO
Slot 2	ESPDIO/AIO (optional, 8-track)
Slot 3	ESPSYNC I/O

The SYNC module occupies the width of four ESPDIO/AIO cards and is held in position by four thumb screws. In addition to the edge connectors on the SYNC module, two flying lead cable assemblies are connected directly to the module. A 10-way cable carries RS232 serial data from the QWERTY side of the Console while a dual 30-way cable provide all the bidirectional syncronization information. Care should be excercised when removing the SYNC module, ensuring the two flying lead cables are disconnected before attempting to fully withdraw the SYNC module from the Mainframe. Similarly, when refitting the SYNC module care should be taken to prevent damage to the cables.



Mini Front View - Detail of the Digital Card Cage

Power in the Mini system is derived from a Computer Products NFS350 switch mode power supply. The supply carries a UL and CSA approval and features automatic shutdown circuitry in the event of a short circuit or overload condition. The supply is auto switching at the input and as such only the mains fuse requires changing when switching between 110V and 240V ranges.

Slot Number	Part Number	Description
1	ESPSYN	Sync Card
2	ESPDCC	Digital channel Card
3	ESPDCC	Digital Channel Card
4	ESPTSR	Turbo SCSI card
5	ESPWX/CG4	Wave Executive / Color Graphics Card

MFX3plus Mini Digital Card Cage Slot Assignment

5.0 Power Supply

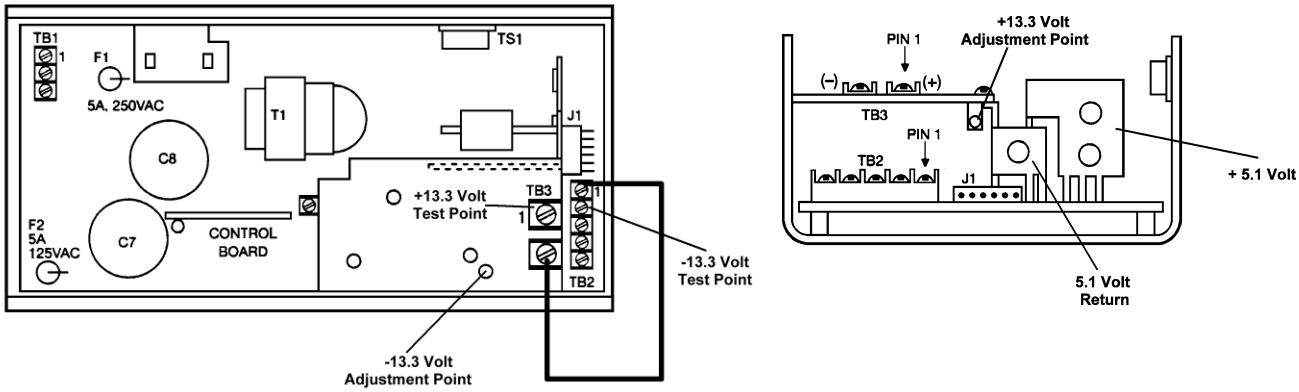
The power supplies employed in the MFX3^{plus} product range are Computer Products™ units. Both the Mainframe and Mini utilise NFS350 350 Watt switch mode supplies. The Mainframe will also accept an optional Computer Products NFS110 110 Watt power supply, required if internal SCSI drives additional to the boot drive are to be fitted. The power supplies in the Mainframe are mounted directly above the card cages. Access can be achieved by removing the top panel. In the Mini the power supply is mounted in the top enclosed area and assess can only be achieved by removing the top frame and front panel assemblies.

5.1 The NFS350-7625

The NFS350-7625 power supply is a quad output, 350 watt open frame switch mode supply. The input circuitry is universal, Thus there is no need for switch settings or jumpers through out the world. There are three fixed outputs, the first being 5V @ 50A, the second 12V @ 12A and the third being -12V @ 5A. The fourth output is adjustable in the range of 4.5V to 16.5V @ 4A. The power supply incorporates thermal protection, overvoltage protection and short circuit protection with auto-restart. This power supply is approved by UL, CSA, VDE, and its built-in line filter reduces conducted noise below FCC and VDE limit A. Cooling for this power supply is provided by means of fans. It is important that the fans at the rear of the Mainframe are checked regularly and with the Mini there is a fan mounted directly on the power supply which should also be checked regularly. Fans used are typically Papst™, and as such are very reliable. All power supplies are set-up and adjusted at the factory and there is no need for adjustment in the field. Faulty units should be returned to the head office for repair/exchange.

<u>There are no user serviceable parts in the above described power supply.</u>

5.2 Power Supply Adjustment Procedure



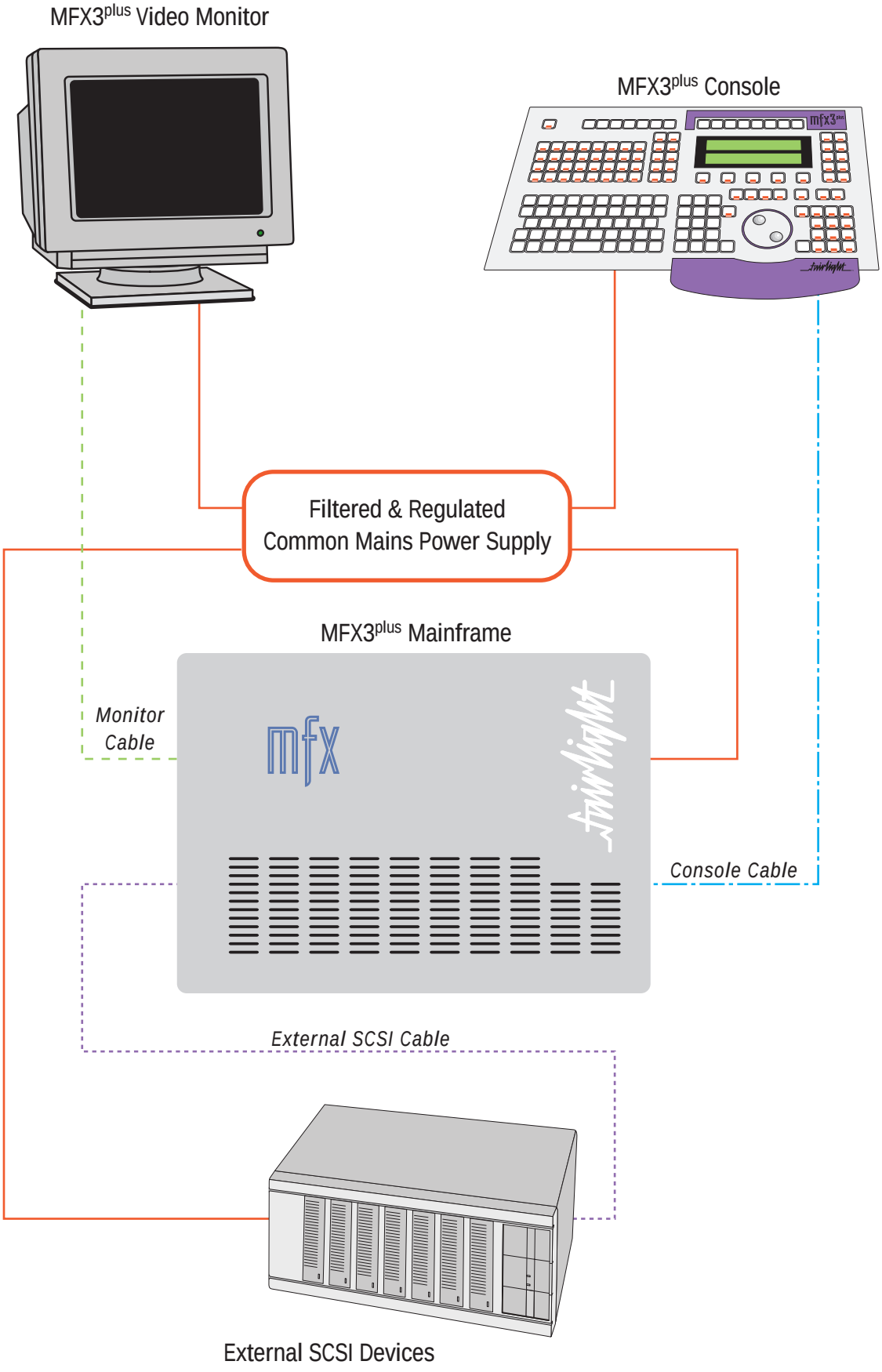
1. Connect ground link between TB3 Pin 2 and TB2 Pin 1 if not already done

2. Adjust the –13.3 Volt adjustment pot fully counter clockwise and note voltage between TB2 pins 1 & 2 (should be about –13.3 Volt)

3. Adjust the +13.3 Volt adjustment pot for the same figure as in step 2 except +ve with respect to ground (about 13.3 Volt) between TB3 pins 1 & 2
   Note: start by turning pot fully anti-clockwise and then 5-6 turns clockwise

6.0 Installation

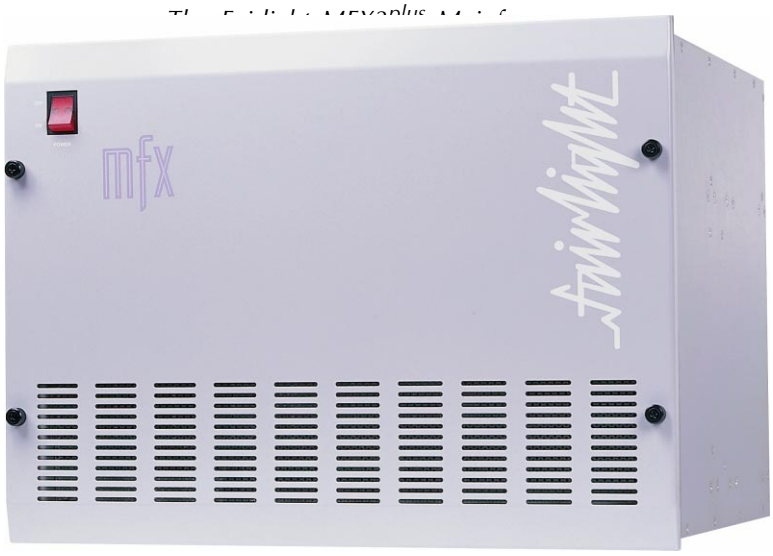
6.1 Installation Power Diagram



6.2 MAINFRAME

The Mainframe takes up 8 RU when fitted into a 19 inch rack. It operates from either 100-120v or 200-250v, 50-60Hz with the mains input being auto-switching. At least two persons are required to fit the Mainframe into a 19" rack as the unit is quite heavy. It is however recommended that a third person be made available for the initial fitment into the rack, such that a person can guide the Mainframe into the rack, from the rear. The Mainframe should be fitted such that there is no restriction to the ventilation at the rear of the unit. If external SCSI devices are to be connected it is recommended that these be placed on a rack tray above or below the Mainframe.

It should be noted that typically the Mainframe unit is fitted with a boot drive with SCSI I.D. '0'(although the boot drive can be at any ID). As the Mainframe uses fans for its forced ventilation system, these generate a degree of ambient noise. The Mainframe should be located in an air conditioned machine room away from the studio and other heat generating equipment.



1. Install Mainframe into 19 inch Rack enclosure (requires removal of front panel).

2. Ensuring mains switch is in the off position, connect the input power cable.

3. Connect the printer cable to the 9-pin D connector on the SYNC I/O module of the Mainframe (the connector is marked as 'RS232').

4. Remove the front dress panel by undoing the four thumb screws.

5. Using an anti-static strap connect yourself to the mainframe chassis ground.

6. Using a small Phillips screwdriver open up the front RFI panel and ensure that all the cards are firmly seated into their respective slots by pushing on the card ears at the top and bottom of each card.

7. Replace the RFI panel and front panel on the Mainframe.

8. Connect the 15-way D connector of the Video cable to the 'Video Monitor'connector on the RIO panel of the Mainframe.

9. Connect the MFX Console cable to the Mainframe at the 24-way

Centronics connector located on the SYNC I/O module at the rear left of the Mainframe.

10. Connect any external SCSI drives and ensure that the last device is terminated. Ensure that the SCSI IDs are not in conflict with each other.

11. Connect all Sync input cables such as LTC, Word clock, and Black burst (video sync).

12. Connect all digital and analog audio input/output cables.

13. Connect 9 pin control cable to the 9 pin D connector machine A (or machine B) on the SYNC I/O module.

Mainframe Rear Panel - Detail of Connections

6.3 MFX3plus Console and Video Monitor

1. Place the MFX3plus Console at a suitable location close to the audio mixer.

2. Connect the MFX cable to the 37-pin D connector on the rear of the Console.

3. Connect the mouse to the 9-pin D connector on the rear of the Console. Please note that the mouse is no longer required. By holding the shift key when selecting 'X-Point' it toggles between horizontal and vertical adjustment of the crossfade parameters.

4. Connect the MFX Console power supply to the MFX Console and then connect the mains power to the MFX Console power supply .

5. Once all connections have been made to the MFX Console, it can be powered up safely at the power distribution board or wall outlet.

Note: To avoid noise on the system and earthing problems, it is advisable that the mains source for the Mainframe also be the mains source for the MFX Console.

The Fairlight MFX3plus Console and Video Monitor

6.4 External and Internal SCSI Drives

The Mainframe is designed to accept one 3.5 inch drive in the rear section. Typically the boot hard drive will be installed into the Mainframe itself, inside the rear rightmost (RIO) panel. When connecting external devices ensure that their SCSI ID does not conflict with devices fitted within the Mainframe. There is a SCSI ID switch on the rear SCSI panel for changing the SCSI ID of the internal boot drive. It is possible to optionally install two additional 3.5 inch drives in the front section of the Mainframe however these drives should be specified in the original order placed on your local Fairlight dealer or Fairlight office.

Typically Exabyte drives should be set to ID '5' when connected to the Fairlight Mainframe. It is recommended that a rack tray be fitted either above or below the Mainframe to hold external SCSI devices. The last device must be terminated with an active terminator. All other devices are to be looped through, un-terminated.

6.5 External Cable Length Considerations

The following table indicates the maximum useable length of interconnect cables.

Cable Type	Recommended Length	Maximum Length
Video Cable	10 metres (monitor dependent)	20 metres (monitor dependent)
MFX Console Cable	10 metres	20 metres
9-pin Control Cable	5 metres	30 metres
External SCSI Cables	1 metre or less, each cable	4 metres total length

7.0 New Installation Testing

The aim of this chapter is to set out a basic procedure for the testing of a new installation of all the MFX3plus system modes. The text is presented in a procedural form. All the points mentioned should be checked where available equipment permits; it may not be possible to test WCLK in if an appropriate signal is not available.

7.1 System Initialisation Test Procedure

After the system has been installed and is ready for power up, perform the following:

1. Check that the video and MFX cables are securely connected.

2. Check that all SCSI devices are connected and that each has a unique address. Exabyte drives must be set to address 5 only.
   Optical drives should be set to address 3.
   Typically, set hard drives to even addresses.
   Ensure that the last device is correctly terminated and the total length of all external SCSI cables does not exceed 4 metres. The longer the SCSI bus cables, the slower the SCSI transfer rate.

3. Check that the correct power is connected to the Mainframe and the MFX console.

4. With all SCSI devices powered down, switch on the Mainframe.

5. Initially you will observe a screen showing the DIO initialization screen as follows:

```
Transfering   DIO   Detection   Program   to   SyncCard.
Transfer OK - Attempting to Run Code at 0x00008000.
DIO Detection Program is Running.
Waiting for DIO 'INIT' Pattern ... OK
DIO #0 Present:YES - Analog In:YES - Digital In:YES
DIO #1 Present:YES - Analog In:YES - Digital In:YES
DIO #2 Present:YES - Analog In:YES - Digital In:YES
DIO #3 Present:YES - Analog In:YES - Digital In:YES
DIO #4 Present:YES - Analog In:YES - Digital In:YES
DIO #5 Present:YES - Analog In:YES - Digital In:YES.
```

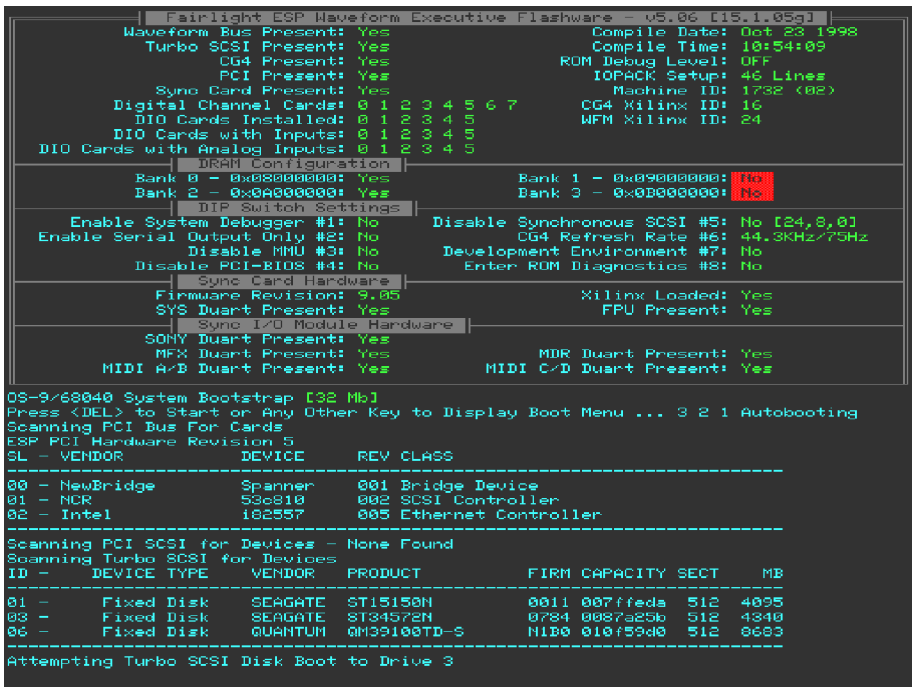
The number of DIO's detected will depend on the configuration of the system

6. The system will complete its power-on reset and the screen should turn to black.

7. The Fairlight ESP Waveform Executive Flashware configuration screen should be displayed - check for the following:

```
i)    [ Fairlight ESP Waveform Executive Flashware - v5.05 [15.1.04d] ]
      Waveform Bus Present: Yes
      Turbo SCSI Present: No
      CG4 Present: Yes
      PCI Present: Yes
      Sync Card Present: Yes
```

Note: For Turbo SCSI or PCI to be present it depends on the configuration of the machine. This screen shows that the PCI option is fitted.



Typical MFX3plus System Boot Screen

ii) Digital Channel Cards: 0 1 2 3 4 5
DIO Cards Installed: 0 1 2 3 4 5
DIO Cards with Inputs: 0 1 2 3 4 5
DIO Cards with Analog Inputs:0 1 2 3 4 5

Note: Channel and DIO cards commence with card 0 to a maximum of 5 (if six cards are fitted for 24 tracks). The same number of DIO and DCC cards should be detected - if not, check the 26-way cables at the front of each DCC card.

iii) [DRAM Configuration]
Bank 0 - 0x08000000: Yes Bank 1 - 0x09000000: No
Bank 2 - 0x0A000000: Yes Bank 3 - 0x0B000000: No

Currently 32MB RAM is fitted as standard to machines, check banks 0,2 say yes.

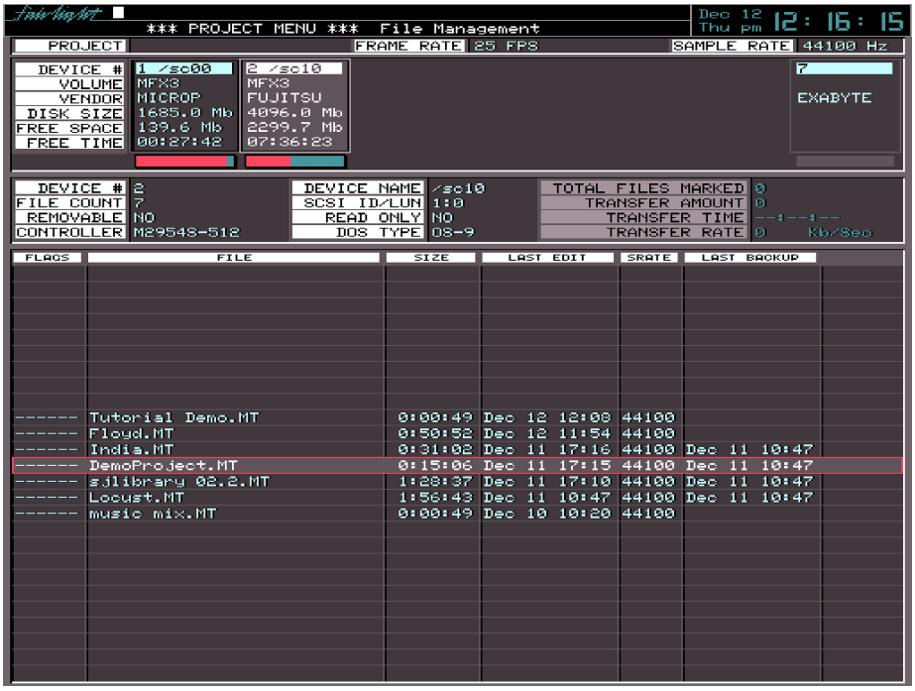
iv) [DIP Switch Settings]
Enable System Debugger #1: No Disable PCI BIOS #5: No
Enable Serial Output Only #2: No CG4 Refresh Rate #6: 44.3KHz/75Hz
Disable MMU #3: No Development Environment #7: No
Disable Copyback #4: No Enter ROM Diagnostics #8: No

All switch settings should say no except when performing diagnostics.

v) [Sync Card Hardware]
Firmware Revision: 9.05 Xilinx Loaded: Yes
SYS Duart Present: Yes FPU Present: Yes

vi) [Sync I/O Module Hardware]
SONY Duart Present: Yes
MFX Duart Present: Yes MDR Duart Present: Yes
MIDI A/B Duart Present: Yes MIDI C/D Duart Present: Yes
OS-9/68040 System Bootstrap [32 Mb]
Press <DEL> to Start or Any Other Key to Display Boot Menu ... 3 2 1 Autobooting

Check here that the system has seen 32 MB RAM



Typical MFX3plus Project Page

7.2 Audio Input Test Procedure

Power up the MFX3plus system and allow to boot to the Project page in the disk recorder. Create a new project called " Test 44 Analog ". Route an audio source (preferably low level background type music) to the first four input channels & arm these channels. Record these four tracks for a period of 15 minutes. Replay the recording, listening carefully to each channel. Jump to the end of the recording you have just completed and remove the source of the music. Record 5 minutes of silence (no audio in). Record onto all available channels & listen to this recording on each channel. No sync set up is required as the MFX3plus will be in its default sync mode. Close the project and proceed to step 7.3.

7.3 Digital Input Test Procedure

Perform step 7.2 again except this time call the project " Test 44 Digital " . Digitally arm all available inputs by selecting the ARM menu and under TYPE, turn the Jogger wheel until AES is selected & press the enter key. Next verify the sync input mode by pressing BLUE DIGI, ensure that HOUSE is selected and that SYNC is AES or where word clock is available, if connected this may be selected (WCLK). Perform a recording as in step A. Play back the recording paying particular attention for clicks etc. If available connect the digital outputs to a quality AES DAC and monitor the digital outputs while in playback. Typically when digitally recording select WCLK as the sync if it is available.

7.4 Syncronization Test Procedures

7.4.1 9-pin Control

If not already connected, connect the 9 Pin control cable to the Mainframe. Select REMOTE on the 9 Pin device and insert media striped with time code. Select the M1 key to the right of the jogger wheel. Press the various transport keys and observe that the 9 Pin machine is locked and operating as per required. Deselect M1 and proceed to the next step

7.4.2 LTC In

Press the M2 key. Press the BLUE key and the DIGI key at the same time and select MASTER M2 ON. Open a project and connect a source of LTC into the Mainframe. When PLAY is pressed the MFX will jump to the time code position of the incoming LTC source. Open a project with audio and copy the audio to the timecode location of the incoming signal. Listen to the audio while locked, for clicks or dropouts. Deselect the M2 key by pressing again.

7.4.3 LTC Out

Connect the MFX3^{plus} LTC output to an external device. Press the SETUP/GEN key and press the PLAY key on the MFX. Set the slave device to play and observe that it tracks MFX3^{plus}.

7.4.4 Locked to Video

Connect a video black reference source into the Mainframe. Under the BLUE DIGI menu under SYNC select VIDEO. Press the ESC key and then Z. Observe that the last line indicates that Video sync is detected. Remove the video source and select VIDEO as above. Observe that an error message is displayed.

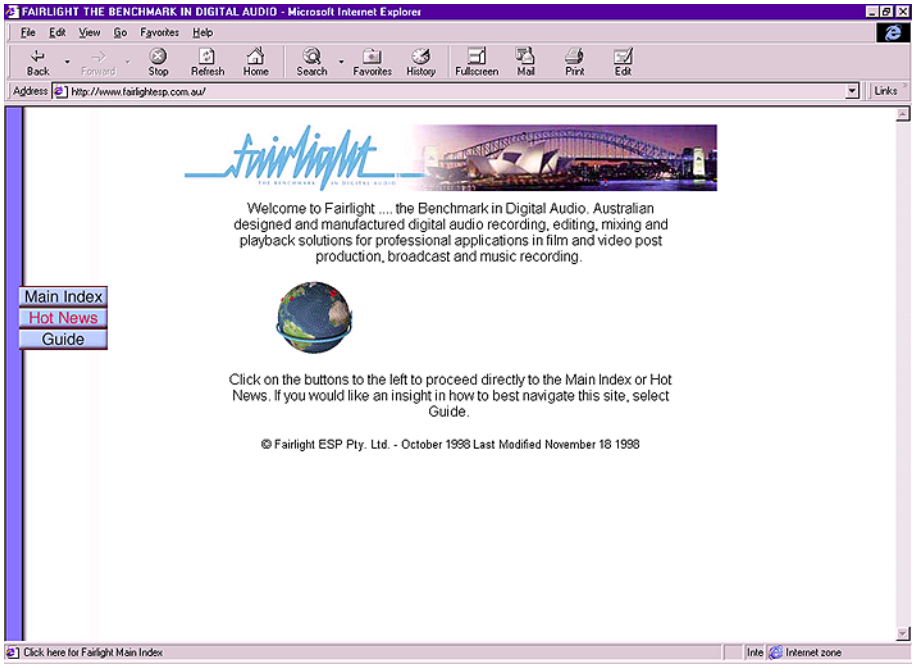
8.0 Obtaining Technical Support

Additional Technical Support for the Fairlight MFX3plus Digital Audio Workstation, which is not covered by this publication, may be readily obtained from a variety of sources, not least of which is your local Fairlight office or Authorised Fairlight Dealer. Other sources of this information are detailed in the section below.

8.1 Internet

Detailed information concerning all Fairlight Products and Services is available on our Internet Web Site, which is located at www.fairlightesp.com.au. Its user-friendly design allows you to easily source the latest news concerning product development and availability, current and past Fairlight Newsletters, Bulletins and Press Releases, Distributor and Dealer contact details, employment opportunities and a brief company history.

The Web Site is currently undergoing a transformation to further enhance our product support and after sales service. The ability to download the latest software, technical documentation, and an approved Peripheral database are some of the new features to become available. A comprehensive Fairlight User Network including hints and tips to get the most out of our products, a FAQ section and links to other useful digital audio sites, will also form part of the structure.



The Fairlight ESP Internet Web Site Home Page

8.2 On-Line Technical Support

Online technical support is available via the Internet from our Web Site. Just point your browser to:

http://www.fairlightesp.com.au

click on products then click on tech support. Once there, you will find links to our FTP site for the latest software and firmware updates, up-to-date software bug information, an up-to-date ECN list, a listing of tech support leaflets and a place to ask specific technical questions. Technical support queries will be promptly answered in the order they're received.

8.3 Technical Support Leaflets

Technical support leaflets such as those found in appendix A of this publication are always available on our Web Site in the form of PDF documents. Just go to:

http://www.fairlightesp.com.au

click on Products,then click on Tech Support, then on Technical Support Leaflets. When you're there you'll have the opportunity to view or download what you like. New Leaflets and updates to current leaflets will continually be posted to the website. Regular visits will help keep your references current and up-to-date.

8.4 ECN Updates

ECN updates are available as Microsoft Excel documents from our Web Site, located at:

http:www.fairlightesp.com.au

Simply click on Products, then Technical Support, and finally Engineering Change Notice to access them. These updates can be easily viewed or downloaded, and there are examples of these illustrated in Appendix A of this Service Manual.

It is therefore strongly recommended that you visit our Web Site on a regular basis to be kept informed of the latest developments and changes concerning ECN's and other technical support documentation.

8.5 FTP Site

8.5.1 Introduction

This Section details the procedures for downloading files from Fairlight's FTP site for upgrades to the MFX3plus system.

FTP, which stands for 'File Transfer Protocol', is the predominant protocol for transferring files over TCP/IP networks. Although FTP originated as a Unix utility, it is now available in many other environments including Windows 95, 98 and NT. PCs that have been set up for TCP/IP networking can access an FTP site in several ways. The most basic of these is a command line interface included with Windows, other methods are via a dedicated FTP Client program which can be downloaded and purchased over the Internet, or using an Internet Browser.

The current implementation of the FTP site is to provide an alternative for the existing BBS system, thus eliminating the need for long international phone calls and the unpredictable quality of international connections. The new system will also provide the basis for taking advantage of future developments with Fairlight's products, as well as any new developments with Internet technology.

8.5.1.2 Getting connected

To get an account on the FTP site, if you do not have access already, you will need to contact Fairlight by Email at the following address:

mail@fairlightesp.com.au

You will then be issued with a user name and password.

8.5.1.3 What you will find

Once you are connected to Fairlight's FTP site, you will find several directories containing the files and documents you will need to upgrade and maintain Fairlight products. The directories you will see depend on the access rights you have been given by Fairlight. The directories you will see in this manual may differ from those you will see once connected.

You will notice that many of the files destined for the MFX3plus will have an accompanying '.crc' file. This is a text file used for checking the integrity of the final transfer. By running the 'crc' program on the MFX3plus and checking the results against those listed in the 'crc' file, you can determine if the file is correct. A PC version is available from the UTILS/CRC directory of the FTP site.

8.5.2 Equipment and Software

8.5.2.1 IBM Compatible PC

The procedures outlined in this document are based on an IBM PC compatible running Windows 95, Windows 98 or Windows NT. Users with experience on other platforms may be able to perform equivalent procedures. The PC should also be fitted with 16550 UARTS for high speed serial communications. This is only an issue for older PCs, as most newer models have these fitted as standard.

8.5.2.2 Internet connection

A connection to the Internet is required. This can be via a modem or a permanent connection. Either way, check that you can run all the standard Internet features to ensure your system is working correctly. Since so much literature is available on Internet connections, and considering the number of things that can go wrong when getting it working, this document will assume you have it all organised.

8.5.2.3 TCP/IP Protocol

The PC must be set up to use TCP/IP protocol. If any part of the procedure is going to prove difficult to set up, it will be the TCP/IP settings. If you are unable to make an FTP connection to Fairlight's site, check to see if you can connect to other sites before assuming the Fairlight site is not working (e.g. ftp.microsoft.com). You may not have access to other sites, but if it asks you for a name and password, that's a good sign.

8.5.2.4 FTP Client or Web Browser

It is possible to download files from the FTP site from the MS-DOS prompt, but it will make life easier if you use an FTP Client or Web Browser. The FTP Client used in the examples in this manual is FTP Voyager. This is available from the following web site:

http://www.ftpvoyager.com

Note: Other programs are also available from other vendors.

A standard Web Browser such as Microsoft Internet Explorer can also be used to download files, and is required if you want to change your password. It is recommended that you use the latest version downloaded from the Net.

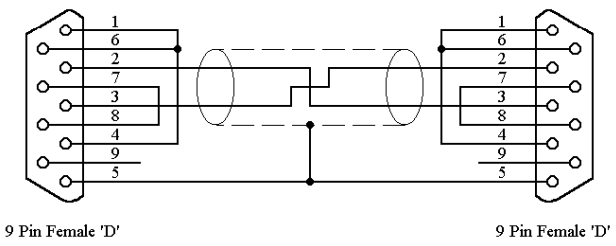
8.5.2.5 Terminal program

A terminal program supporting Zmodem transfers is required to send the file from the PC to the MFX3. HyperTerminal, which is included with Windows 95, 98 and NT, is suitable for this purpose.

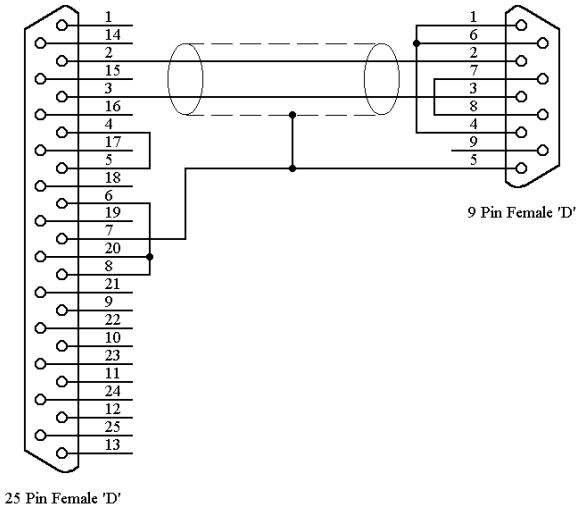
8.5.2.6 Null modem cable

Once the files have been downloaded to a PC, a Null Modem cable is required to transfer the files to the MFX3plus. The 9 pin to 9 pin cable is the most common and can be used with a 9 pin to 25 pin adapter for use with 25 pin Com ports.

Null Modem cables can usually be purchased ready made from most computer stores. To make your own, use the wiring as detailed below:



9-pin to 9-pin Null Modem Cable



25-pin to 9-pin Null Modem Cable

8.5.3 File transfer using Windows FTP

8.5.3.1 Connecting to Fairlight's FTP site

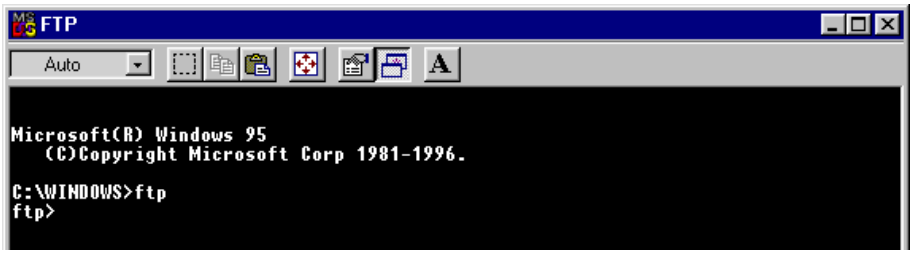
8.5.3.1.1 Starting an FTP session

Start an FTP session with one of the following methods:

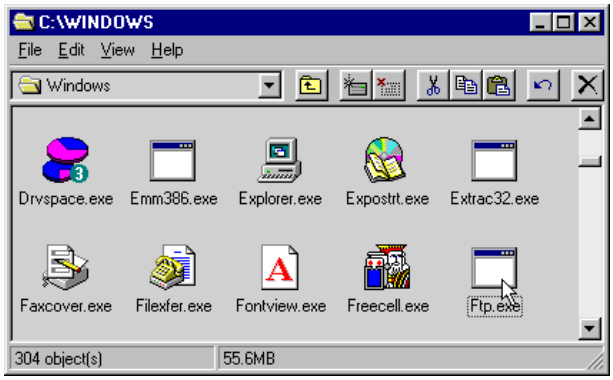
a) Select Programs from the Start Menu, select MS-DOS Prompt, type:

```
ftp <return>
```

OR



b) Double-click on the FTP icon in your Windows folder. It is possible to create a shortcut to this for future use.



OR

c) Select Run from the Start Menu, type in FTP, and click OK.
Note: This may actually run an alternative Browser program if one has been configured as your default FTP program. Some internet browsers may change this when they are installed.

8.5.3.1.2 Connecting

At this point, if you do not have a permanent internet connection, you will have to use Windows Dial-up Networking to connect to an internet provider as you would for normal Internet and Email use. It is not necessary to run your Internet browser or Email software.

8.5.3.1.3 Opening the FTP site

Connect to Fairlight's FTP site with the following command:

```
open    ftp.fairlightesp.com.au    <return>
```

Note: It is also possible to open the ftp site directly from the MS-DOS prompt in one step with the following command:

```
ftp    ftp.fairlightesp.com.au    <return>
```

8.5.3.1.4 User name

```
ftp> open ftp.fairlightesp.com.au
Connected to ftp.fairlightesp.com.au.
220-Welcome to Fairligtht FTP
220 Service ready for new user
User (ftp.fairlightesp.com.au:(none)):
```

Enter your user name as supplied by Fairlight and hit <*return*>.

8.5.3.1.5 Password

```
ftp> open ftp.fairlightesp.com.au
Connected to ftp.fairlightesp.com.au.
220-Welcome to Fairligtht FTP
220 Service ready for new user
User (ftp.fairlightesp.com.au:(none)): s.bartfast
331 Password required
Password:
```

Enter your password as supplied by Fairlight and hit <*return*>.

Note: Your password will not appear on the screen as you type.

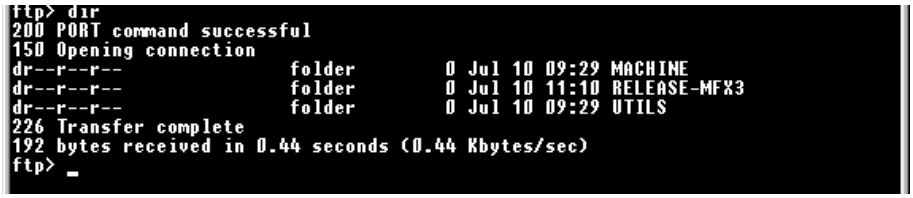
If you have made a successful connection, you will be returned to the ftp prompt after showing 'User logged in'. If there has been a problem, the system will print 'Login failed'.

8.5.3.2 Downloading files

8.5.3.2.1 Root directory

Once logged in, you will be able to access certain directories depending on your access rights as given by Fairlight. To see a list of directories and files, type the following:

`dir` *<return>*



Use this command at any time to display the contents of your current directory. To list the contents of a certain directory, use the 'dir' command followed by the directory's name:

`dir` *<directory_name>* *<return>*

e.g:

`dir machine` *<return>*

8.5.3.2.2 Changing the current directory

Change the current directory to the one containing the desired files.
In this case, we will use the Machine file as an example.

`cd machine` *<return>*

Note: To go back one step on the directory structure, type:

`cd ..` *<return>*

Noting that unlike DOS, a space is required after the cd i.e:

`cd` *[space]* `..` *<return>*

8.5.3.2.3 Changing the local directory

Change the local directory to where you would like the files placed. This will usually be a directory on your PC.

```
lcd   <directory_name>   <return>
```

e.g:

```
lcd   d:\data\download   <return>
```

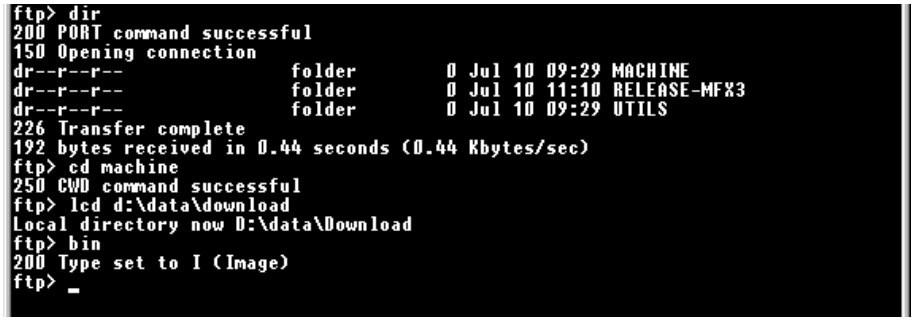
Note: Substitute the directory path with your own.

8.5.3.2.4 Binary transfer mode

Set the system for binary file download with the following command:

```
bin   <return>
```

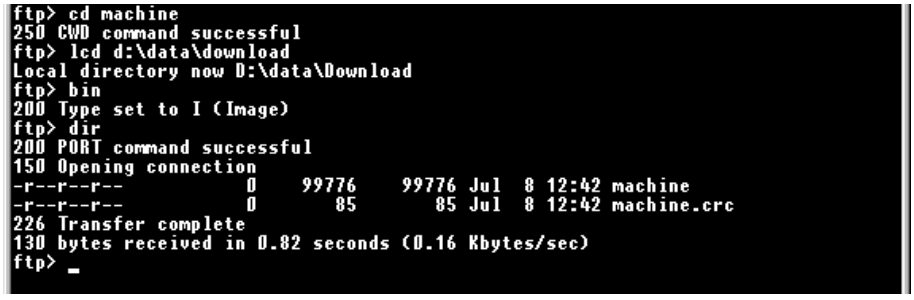
Note: It is only necessary to type this once per session. If this command is not sent, files may be corrupt when downloaded.



8.5.3.2.5 Listing files

Use the 'dir' command to display a list of files in the current FTP directory:

```
dir   <return>
```



8.5.3.2.6 Downloading

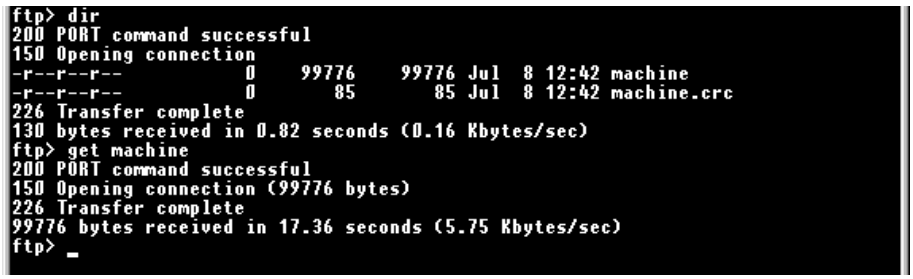
Download a file with the following command:

```
get  <filename>  <return>
```

e.g:

```
get  machine  <return>
```

Note: Substitute the filename as required.



8.5.3.2.7 Ending a session

When finished, close the connection with the following command:

```
quit  <return>
```

8.5.3.3 FTP Commands

The following is a list of other commands you can use when accessing the site. Please remember that they are case sensitive. This means that if you use "BIN" instead of "bin" you will get an error message from the FTP server.

bin — The '**bin**' command tells your system to retrieve data in an 8-bit format. If you do not use the '**bin**' command and you retrieve an 8-bit file (such as a .zip or .gz file) the file will be corrupt.

cd — The '**cd**' command has the same use as the '**cd**' command from DOS. If you enter '**cd** *directory_name* <*return*>', you will make the directory the current directory. Note that you cannot enter '**cd..**' like you can in MS-DOS, you must use '**cd ..**' (that is '**cd** <*space*> **..**') to go back a directory.

close — Close the current FTP connection. This will then return you to the very first ftp prompt.

del — Used to delete a file if you have permission.

dir — Lists the files and directories in the current directory or the specified directory. Equivalent to the **ls -al** command.

get — '**get**' is used when you want to retrieve a file from the FTP server, the command syntax is '**get** *filename*', remember to use the '**bin**' command before you do this. If you do not use the '**bin**' command then the file may be corrupted when your receive it.

hash This command is useful as it makes the software print a hash '#' symbol every time a certain amount of data is downloaded to your PC. Usually when you decide to download a file you would type '**get** *filename <return>*', at which stage no indication of activity is displayed until download has been completed. If you enter the '**hash**' command, you can see that your PC is downloading data.

help Prints a short explanation of the command you specify. If you enter help without specifying a command, you will receive a list of the commands available in FTP.

lcd When you first run the FTP program from your PC, any files that you retrieve will be sent to the directory that you were in when you started FTP. This is often not convenient. To change the directory that files will be saved to on your PC, use the '**lcd**' command to change the local current directory.

ls '**ls**' is a Unix command that can be used to display file and directory information. '**ls**' on its own displays the current files on the FTP server. As with the '**dir**' command on your PC, there are various switches that you can use. Using **ls -al** will list additional information such as file size and is equivalent to the **dir** command.

mget '**get**' is fine if you only want to get one file. However, if you want to retrieve multiple files, then you can use the '**mget**' command. You can experiment with wildcards. If you specified '*.zip', then '**mget**' would only try to retrieve '.zip' files.

mkdir This is the same as the '**MD**' command in DOS and is available only if you have been given permission.

mput The opposite to '**mget**'. This command allows you to send multiple files to the server if you have permission.

open Establishes a connection to the FTP server on the specified host.

pwd This command tells you the name of the directory that you are in on the FTP server.

quit Logout from the current FTP connection and return to the operating environment.

rename Does the same as the DOS rename command, i.e. renames a file. This can only be done if you have been given permission.

rmdir This command removes the directory that you specify if you have permission.

send '**send**' is the opposite of '**get**'. With this command you can send files to the FTP server (if you have been given permission).

user With the '**user**' command it is possible to re-log into the FTP server with a different account.

8.5.4 File transfer using an FTP Client

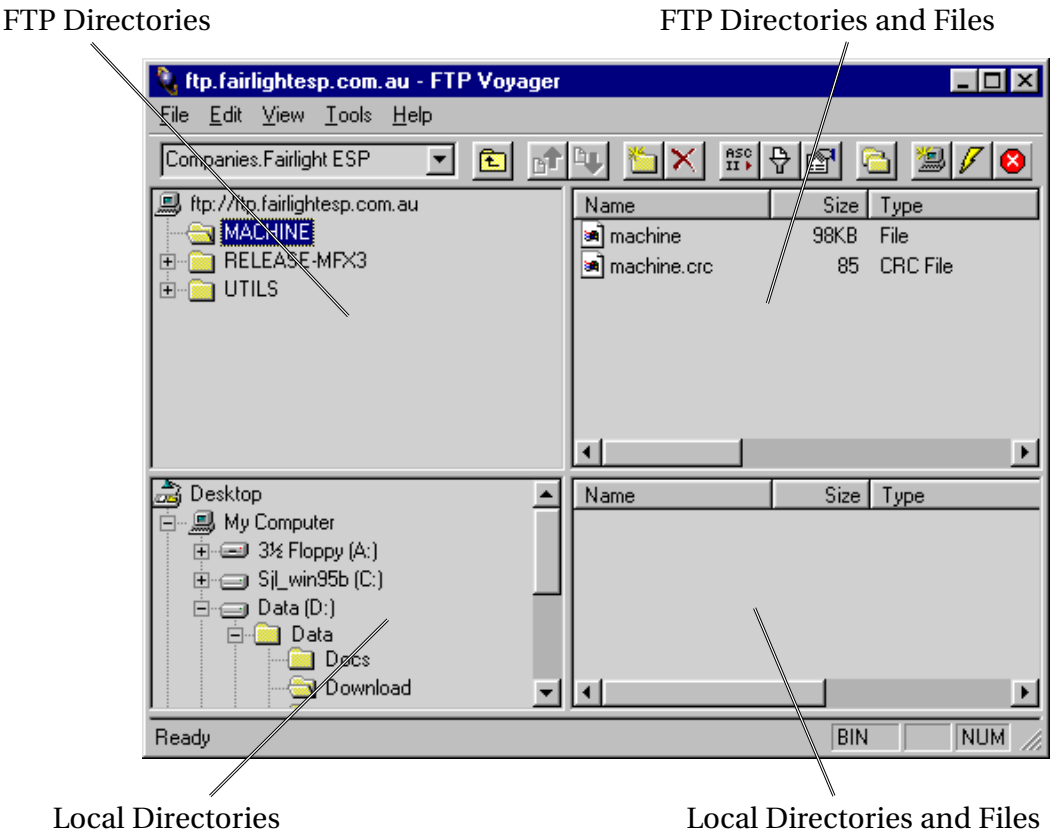
8.5.4.1 FTP Clients

FTP client programs offer the familiar 'drag and drop' interface similar to Windows Explorer. It is possible to configure such programs to automatically log on to specific sites and directories within those sites at start-up.

The example screen below is from 'FTP Voyager' available from the following Web site:

http://www.ftpvoyager.com

The Help files included with these programs have instructions for connection and configuration.

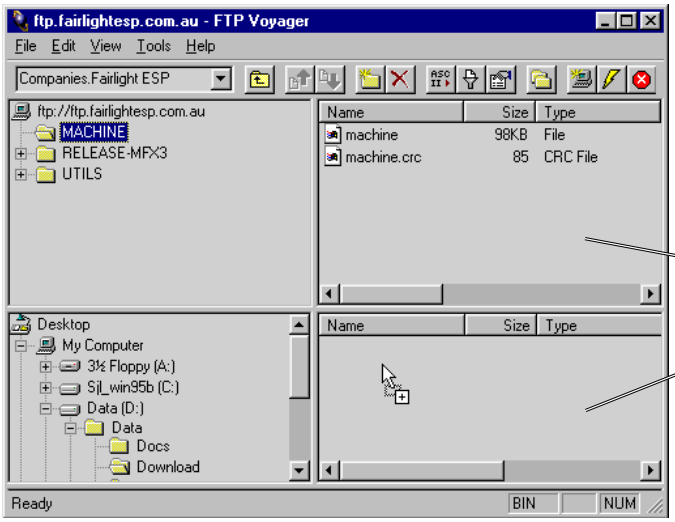


Some other programs can be found at:

http://www.us.terra-net.com
http://www.ipswitch.com
http://www.cuteftp.com
http://www.ftppro.com
http://www.ftpvoyager.com

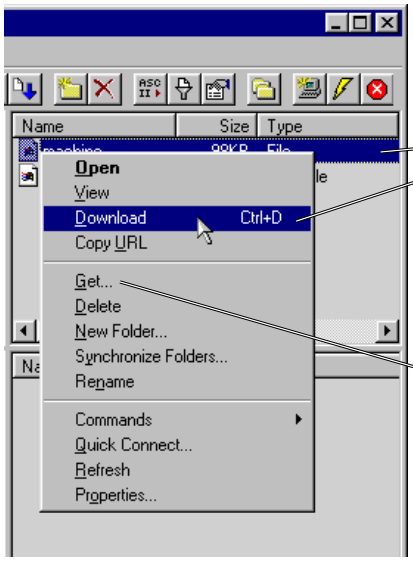
8.5.4.2 Downloading files

Like Windows Explorer, there are several methods available to copy files. Two of the basic methods offered by FTP Voyager are as follows:



To copy files to your PC simply 'drag and drop' as required

OR



'Right Click' on the desired file and select 'Download'. This will put the file into the local directory displayed in the lower window.

Alternatively, select 'Get' for a choice of download locations.

Note: It is possible to select multiple files for download. This is done in the same manner as for other Windows programs. i.e. selecting a range of files with the mouse, or holding down <Alt> and clicking on the files.

8.5.5 File Transfer using a Web Browser

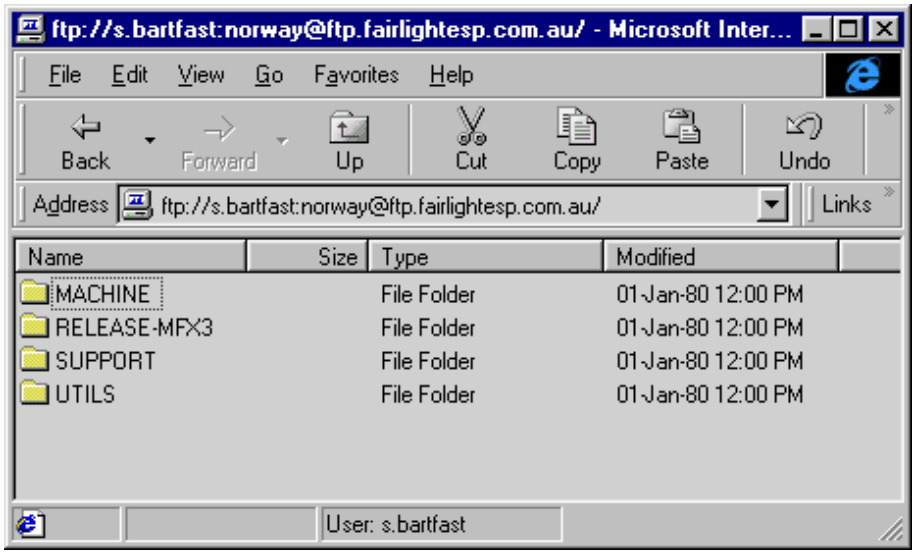
8.5.5.1 Connecting to the FTP site

To connect to the FTP site, enter the address into your browser as follows:

ftp://s.bartfast:norway@ftp.fairlightesp.com.au/

fttp:// username colon password @ ftp.fairlightesp.com.au/

Note: If you use this method, your password will be visible on the screen and in history files! Please bear this in mind if others use your computer.

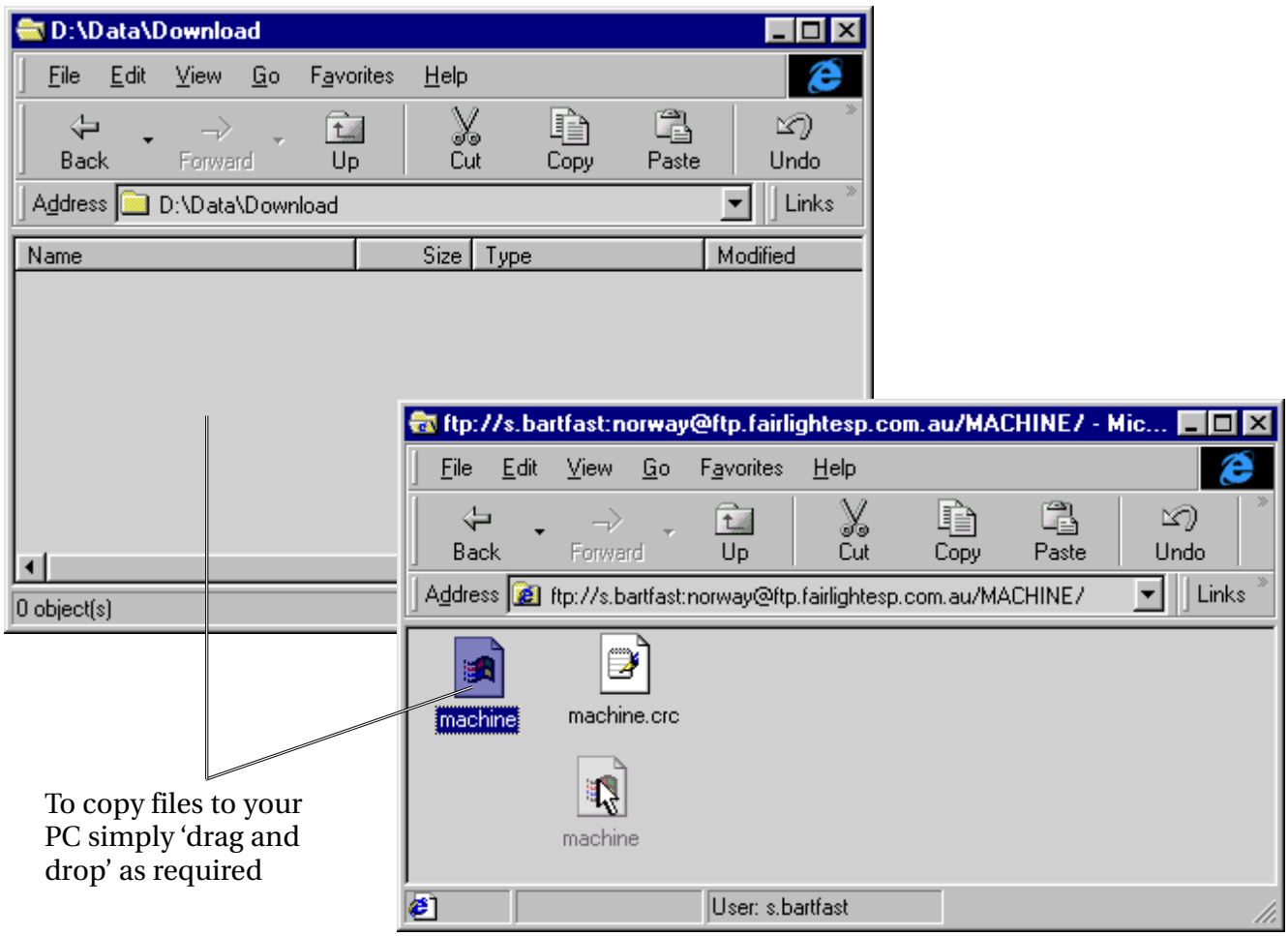


Once you have connected, the directories and files will be displayed according to the 'View' settings of your browser.

If you have an old version of your browser, you may not be able to perform all these tasks. It is advisable to download the latest version from the Net. It is recommended that you use Internet Explorer 4 or later.

8.5.5.2 Downloading files

To download files, simply drag and drop into the required directory on your PC.

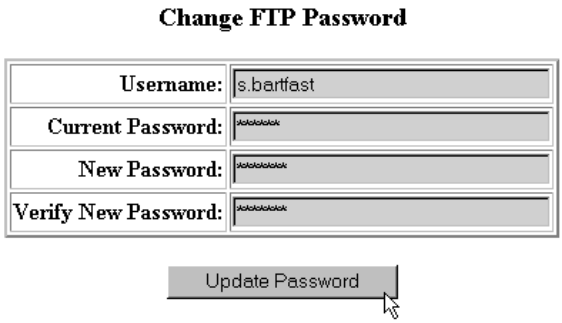


8.5.6 Administering your account

To administer your FTP account, use an internet browser to display the following web site:

http://ftp.fairlightesp.com.au/

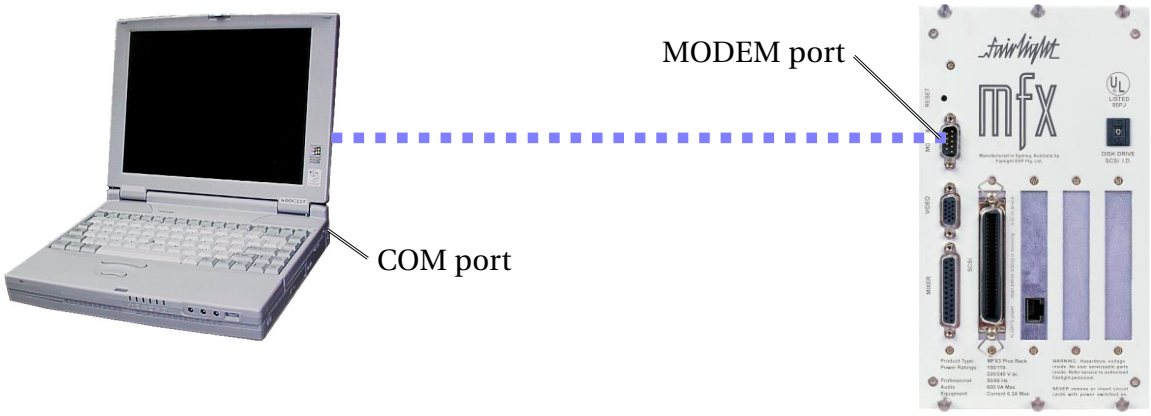
Selecting "Change Password" will take you to a page where you can enter a new password.



8.5.7 Transferring files to an MFX3plus

8.5.7.1 Connecting the MFX3plus

Connect a 'Null Modem' cable between a spare Com port on your PC, and the 'Modem' port on the rear of the MFX3plus.



8.5.7.2 MFX Telix

The following procedure is required so that MFX3plus is ready to accept files from the PC:

Step 1: Close all projects and then quit the Disk Recorder application with the following command:

```
quit  <return>  y
```

This should leave you at the '#' prompt.

Step 2: Change to the root directory:

```
chd  /dd  <return>
```

It is possible to select a specific directory if required. Software and Machine files are placed in the root directory.

Step 3: To be safe, rename any files that are to be replaced as a backup, for example:

```
rename   machine   machine.old   <return>
```

Substitute other filenames for 'machine' as required.

Step 4: Run the Telix program:

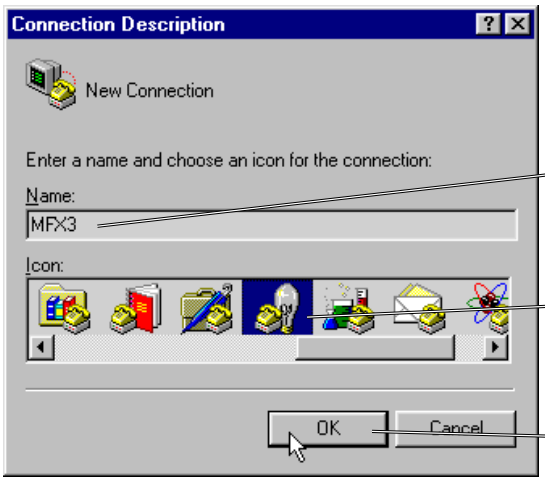
```
telix   <return>
```

8.5.7.3 PC HyperTerminal setup

Use the following procedure to set up a HyperTerminal session on a PC for use with MFX3plus. Once set up, future sessions can be started by running from the new icon and jumping straight to performing the transfer (Section 8.5.7.4).

Start a new HyperTerminal session from the Windows 'Start' menu.

Select: Start->Programs->Accessories->HyperTerminal



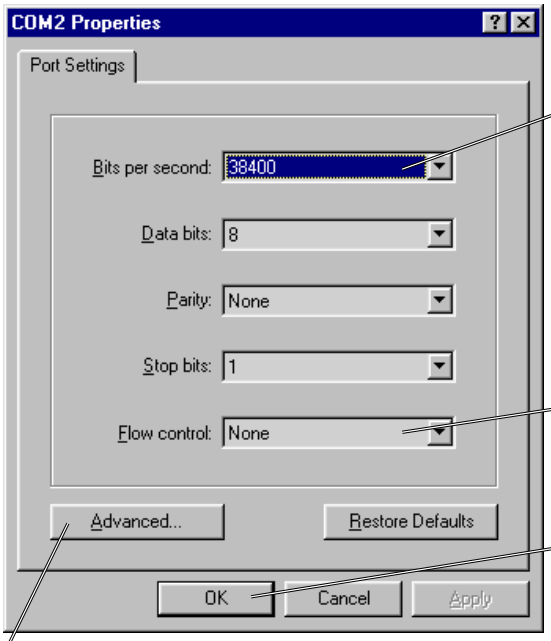
Step 1: Type a name for the session.

Step 2: Select an icon.

Step 3: Select OK.

Step 4: Select a direct connection to the Com port used for MFX3plus.

Step 5: Select OK

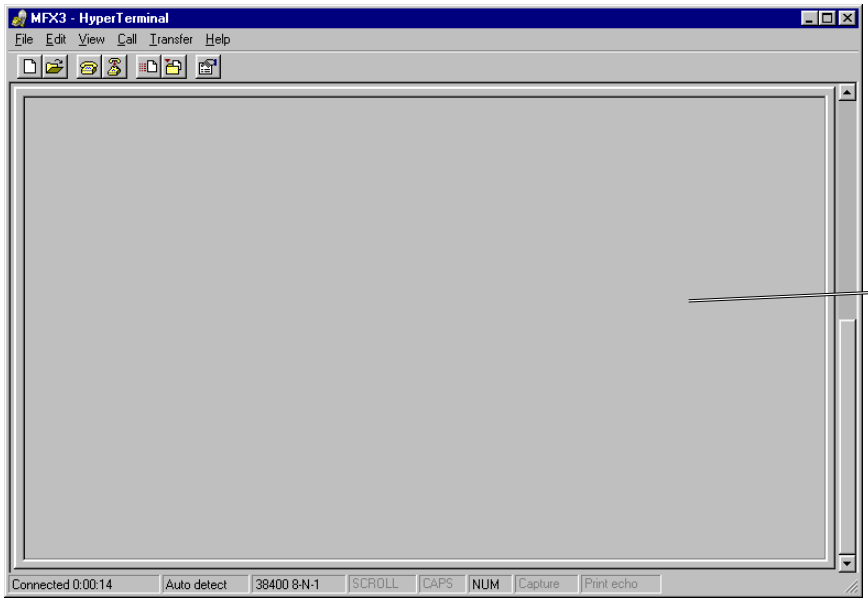


Step 6: Select 38400 Baud

Step 7: Select Flow Control - None

Step 8: Select OK

Note: The Advanced options should be set to default.



Click in the HyperTerminal window and type some characters to check communications with MFX3plus. The characters should appear on the MFX3plus screen.

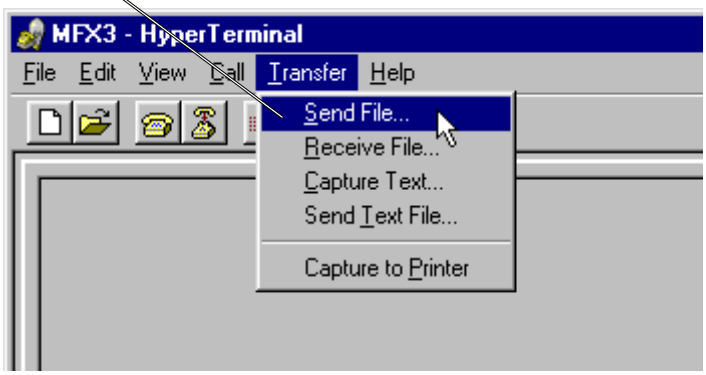
With Telix running on the MFX, and HyperTerminal running on the PC, you should be able to type characters on either system and have them appear on the other. This is a quick way to test the system prior to attempting file transfers.

Note: When exiting the program, you will be prompted to save the session. Select 'OK', so as to be able to run the program directly from the previously selected icon and skip this set-up procedure in the future.

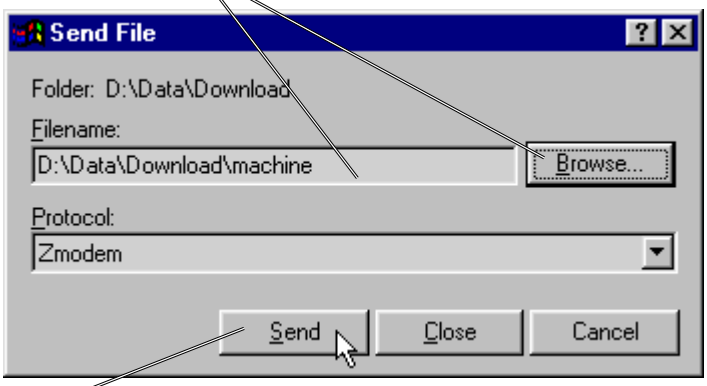
8.5.7.4 HyperTerminal Transfer

Once Telix is running on MFX3plus and HyperTerminal is set-up and running on the PC, use the following procedure to transfer files:

Step 1: Select Transfer->Send File.



Step 2: Type in or browse for the required file(s).



Step 3: Select Send.

If all is well, you will see the transfer start on both systems. Hold down the <ctrl> key and hit 'c' to exit the Telix program.

8.5.7.5 Setting the file attributes

Once files have been transferred to MFX3plus, it is essential to change the attributes of the files to allow normal operation.

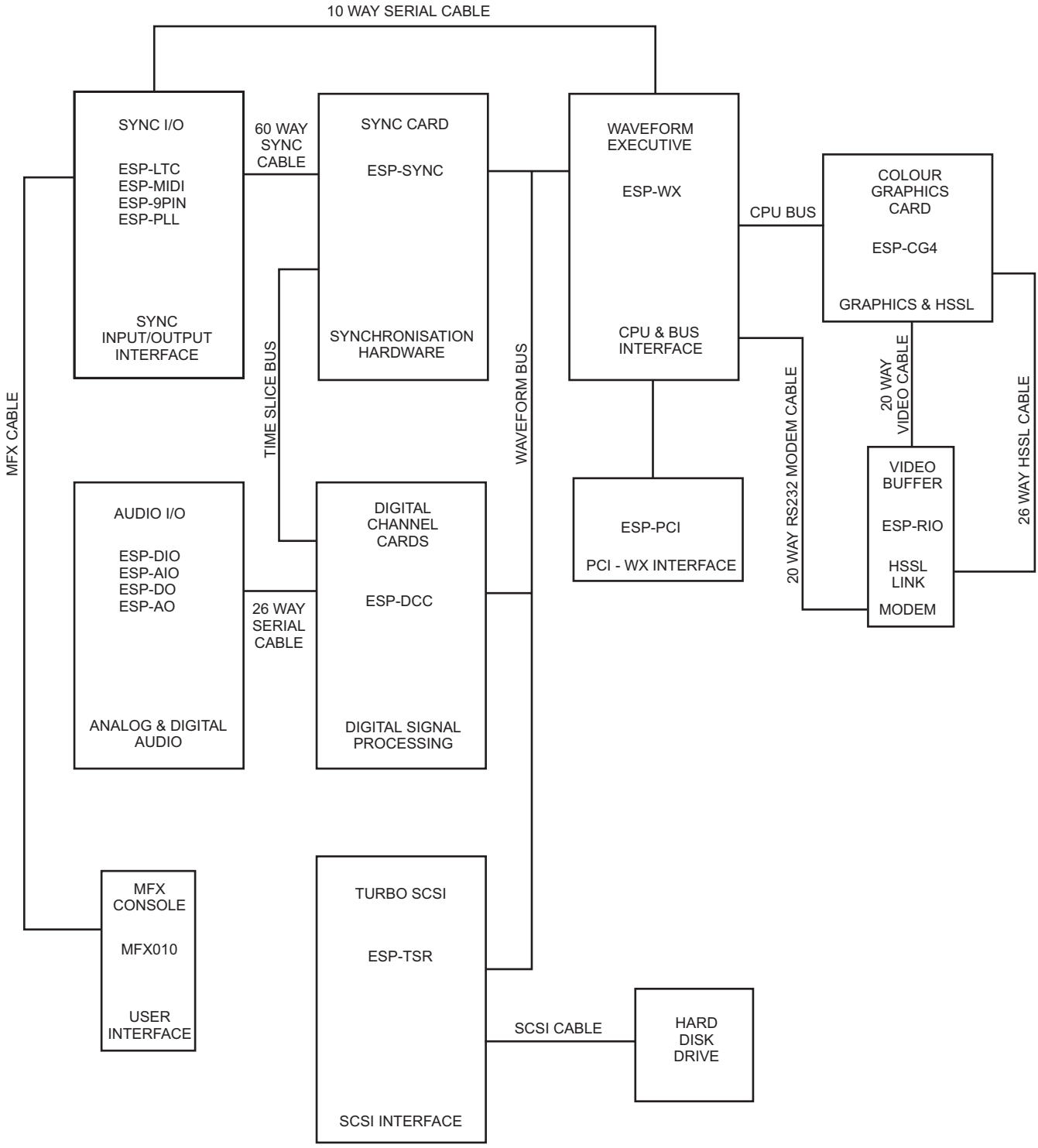
Type the following for each file transferred:

```
attr    <filename>  -erw  <return>
```

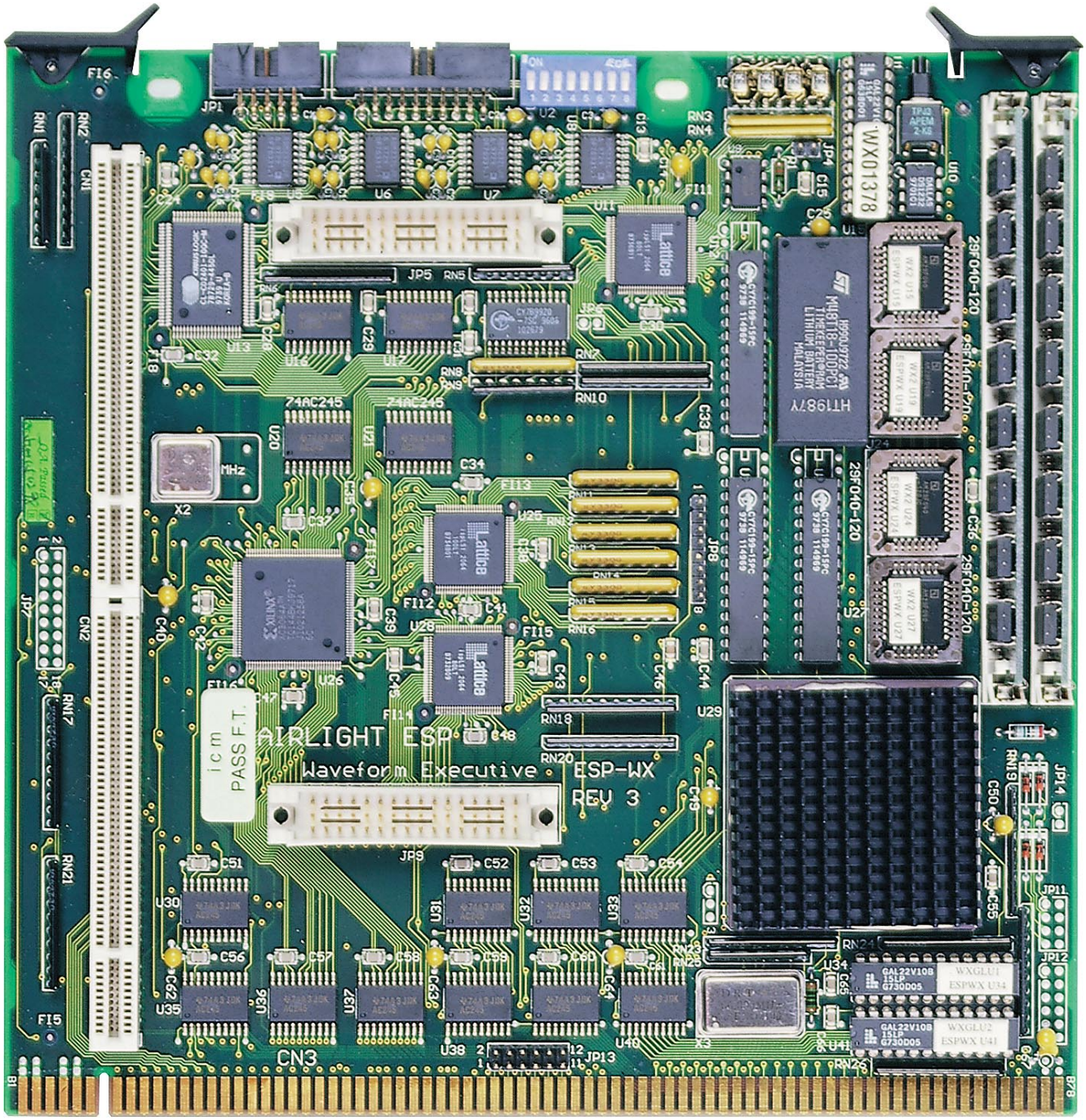
e.g:

```
attr  machine  -erw  <return>
```

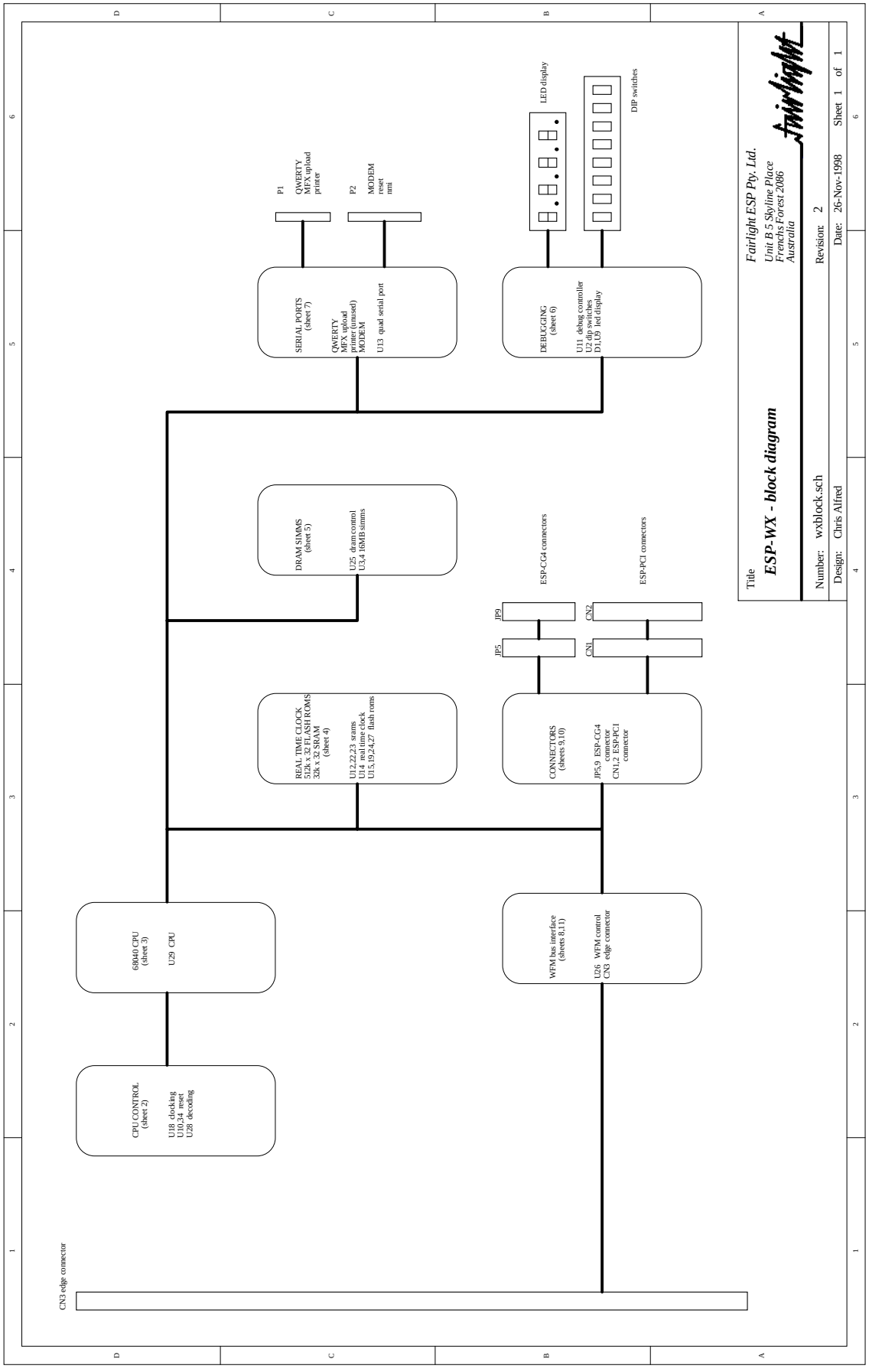
9.0 MFX3plus Block Diagram



10.0 ESPWX Waveform Executive Card



10.1 ESPWX Block Diagram



10.2 ESPWX Circuit Description

10.2.1 Document Revision

11.4.1996	v1.0	cea:	created
15.4.1996	v1.1	cea:	proof read
10.9.1996	v1.2	cea:	16M simms
16.10.1996	v1.3	cea:	Rev 2.1 PCB release

10.2.2 Terminology

DRAM	Dynamic RAM
SRAM	Static RAM
FROM	Flash ROM
WS	CMI-41 Waveform Supervisor
WX	ESP-WX Waveform Executive
SC	ESP-SYN Sync Card
TS	ESP-TS Turbo SCSI Card
PCI	ESP-PCI PCI Interface Card
CG4	ESP-CG4 Graphics Card
RTC	Real Time Clock
OS	Operating System (OS9 for 68xxx)
WFM	Waveform Bus
PLL	Phase Locked Loop

10.2.3 Introduction

The WX is a stand-alone 68040 based CPU card with interfaces for the WFM bus, PCI card, and CG4. The WX replaces the WS and all P1/P2 cards.

10.2.4 Installation

All P1/P2 cards and the WS card are to be removed (during initial production, the CG3 may be used while the CG4 is not operational).

If the TS card is to be used, then the WX is placed in the WS slot. Note that the ESP-TS card must be modified to operate with the ESP-WX. If the TS is not to be used, then the TS is removed, and the WX installed in the TS slot. This configuration is used when PCI is installed. Note that the jumpers at JP13 must be installed.

WX connector JP1 connects the 10 way ribbon cable which was connected to the Q133 connector SO2.

For systems with the Q137 front panel LEDs and switch board, the 20 way cable to the Q137 connects to JP2 on the WX.

The CG4 plugs onto connectors JP5 and JP9 with the CG4 components towards the WX card.

The PCI connects onto CN1 and CN2. Note that there is a metal support bracket for the PCI.

10.2.5 General overview

All clocking on the WX card is synchronous to the CPU (68040-33 U29) and at 33.000MHz derived from the 66.000MHz crystal X3. To distribute the 33MHz system clock, a PLL/buffer chip (CY7B9920-7SC U18) provides individial outputs for each device requiring the clock. The operating system is contained in Flash ROMs (29F040 U27,U19,U24,U15). As these devices are in-system programmable, they need only be programmed once in a programmer; subsequently they are programmed by software.

A realtime clock chip (DS1643 U14) is used to maintain the data and time for the operating system. As this device appears as non-volatile memory, this chip is also used to hold system configuration information. SRAM chips (M5M5278DP-15 U22,U12,U23) are used to extend the memory to 32 bits wide - these 24 data bits are volatile. This memory is used to hold system confuguration data.

DRAM is installed as SIMM modules (in sockets at U3,U4). Initially 16M is installed at U3, a further 16M SIMM can be installed in U4 and will be automatically detected by the software.

There are four RS232 serial ports provided by a quad serial chip (CS2401 U13):

1. RS232 serial port to QWERTY keyboard in MFX console
2. P1 spare serial out port
3. MFX serial port used for MFX upload
4. COMMS spare serial port to Q137 front panel card

The interface to the WFM bus is implemented in a XILINX (XC3064A-6 U26) which is uploaded after reset. This chip also includes a 100Hz clock (OSCLK) divided down from a 20MHz crystal input. When the operating system starts, the time is read once from the RTC and then maintained via an interrupt generated by the 100Hz clock.

A quad 7-segment LED displays system operation for debugging. The digits are allocated as:

1. Left-most processor running status
2. current interrupt level pending
3. debug left
4. Right-most debug right

The processor running status is the value provided directly by the 68040. Normally this shows ‘8’ when running,and ‘5’ when the operating system has nothing to do. Other values usually imply something is wrong. The interrupt level should show ‘0’ or flicker to other values, if another value is persistant, then the interrupts are not being serviced by the CPU correctly. The debug left and right digits are used during software operation to indicate the progress.

The decimal points on the display are allocated as:

1. left-most OSCLK 100Hz interrupt enabled
2. serial port interrupt enabled
3. [spare for debugging]
4. right-most interrupt pending

When the operating system is running, decimal points 1 and 2 are on, 3 is off and 4 flickers.

There are 8 DIP switches which are used during diagnostics and selection of the operating system boot mode. For normal operation, all DIP switches should be OFF. After reset, the DIP switches are read to select the boot mode as below:

DIP switch

8	enable ROM diagnostics
7	spare
6	spare
5	disable PCI BIOS (disable synchronous SCSI, Rev 15 Software)
4	disable copyback caching
3	disable MMU
2	disable CG4, use serial port
1	enable ROM debugger

To allow hardware debugging, the jumper at JP4 is connected to a logic analyser to provide a trigger pulse during diagnostics. The connectors JP5 and JP9 (used to connect to the CG4) provide easy logic analysis access to all significant CPU signals.

The WXDONG pal (22V10-15 U1) is coded with a 4 byte dongle code. Each read from the dongle reports one dongle byte (data bits 0..7) and the byte number (data bits 8..9). The byte 0 includes the PCB revision which is hard coded on the PCB to the inputs of the WXDONG pal.

10.2.6 Detailed Description

10.2.6.1 CPU control

(see 10.4.2 CPU Control schematic)

The main devices on this schematic are:

1. **WXGLU1 pal**
   Controls *RESET,*LRESET,*RSTI reset signals.
   Inverts A25 to *A25 for WFM bus interface.
   Controls *CPU bus grant signal (*CPUBG).
   Controls Flash ROM ROMA20 line.
   Divides 66.000MHz crystal by 2 to generate BCLK.

2. **U18 CY7B9920-7SC**
   PLL and buffers to drive system clocks.

3. **WXCPUC Lattice**
   All address decoding.
   Byte write selection (*WE0..3).
   Programmable device in-circuit programming interface.
   Bus error detection (*TEA).

4. **WXGLU2 pal**
   Controls Lattice program enable *LISPEN.
   Routes Lattice/XILINX program data (LXSDO).

When the system is powered-up or reset via S1 (or Q137 front panel board P1 reset), U10 (DS1232) emits a 250mS reset pulse. If the CPU clock (CLKDOG) is not present, then U10 will time out after 500mS and generate another reset pulse (the debug display will flash at a half second interval). RESETIN is fed into the WXGLU1 (U34) pal to distribute the reset as *RESET for the peripherals, *RSTI to the CPU, and *LRESET to the Lattice programmable devices.

It is possible for the CPU to generate a reset on *RESET by asserting *RSTO when the RESET instruction is executed. This is done by the operating system startup to reset all peripherals (approximatly 250mS after RESETIN is deasserted).

During RESETIN assertion, WXGLU1 asserts *CPUMODE to select the internal CPU bus buffer type via diodes D2..D5 and JP11 jumpers (see cpu.sch). Jumpers are not normally installed at JP11, so the CPU starts up with low power buffers for low power consumption.

If the PCI card is not present (*PCIPRESENT deasserted), *CPUBG is always asserted allowing the CPU full access to the bus. If the PCI card is present, then the WXGLU1 pal drives *CPUBG according to *PCICPUBG generated by the PCI card.

For R+D debugging purposes, a jumper may be placed on JP14 to pull ROMSEL low. This will invert the A20 line to the Flash ROMs (ROMA20 = !A20); otherwise ROMA20 follows A20. This allows the two halves of a 29F040 to be swapped in the address map.

Historically, the WFM bus is decoded using address line A25 inverted to become WA25. WXGLU1 inverts A25 to generate *A25.

The 68040-33 CPU internally uses 66.000MHz (PCLK) for its processing, however the external bus operations are at 33.000MHz. WXGLU1 divides the 66.000MHz crystal (X3) output by 2 to generate BCLK which is used as a reference for the PLL buffer chip (U18 CY7B9920-7SC). The PLL buffer chip provides individual low skew clocks for each clocked device on the WX card.

All Lattice devices can be programmed from an external PC by connecting to JP8 (special cable provided by R+D). However, the WXCPUC lattice includes an internal interface which can program all other Lattice and XILINX devices from software. As the main CPU control logic and programming interface is in the WXCPUC Lattice device, this device must be operational at all times and is the only device which cannot be programmed via software. Programming of the Lattice/XILINX devices is serial via the following signals:

*LISPEN	enable Lattice programming (disable XILINX programming)
LMODE	programming mode to Lattice (or enable XILINX XPROG output)
XPROG	active low XILINX program start
LXSDI	serial data to Lattice/XILINXs
LXSDO	serial data from Lattice/XILINXs
XINIT	XILINX ready for data (XILINX initialised)
XDONE	XILINX load complete

The devices are connected as two serial chains (one for XILINXs, other for Lattices) using the SDI and SDO pins on the devices. As the PCI and CG4 cards can be removed, the WXGLU2 pal routes the SDI/SDO signals to keep the chain continuous by observing the *PCIPRESENT and *EXPPRESENT (CG4 present) signals.

Using the Address bus (A[16..31]), and control signals (*TS,TT[0..1],SIZ[0..1]), the WXCPUC lattice provides all address decoding. The 68040 starts a cycle by asserting *TS (Trasnfer Start) and ends without error when *TA (Transfer Acknowledge) is asserted, or with bus error when *TEA (Transfer Error Acknowledge) asserted (i.e. device did not respond). If there are more than 256 BCLK cycles after *TS is asserted and there is no *TA asserted, WXCPUC asserts *TEA to indicate a bus transfer timeout. When *TA is asserted, if *TCI (Transfer Cache Inhibit) is asserted, then the data is not cached, if *TBI (Transfer Burst Inhibit) is asserted, then the device is not able to transfer as a burst (For further information refer to 68040 CPU documentation[1],[2]).

The following are the device selection signals controlled by WXCPUC:

*FROMCE	Flash ROM chip enable
*FROMOE	Flash ROM output enable for reads ($00400000-$007FFFFF)
*CGDTS	CG4 transfer start ($00800000-$0083FFFF)
*WXMIXRTS	Mixer interface transfer start [high speed serial link on ESP-CG4] ($00840000-$0087FFFF)
*RTCCE	RTC and SRAM enable ($00880000-$0088FFFF)
*QSCS	Quad serial chip enable
*QSDS	Quad serial chip data strobe
*QSE	Quad serial chip data enable
*QSDTACK	Quad serial chip data acknowledge ($00890000-$0089FFFF)
*QSIACK	quad serial port interrupt acknowledge ($008A0000-$008AFFFF)
*WXDEBGTS	WXDEBG debug Lattice transfer start ($008F0000-$008FFFFF)
*WFMTS	WFM bus access transfer start ($02000000-$07FFFFFF)
*PCITS	PCI card transfer start ($10000000-$FFFFFFFF)

After reset or if location $008C0000 is accessed, then the flash ROMs also appear at location $00000000. If location $008D0000 is accessed, then the PCI card is enabled at $00000000. Mapping the PCI card is used to initially configure the PCI cards. Once PCI cards have been configured, the flash ROMs are mapped at $00000000.

Internal to WXCPUC the programming interface is decoded as a byte at $008E0003. The bits are allocated as:

$008E0003 read - programming status

bit	0	LXSDO data from Lattice/XILINX
	1	XINIT XILINX initialised
	2	XDONE XILINX programming done
	3	[spare]

write - programming control

bit	0	LXSDI data to Lattice/XILINX
	1	LXSCLK serial data clock
	2	LMODE Lattice mode and *XPROG
	3	LISPEN Lattice enable/ XILINX disable

When the FROM or RTC locations are read, the *OE signal is asserted to enable the data to the CPU data bus. When a write is made to these locations, SIZ[0..1] and A[0..1] are used to assert the appropriate *WE0..3 to enable writing to the correct bytes.

If the bus cycle has TT[0..1] = 112 indicating an interrupt acknowledge cycle, WXCPUC asserts *AVEC with *TA. This causes the CPU to use auto-vectored interrupts (see 68040 documenatation). Vectored interrupts are not used on the WX.

10.2.6.2 CPU

(see 10.4.3 MC68040 CPU schematic)

This schematic includes the CPU and boundary scan TAP PORT. The TAP PORT is used for R+D diagnostics, and at this stage not used in production. The CPU has a heatsink bonded with heat conductive glue. With this heatsink, it is not necessary for any forced air cooling.

The jumpers at JP11 are used to select the buffer mode of the 68040 after reset. All jumpers should be off.

10.2.6.3 Flash ROMs and SRAMs

(see 10.4.4 RTC, RAM and FROM schematic)

The SRAM is organised 8k x 32 bits. The top 24 bits are in normal SRAMs (U22,U12,U23). The bottom 8 bits are inside the RTC chip (U14 DS1643). The top 64 bytes are the real time clock values (held in low 8 data bits). As the RTC has an internal battery, the low 8 bits of this SRAM region is non-volatile. For documentation on the Dallas DS1643 RTC see [4].

The Flash ROMs are organised as 512k x 32 bits (U27,U19,U24,U15). Flash ROMs hold the operating system and all diagnostics. For documentation on Flash ROMs see [3].

JP14 can be shorted to hold ROMSEL low thus inverting A20 to drive ROMA20. This is for R+D development use only, JP14 will not normally be shorted. The ROMA20 line is connected to the WXDEBG Lattice to allow software detection of which half of the Flash ROMs are currently being used.

10.2.6.4 DRAM

(see 10.4.5 DRAM schematic)

The 72 pin DRAM SIMM modules are placed in sockets at U3 and U4, and controlled by the WXDRAM Lattice (U25). The DRAMs are decoded to appear at addresses $08000000-$0FFFFFFF by WXDRAM. The DRAMs can be parity or non-parity types as the WX does not use parity. Normally 4M x 32 bit SIMMs are installed. If there is one SIMM, it must be in socket U3. For PCI machines a 32Meg SIMM is installed at U3 and a terminator is installed at U4.

Every 512 BCLKs (15.3uS) WXDRAM performs a CAS-before-RAS refresh cycle to refresh the DRAMs.

If the CPU asserts SIZ[0..1]=112 (line burst transfer), then WXDRAM will assert RAS and then 4 cycles of CAS to burst 4 x 32bits of data.

The buffers at U20,U21 (74AC245) allow reading of the SIMM DRAM type bits (DS0..7 and DS8..15). These bits appear on D31..16 when the system information is read (*SYSSTAT asserted). This feature is not currently used as most DRAM manufacturers are lazy and do not correctly connect the DRAM type bits. For documentation on SIMM DRAMs see [5].

10.2.6.5 Debugging Interface

(see 10.4.6 Debug Interface schematic)

The WXDEBG Lattice (U11) provides facilities for debugging the WX. The address map is (all locations are bytes):

$008F0003 read - interrupt source

bit	0	100 clock interrupt
	1	quad serial chip interrupt 1
	2	quad serial chip interrupt 2
	3	quad serial chip interrupt 3
	4	PCI interrupt A
	5	PCI interrupt B
	6	PCI interrupt C
	7	PCI interrupt D

write - right 2 7-segment LEDs

$008F0007 read - interrupt enable register

write - interrupt enable register

bit	0	100 Hz clock interrupt enable
	1	quad serial chip interrupt enable
	2	generate software interrupt on level 1
	3	enable read of system information at $008F000C, else DIP switches
	4	[spare]
	5	[spare]
	6	debug decimal point
	7	LASTOBE to JP4

$008F000B read - interrupt source

bit	0	software interrupt
	1	CG4 interrupt
	2	mixer interface interrupt
	3	WFM bus interrupt
	4	non-maskable interrupt (from Q137 front panel P1 NMI)
	5	ROMA20 detect
	6	CG4 present
	7	PCI present

$008F000C read and $008F0007 bit 3 set - read dongle (32bits) (asserts *SYSSTAT)

bit	31..24	U3 SIMM socket status
	23..16	U4 SIMM socket status
	9..8	dongle sequence number
	7..0	dongle code

There are 4 dongle codes, each byte read sequenctially with a different sequence number:

0	pcb revision
1	dongle byte 1
2	dongle byte 2
3	dongle byte 3

$008F000F read and $008F0007 bit 3 clear - read DIP switches
The dip switches are read as a 1 repesenting the ON state of the switch.

$008F000F write - clear 100Hz interrupt request

The 7 Segment displays display CPU operation debug:

Left digit	1	- processor status (PST0..3)
	2	- current interrupt level (*IPL0..2)
	3	- value from $008F0003 write (MSN)
Right digit	4	- value from $008F0003 write (LSN)

The decimal points are allocated as:

Left	1	- 100 Hz interrupt enabled
	2	- quad serial port interrupt enabled
	3	- state of $008F0007 bit 6
Right	4	- interrupt pending (*IPEND)

The display is multiplexed at the rate determined by the 555 clock (U9).

10.2.6.6 Quad Serial Port

(see 10.4.7 Serial Ports schematic)

All four serial ports are on the CS2401 quad serial chip (U13) at base address $00890000. The buffers at U16 and U17 are enabled when ever the CS2401 is accessed to control when data appears on the CPU bus as the CS2401 is a slow chip.

X2 (20MHz crystal) provides the clock for the internal operation of the quad serial chip, and the serial data transfer. The four ports are converted to RS232 levels via U5,U6,U7,U8 (all MAX232ECWE).

For documentation on the CD2401 quad serial port see [8].

10.2.6.7 WFM Bus Interface

(see 10.4.8 WFM Bus Interface schematic)

The WFM bus interface is controlled by the XILINX at U26 (XC3042A-6-TQ144). This device is loaded when the ROM starts and provides the following facilities:

1. WFM bus control
   Decoded as addresses $02000000-$05FFFFFF.

2. 100Hz clock generation (OSCLK) from X20M signal.

This XILINX operates as the master WFM bus controller providing the WFM bus refresh (*LWREF), slice clock (LSCLK) and slice taken by WX signal (*LTSOUT). The PCI WFM bus interface XILINX connects to the local bus signals (LWA0..25, LWD0..15, *LWUDS, *LWLDS, *LWWR) and arbitrates with the WX XILINX for the WFM bus. The PCI WFM bus XILINX is synchronised to the WX WFM bus XILINX by a 33nS pulse at the start of each WFM bus cycle (SCLKO).

10.2.6.8 Expansion Bus Connectors

(see 10.4.9 Expansion Bus Connector schematic)

The expansion bus connectors JP5 and JP9 are where the ESP-CG4 card is connected to the ESP-WX. These connectors can also be used for connection to a logic analyser and provide access to all useful CPU signals.

Any card connected to JP5,9 holds *EXPRESENT low indicating the presence of the card. This is reported as $008F000B bit 6 asserted in the WXDEBG Lattice.

10.2.6.9 ESP-PCI Connectors

(see 10.4.10 Edge Connectors to ESPPCI schematic)

Connectors CN1 and CN2 are for connection of the ESP-PCI card. The presence of the card is detected by *PCIPRESENT being held low by the ESP-PCI PCB.

CN1 has connections to the complete CPU bus and is used by the CPU access the PCI bus. CN2 connects to the local WFM bus interface and is used by the PCI cards access the WFM bus.

10.2.6.10 Digital Edge Connector

(see 10.4.11 Digital Edge Connector schematic)

If the WX is in the TS slot all JP13 jumpers must be installed, if in the WS slot all JP13 jumpers must be removed or hardware damage may occur.

10.3 ESPWX Field Diagnostics

The ROMs supplied with the ESP-WX include low level diagnostics to check hardware operation, debugger provided by Microware, a WX version of the KMON diagnostics by Fairlight, and the facilities for booting the operating system.

There are 8 DIP switches which are used during diagnostics and selection of the operating system boot mode. For normal operation, all DIP switches should be OFF. After reset, the DIP switches are read to select the boot mode as below:

DIP switch

8	enable ROM diagnostics
7	spare
6	spare
5	Rev 14: Disable PCI BIOS Rev 15: Disable synchronous SCSI
4	disable copyback caching
3	disable MMU
2	disable CG4, use serial port
1	enable ROM debugger

If DIP switch 8 is on when the system is reset or powered-on, the ROM starts executing the low level diagnostics. It is assumed that only the WXCPUC and WXDEBG lattice are loaded and operational. Once started, the only way to exit the diagnostics is to reset the WX with DIP switch 8 off.

During operation, the right two LED displays show the progress. The first of these digits shows the current test number, and the other displays the progress.

Test values

1	Cache Push test
2	Dongle test
3	Static RAM test
4	Dynamic RAM test
5	Realtime clock test
6	[unused spare]
7	Xilinx loading test
8	100Hz timer test
9	WFM bus access test
A	WFM bus interrupt test
B	QUAD serial port test
C	serial receive/transmit test

Test progress values

1	started test
B	error detected, test still running
F	test completed with error
0	test completed without error

After each test the card pauses until the state of DIP switch 1 is changed, then procedes to the next test. If DIP switch 2 is ON then the diagnostics will run the last test again when DIP switch 1 is changed.

10.3.1 Cache Push test

The diagnostic assumes failure then executes the CPUSH (cache push) instruction. If this fails then the failed condition will still be displayed on the LEDs and the card will hang until reset. Otherwise, the success code is displayed.

10.3.2 Dongle test

The dongle is enabled within the WXCPUC lattice and the 4 dongle byte sequence is read twice. The two sequences are checked to be the same and that data bits 8..9 count correctly. Then the dongle is disabled in WXCPUC lattice.

10.3.3 SRAM test

The SRAMs are tested by writing a walking address pattern and checked after each write. If there is an error, the LASTROBE pin is strobed (for tracing on a logic analyser) and the error detected code is displayed.

10.3.4 DRAM test

The DRAMs are tested by writing a walking address pattern and checked after each write. If there is an error, the LASTROBE pin is strobed (for tracing on a logic analyser) and the error detected code is displayed. Only the first 8M is tested.

10.3.5 Realtime clock (RTC) test

The RTC seconds are read and the test waits for 1.5s and ensures that the seconds have changed.

All subsequent tests assume that the Static RAM is operational.

10.3.6 XILINX load

The Xilinx is loaded with the standard Xilinx code. If the test fails quickly then the XINIT signal was not detected to go low. If the test fails after about 3 seconds then the XDONE signal did not go high at the end of loading.

All subsequent tests assume the Xilinx has loaded correctly.

10.3.7 OSCLK test

The 100Hz clock is tested by clearing the clock request and ensuring no clock request is pending. Then the test waits 20mS and checks that there is now a clock request pending.

All subsequent tests assume that an operational ESP-SYN card is installed.

10.3.8 WFM BUS ACCESS TEST

The diagnostic does a walking address memory test on the SC shared memory and verifies each value after it is written, and strobes LASTROBE on error.

10.3.8.1 WFM BUS INTERRUPT TEST

The diagnostic writes to the SC to assert the WBINT interrupt signal and checks that it is asserted. Then it writes to the SC to deassert then WBINT interrupt signal and checks that it is deasserted.

10.3.8.2 QUAD SERIAL PORT TEST

All values $0000..$FFFF are written to a word location in the CS2401 quad serial chip and verified. LASTROBE is pulsed on error.

10.3.8.3 SERIAL PORT TEST

The quad serial port is initialised; then the right LED digit is changed to '2'. Then 'U' is continuously transmitted on the RS232 port and the COMMS port. If a character is received on either port then it is displayed on the LED digits.

10.3.8.4 MICROWARE DEBUGGER

If DIP switch 1 is on when the system powers-up or is reset, the Microware debugger is entered. This debugger provides extensive utilities as described in OS-9 ROM DEBUGGER USER'S MANUAL.

Note that the DRAM and quad serial port must be operational to use this debugger.

10.3.8.5 FAIRLIGHT KMON DIAGNOSTICS

Once in the Microware debugger, if g diag is executed, the KMON diagnostics similar to the WS are started. Refer to the KMON diagnostics documentation for usage [9].

10.3.8.6 NORMAL STARTUP

If all DIP switches are off, the ROM will startup and display a list of command options to boot the WX to the operating system.

This is the only form of startup where interrupts are enabled.

10.3.8.7 7-SEGMENT LED BOOT PROGRESS CODES

As the ROM starts up the Microware debugger or the normal startup, the LED displays show the progress for tracing errors during booting. If the system fails, one of the codes below will remain on the right two digits showing the last successful operation:

00	System reset (ROM faulty)
01	initialisation entry
02	initialisation complete
03	vector tables built in DRAM
04	initialise data in DRAM entry
05	initialise data in DRAM exit
06	code correctly compiled for 68040
07	about to use address trap to detect CPU type
08	address trap returned ok
09	start of CPU type detection
0A	did not detect 68040 (ERROR)
0B	end cpu detection, detected 68040
0C	enter debugger initialisation
0D	exit debugger initialisation
0E	initialise quad serial chip
0F	print first CR and LF
10	print first signon string,or DRAM missing
11	exit print signon string
12	bus error (ERROR)
13	check whether to use debugger
14	enter debugger
15	exit from debugger (ERROR)

The following are quad serial progress messages:

81	waiting for chip reset during initialisation
82	reset complete
83	exit port initilalisation
84	initialise COMMS port
85	check for character on COMMS port
86	exit check for received character
87	output character
88	output character to COMMS port
89	exit output character routine [also displays received character onm 7-segment LEDs]
8A	wait for character
8B	initialise serial ports
8C	enter quad serial port check for status
8D	exit quad serial port status check

After performing the initial diagnostics with the dip switches the following will be seen on the monitor when system restarted:

```
***  ATTENTION  ***

NVRAM  was  found  corrupted  -  reconfiguration  is  forced.

Do  you  want  to  use  the  recommended  NVRAM  configuration  ?  (Y/N)
```

Answer "n" to configure the NVRAM and the following will be on the screen:

```
Boot   Drivers   Available:-

A:  Boot  from  PCI  SCSI  Disk  Drive

B:  Boot  from  Turbo  SCSI  Disk  Drive

C:  Display  Devices  on  PCI  SCSI

D:  Display  Devices  on  Turbo  SCSI

E:  Boot  From  Flash  ROM

F:  Enter  KMON30  on  the  Sync  Card

G:   Enter   Diagnostics
```

The priority and SCSI target of these boot drivers can be set below.

This priority determines the order of the boot sequence.

e.g. Enter A0 to boot from driver 'A' SCSI target 0

A3 to boot from driver 'A' SCSI target 3

B5 to boot from driver 'B' SCSI target 5

If no data is entered here then the Turbo SCSI will be scanned from target 0 thru target 6. Then, if it is present, the PCI SCSI will be scanned from target 0 thru target 6. The first drive located will be booted from.

Enter a blank line to finish configuration:

```
01:>
```

At this point type the following at the prompt to perform a full configuration:

```
01:>  d

02:>  b0

03:>  b1
```

```
04:>  b2

05:>  b3

06:>  b4

07:>  b5

08:>  b6

09:>
```

At this point press return and the following should be displayed on screen:

```
Boot order will be set to ...

01: Display Devices on Turbo SCSI     Target:0

02: Boot from Turbo SCSI Disk Drive  Target:0

03: Boot from Turbo SCSI Disk Drive  Target:1

04: Boot from Turbo SCSI Disk Drive  Target:2

05: Boot from Turbo SCSI Disk Drive  Target:3

06: Boot from Turbo SCSI Disk Drive  Target:4

07: Boot from Turbo SCSI Disk Drive  Target:5

08: Boot from Turbo SCSI Disk Drive  Target:6
```

Press return through all of these :

```
ROM Debug Level                                (000 .. 009) [000] >

TURBO SCSI Initiator ID                        (000 .. 007) [007] >

IOPACK Lines 0=46 1=34                         (000 .. 001) [000] >

Seconds Till Autoboot                          (000 .. 005) [003] >

SCSI Reset Delay in 10ths/Second              (000 .. 100) [010] >

Enable MFX3 Logo on Startup                    (000 .. 001) [001] >

NVRAM configuration is complete ... System will now restart ... 3 2 1

Exception Error, vector offset $0008 addr $00000000
```

At this point the system should boot as per the following:

```
Fatal System Error; rebooting system

OS-9/68040  System  Bootstrap

Transfering DIO Detection Program to SyncCard.

Transfer OK - Attempting to Run Code at 0x00008000.
```

```
DIO  Detection  Program  is  Running.

Waiting  for  DIO  'INIT'  Pattern  ...  OK

DIO  #0  Present:YES  -  Analog  In:YES  -  Digital  In:YES

DIO  #1  Present:NO

DIO  #2  Present:NO

DIO  #3  Present:NO

DIO  #4  Present:NO

DIO  #5  Present:NO

Fairlight  ESP  Waveform  Executive  Flashware  -  v4.03

      Waveform  Bus  Present:  Yes            Compile  Date:  Mar  9  1998

      Turbo  SCSI  Present:  Yes              Compile  Time:  15:58:06

      CG4  Present:  Yes                      ROM  Debug  Level:  OFF

      PCI  Present:  No                       IOPACK  Setup:  46  Lines

      Sync  Card  Present:  Yes               Machine  ID:  0997  (02)

      Digital  Channel  Cards:  0

      DIO  Cards  Installed:  0

      DIO  Cards  with  Inputs:  0

      DIO  Cards  with  Analog  Inputs:  0

DIP  Switch  Settings

      Enable  System  Debugger  #1:  No       Disable  PCI  BIOS  #5:  No

      Enable  Serial  Output  Only  #2:  Yes   Old  CG4  Xilinx  Enable  #6:  No

      Disable  MMU  #3:  Yes                  Development  Environment  #7:  No

       Disable  Copyback  #4:  No             Enter  ROM  Diagnostics  #8:  No

Sync  Card  Hardware

      Firmware  Revision:  9.05               Xilinx  Loaded:  Yes

      SYS  Duart  Present:  Yes               FPU  Present:  Yes

Sync  I/O  Module  Hardware

      SONY  Duart  Present:  Yes              MFX  Duart  Present:  Yes

      MDR  Duart  Present:  Yes               MIDI  A/B  Duart  Present:  Yes

      MIDI  C/D  Duart  Present:  Yes
```

```
OS-9/68040 System Bootstrap [32 Mb]

Press <DEL> to Start or Any Other Key to Display Boot Menu ... 3 2 1 Autobooting

Scanning Turbo SCSI for Devices

ID -     DEVICE TYPE     VENDOR    PRODUCT             FIRM CAPACITY SECT    MB

00 -       Fixed Disk     FUJITSU   M2694ES-512         811A 00204da0   512 1033

Hardware Does Not Exist For PCI SCSI Boot

Attempting Turbo SCSI Disk Boot to Drive 0

Detected an RBF Formatted Disk.

A valid OS-9 bootfile was found.

Setting Default Device to SCSI id 0

Waveform Executive Startup File - v1.14 .........

Loading and Installing OS9 System Modules ........

Setting Lines Per Page to 25 - [TERM=xterm] ......

Loading and Installing Fairlight System Modules ..

flight: v2.03 - Fairlight OS9 Extensions

Starting RAM Resident IOPACK .....................

Starting QSYS and TVT Drivers ....................

Starting QSYS Applications .......................

Creating Temporary Directory (/dd/TMP) ...........

Attaching Devices (/tomfx and /frommfx) ..........

Starting ESP Message System ......................

ESP Messages Version 1.10

Starting MFX Console Daemon ......................

Starting DFN .....................................

Checking Machine ID ..............................

================================================

              Machine ID:0997 [GAL]

          Fairlight ESP Pty Ltd - Production No. 3

     Channels:24          EQ:YES              TimeFX:YES

     Editing:YES          NinePin:YES         Printing:YES
```

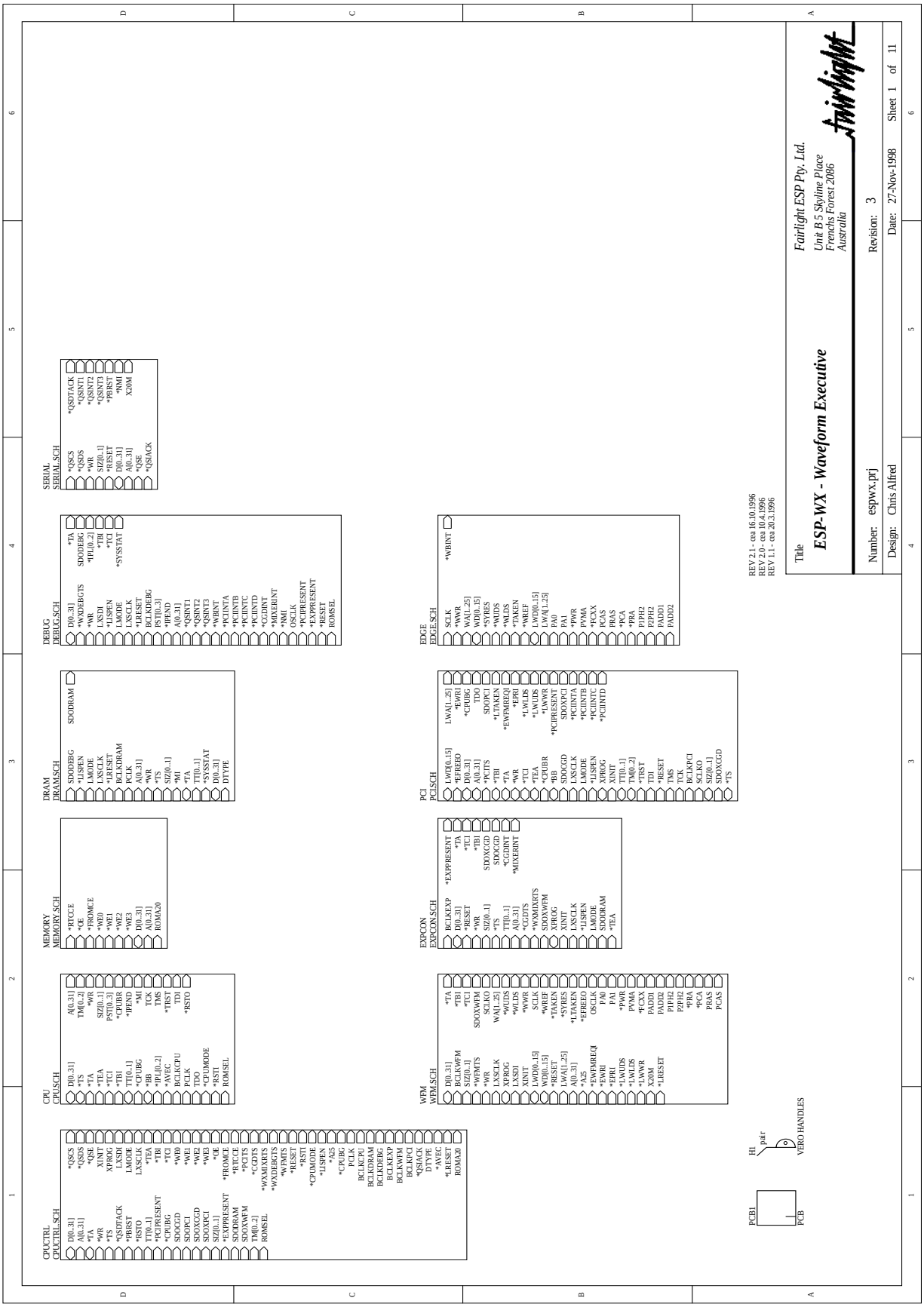
```
      Fame:YES        AudioBase:YES   OMF:NO

      Wide-Words:NO   CD-Writer:NO    Preview:NO

      Waveframe   NO    Multi-Out:YES

 ================================================

 Starting  Media  Daemon  and  Disk  Cache  ............

 Starting    Session    ..............................
```

10.3.8.8 Additional References

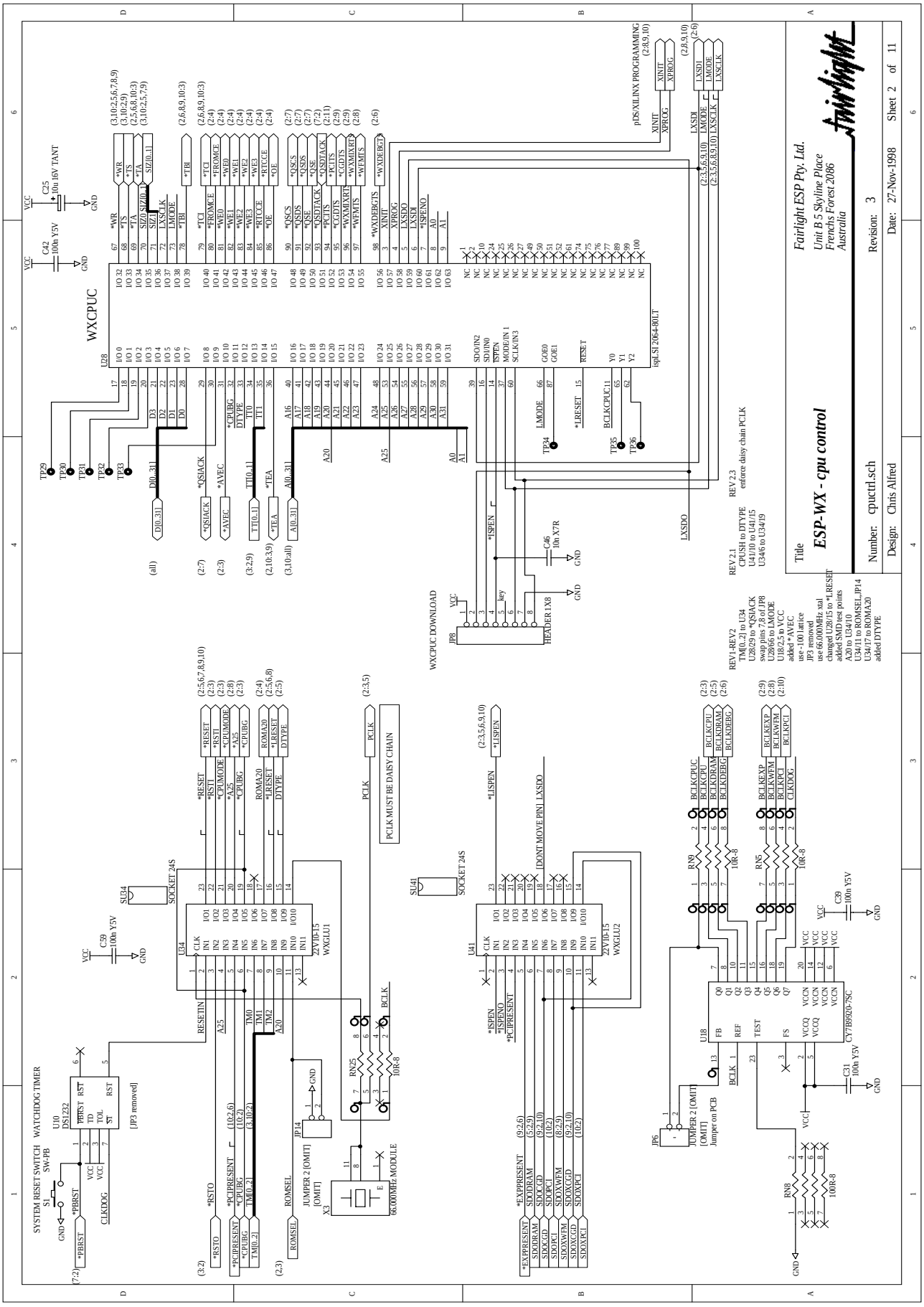
[1] Chris Alfred, Motorola MC68040 operation, Failrlight ESP.
[2] Motorola, MC68040 32 bit Microprocessor User's Manual.
[3] Advanced Micro Devices, Flash Memory Products 1994/95 Data Book/Handbook.
[4] Dallas Semiconductor, 1992/1993 Product Data book.
[5] Micron Technology, 1995 DRAM Data Book.
[6] Lattice Semiconductor, Lattice Data Book 1994.
[7] Xilinx, The Programmable Logic Data Book 1994.
[8] Cirrus Logic, CL-CD2400/CD2401 Data Book August 1993.
[9] Fairlight ESP, CDIAG v3.0.

10.4 ESPWX SCHEMATICS

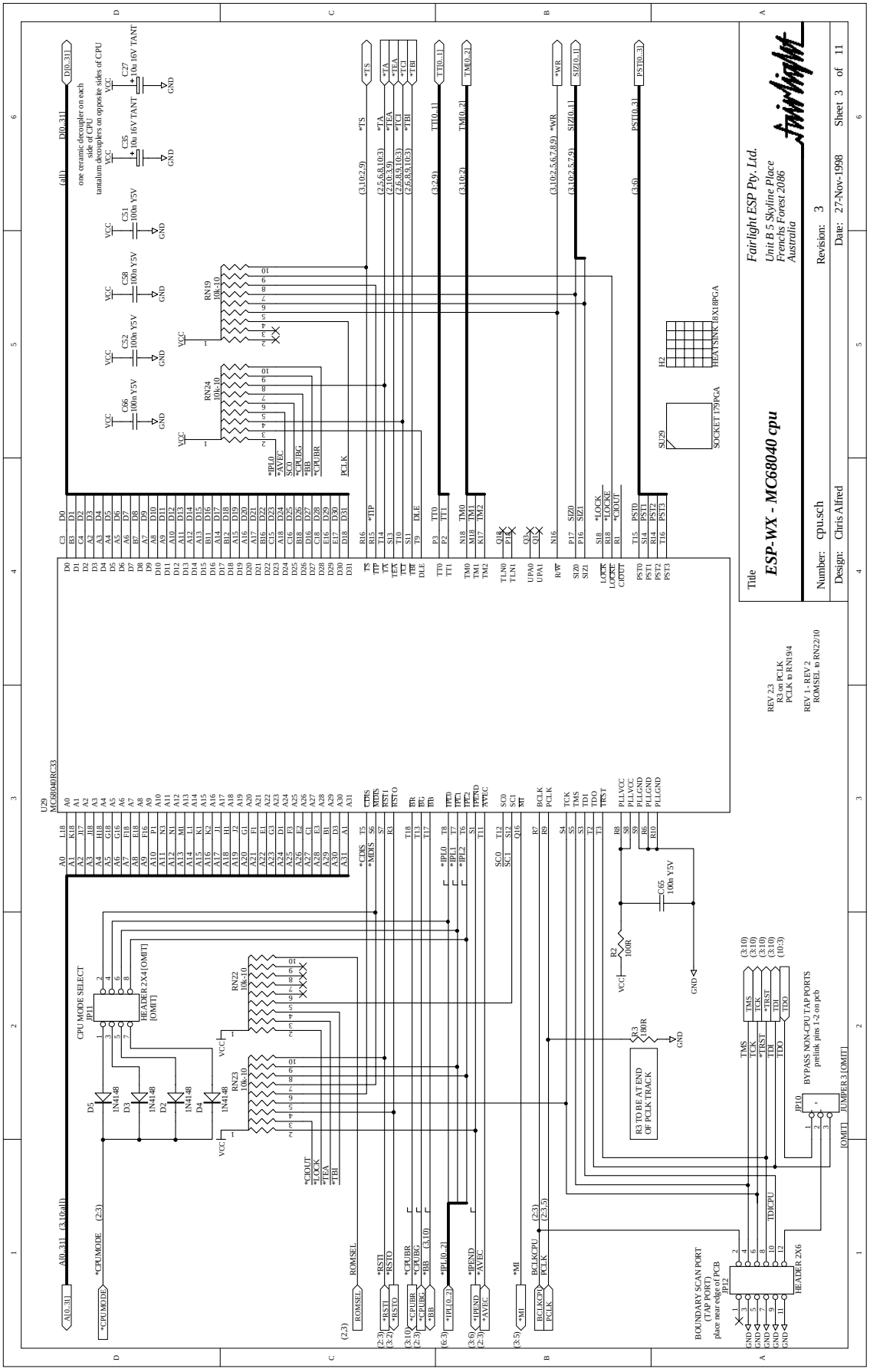
10.4.1 ESPWX INTERCONNECTING DIAGRAM



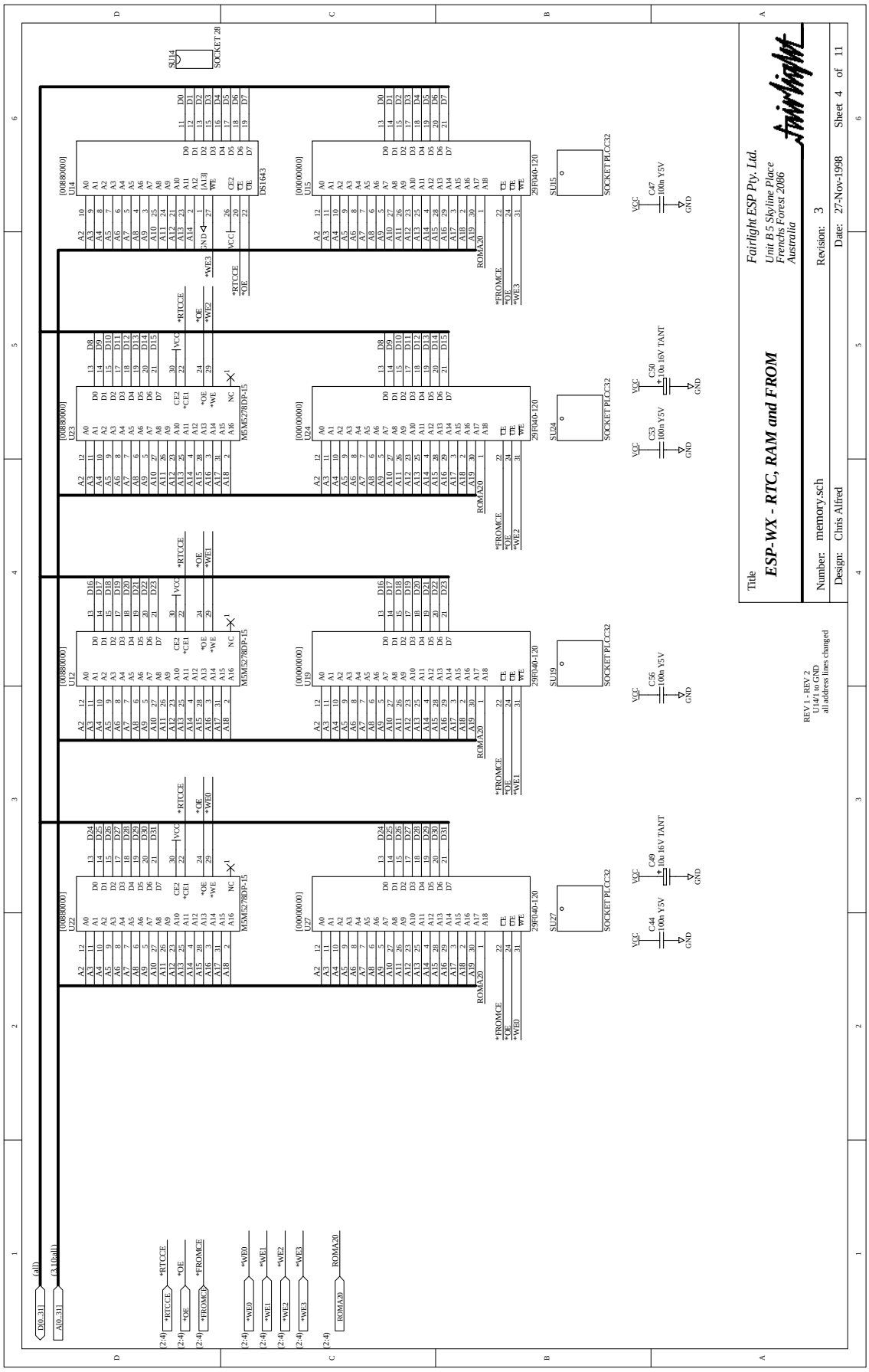
10.4.2 CPU CONTROL



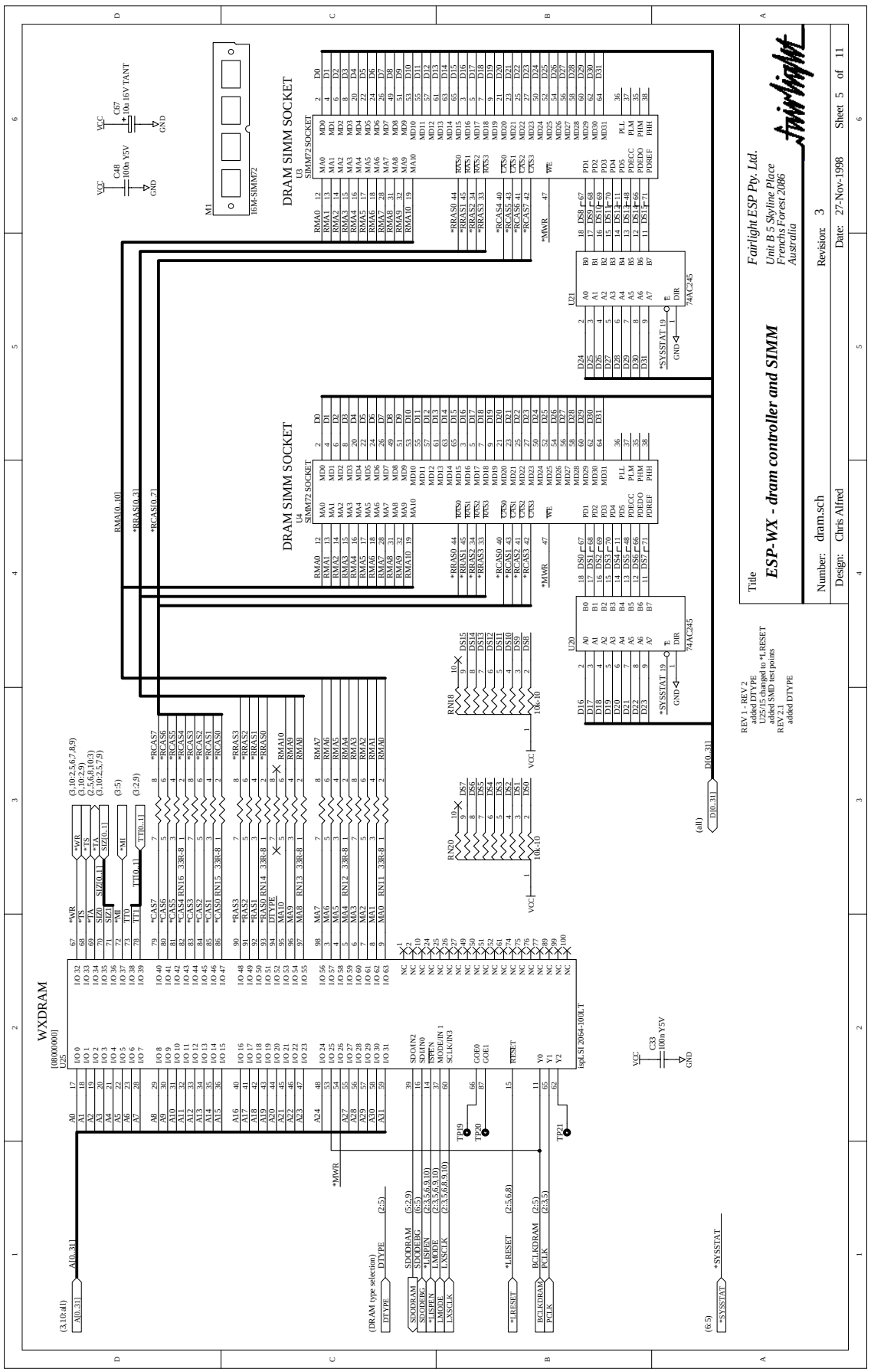
10.4.3 MC68040 CPU



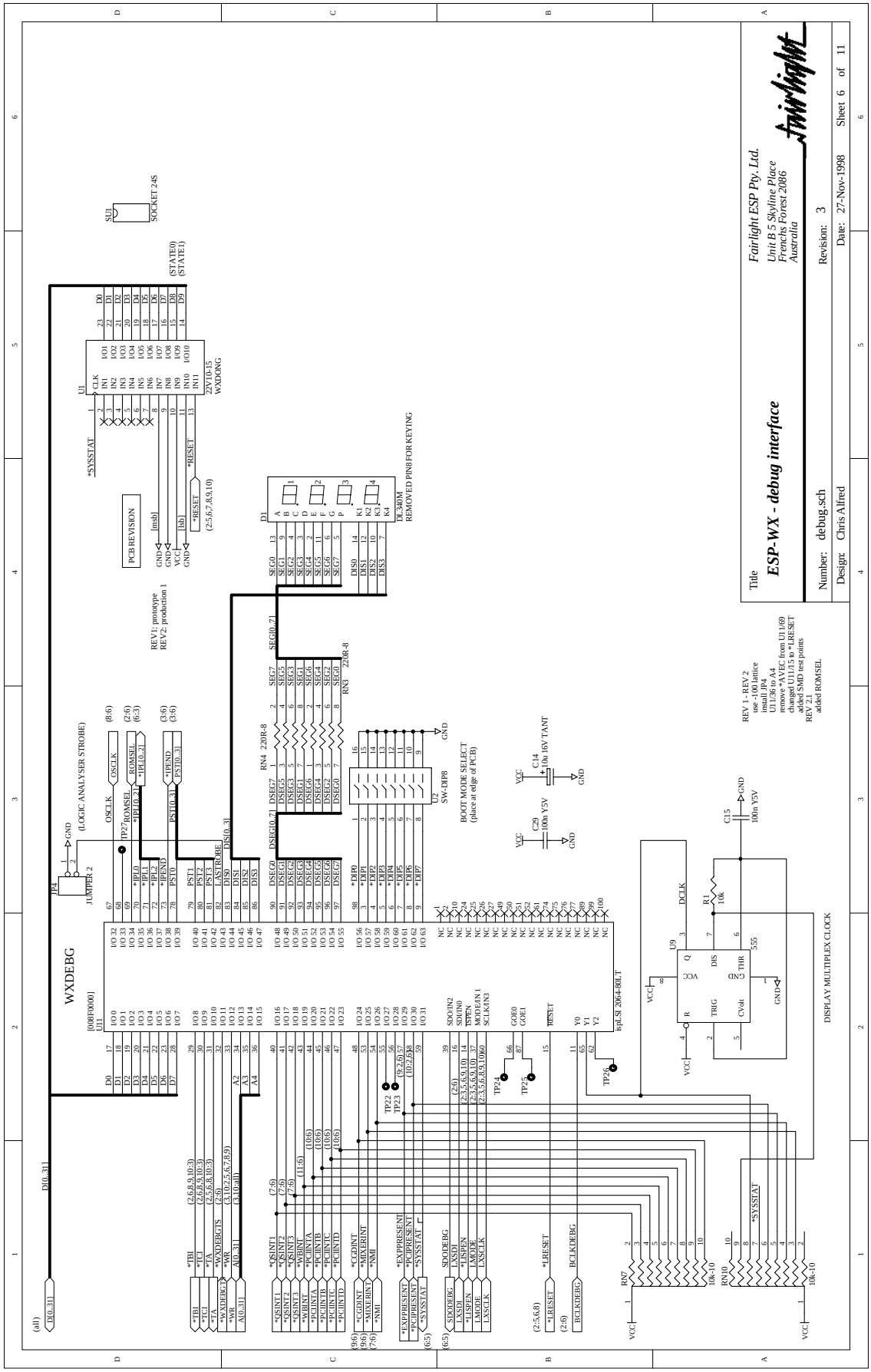
10.4.4 RTC, RAM AND FROM



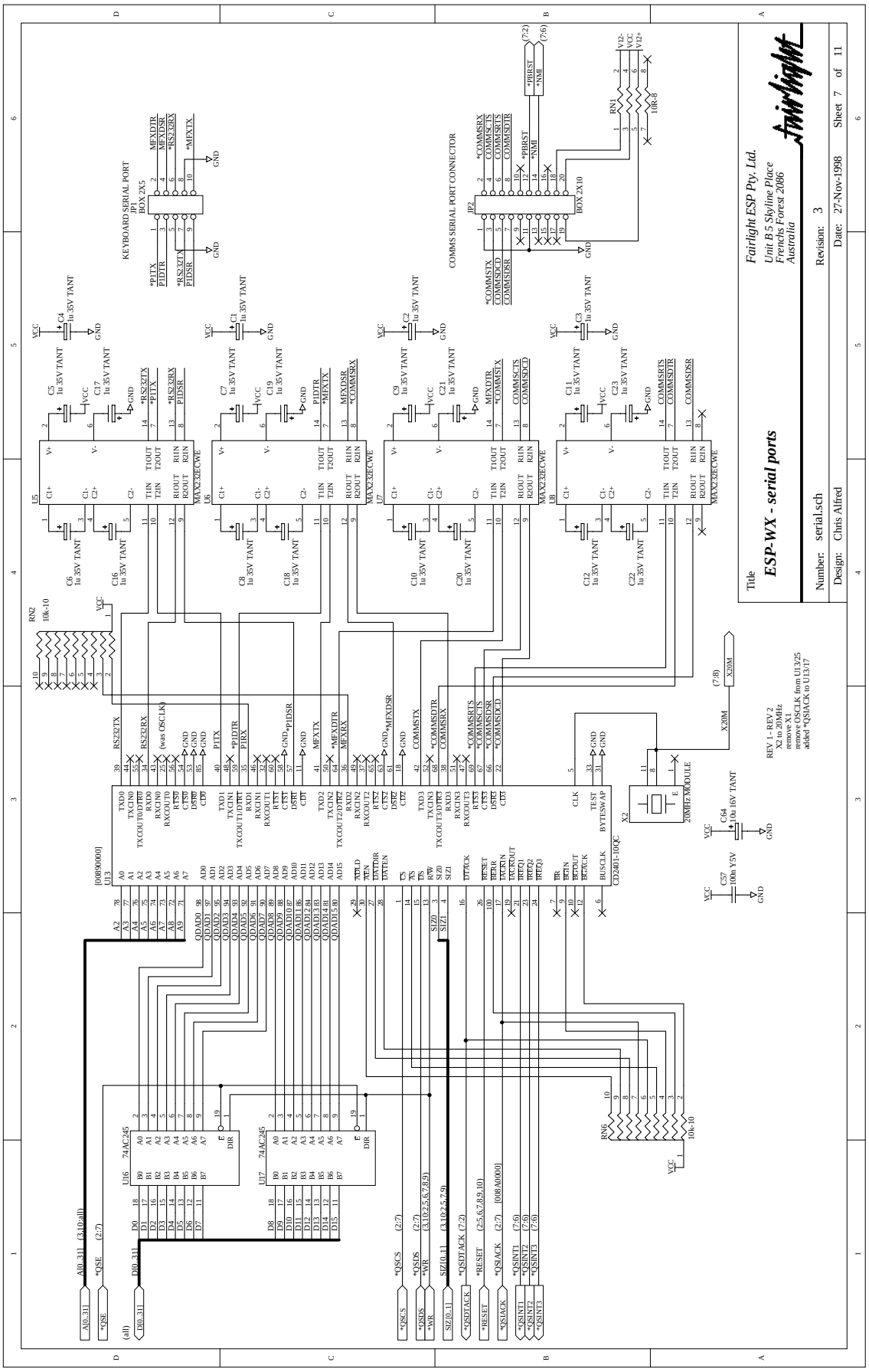
10.4.5 DRAM Controller and SIMM



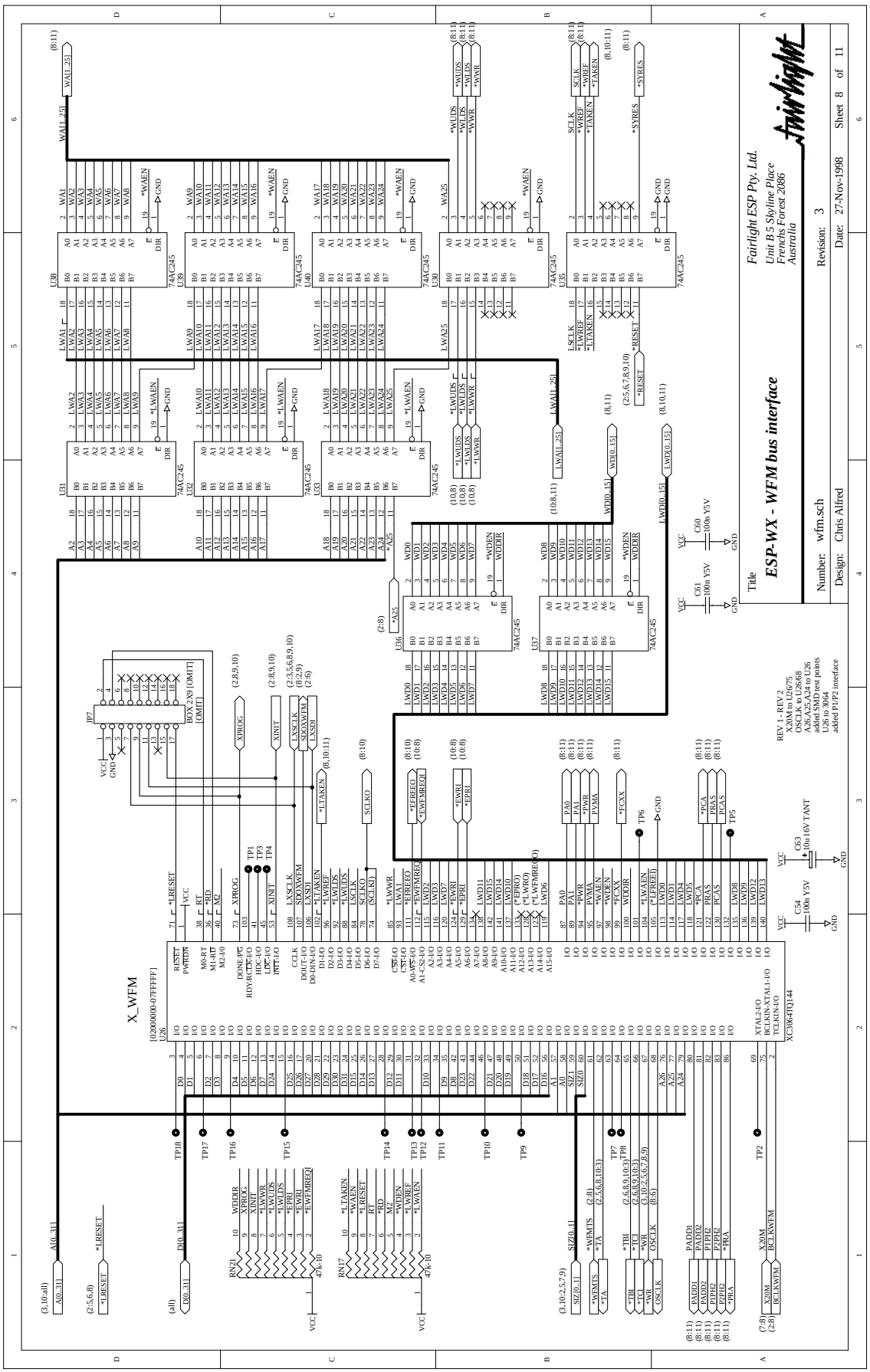
10.4.6 DEBUG INTERFACE



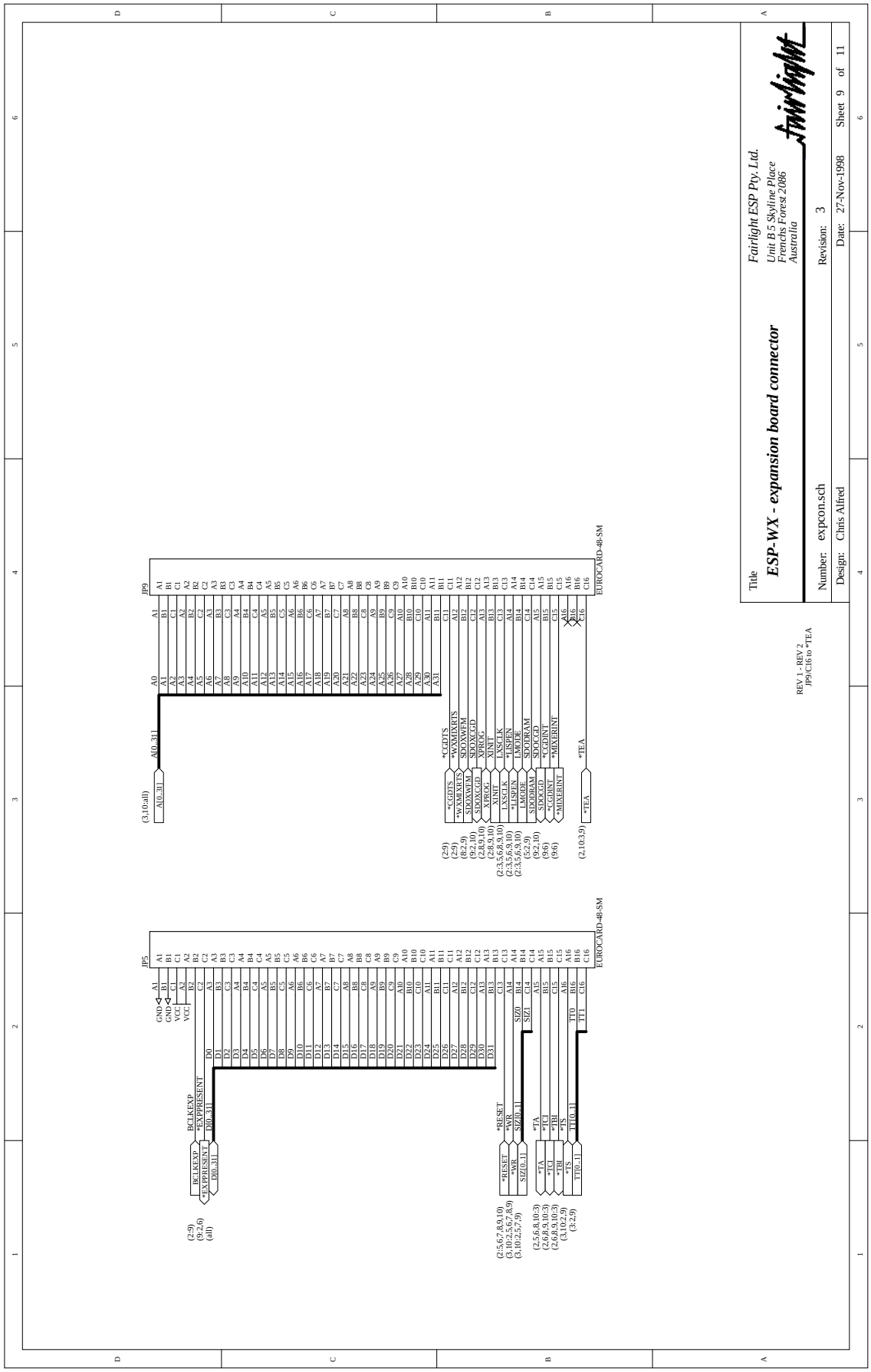
10.4.7 Serial Ports



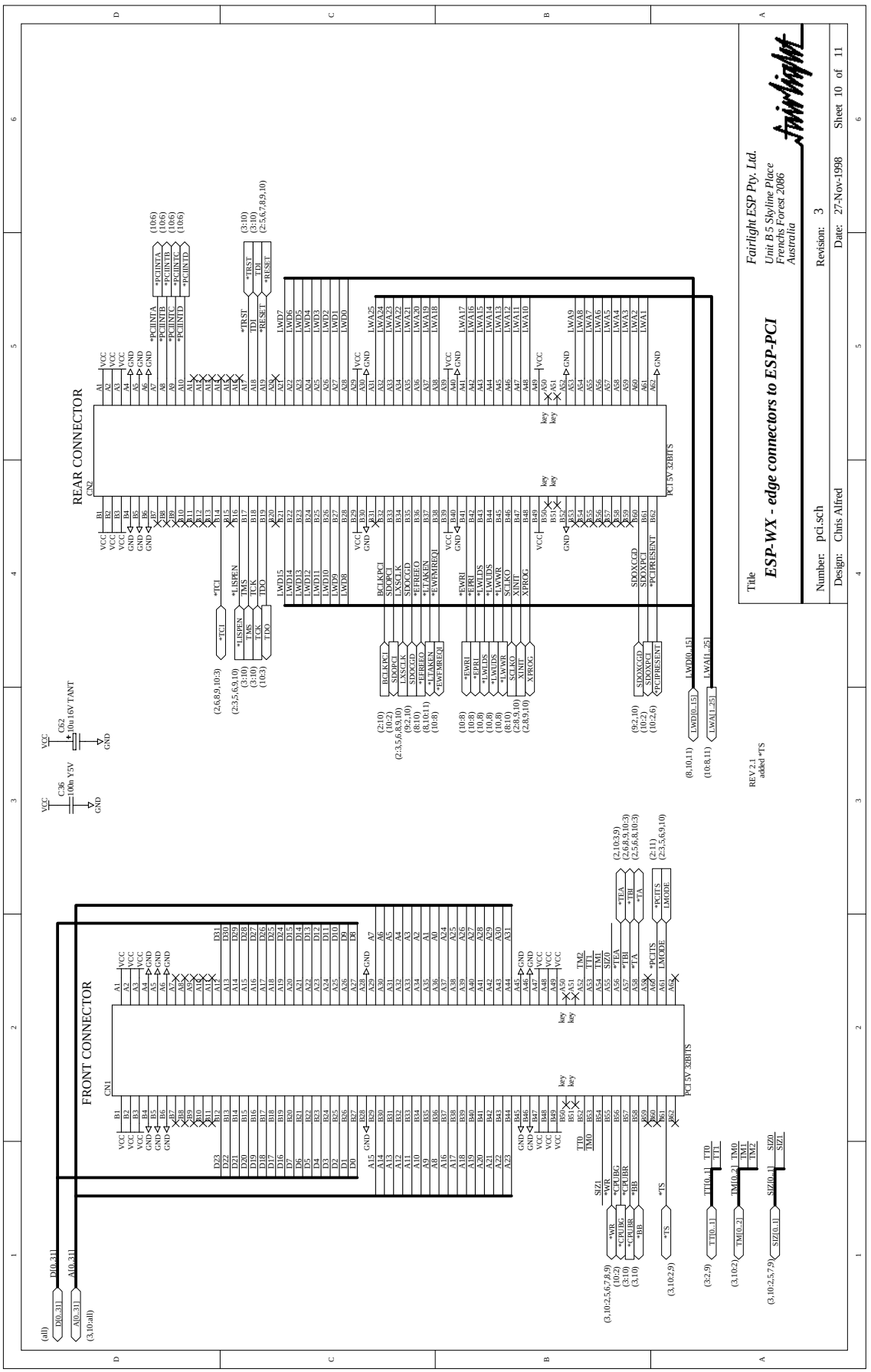
10.4.8 WFM Bus Interface



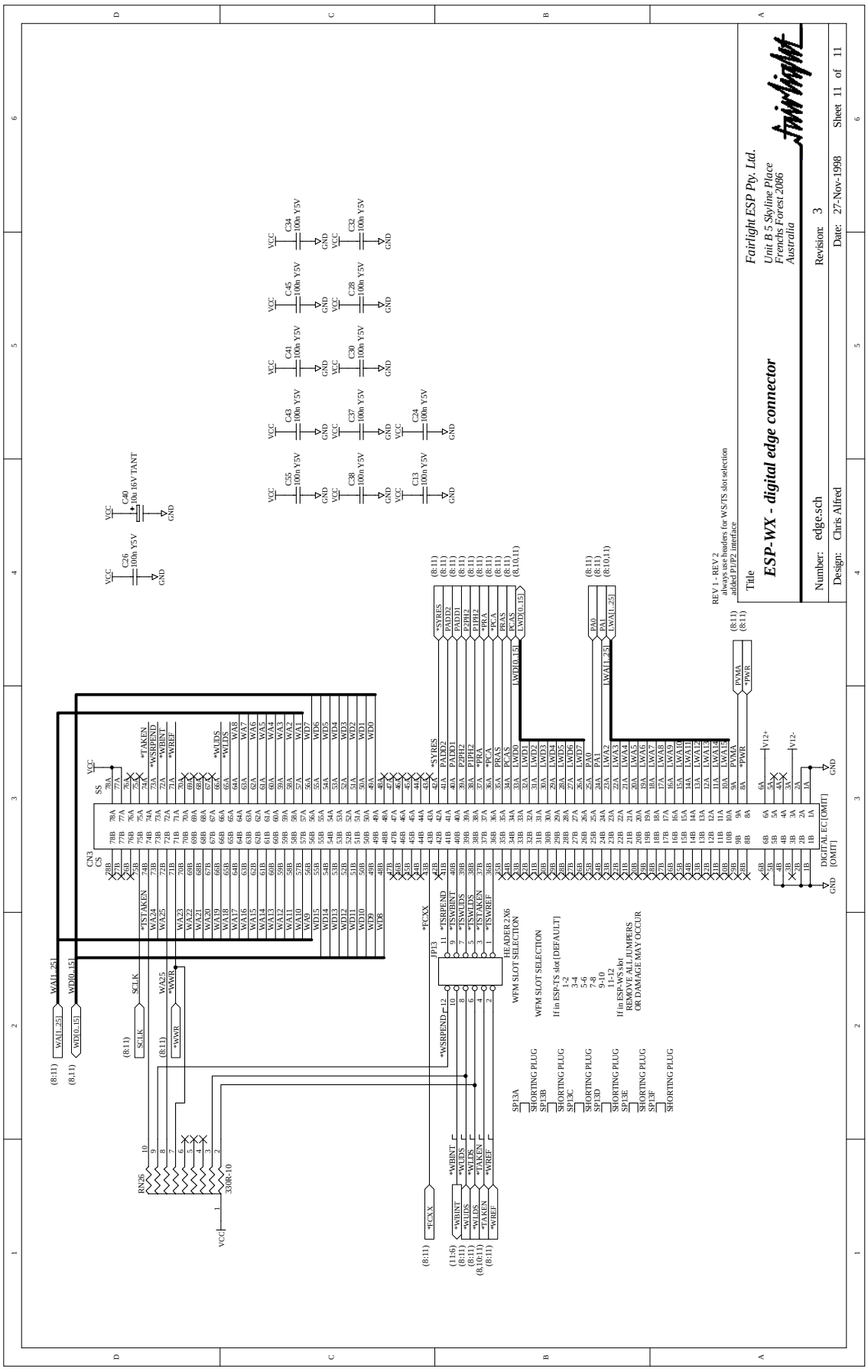
10.4.9 Expansion Board Connector



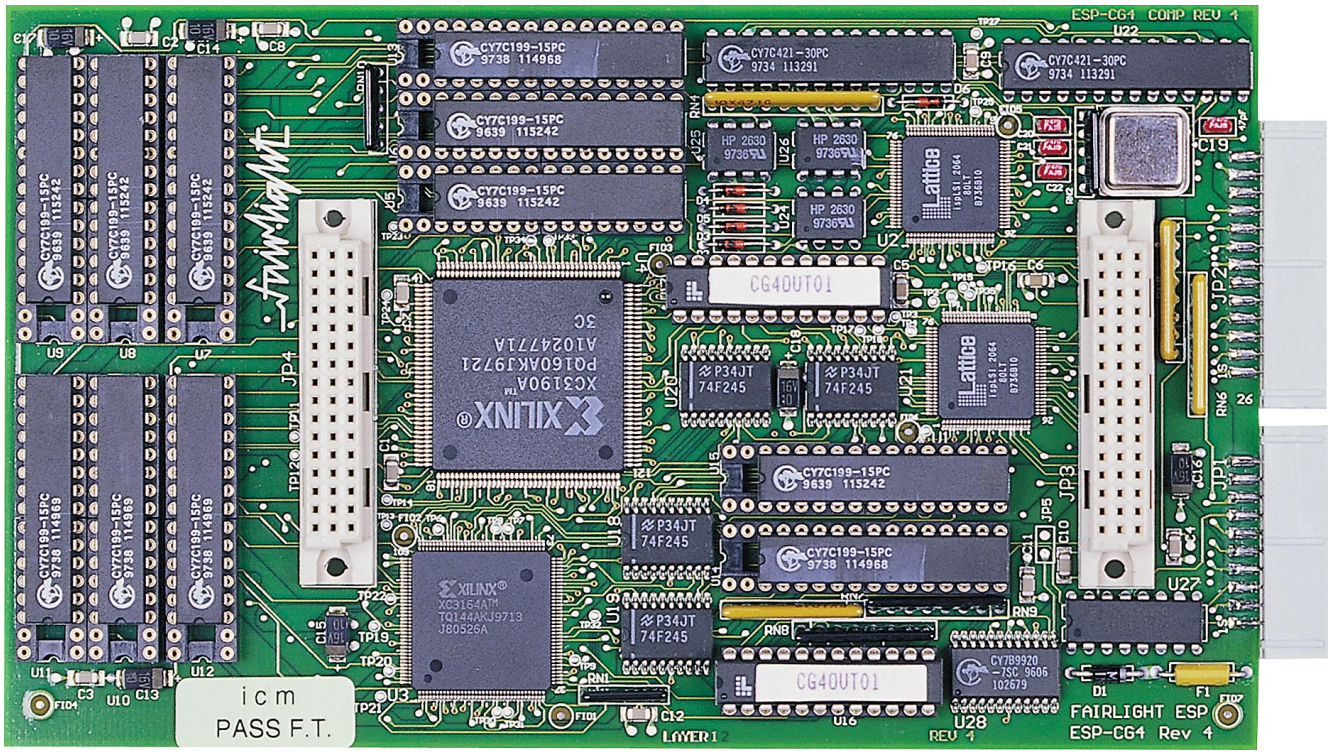
10.4.10 EDGE CONNECTORS TO ESPPCI



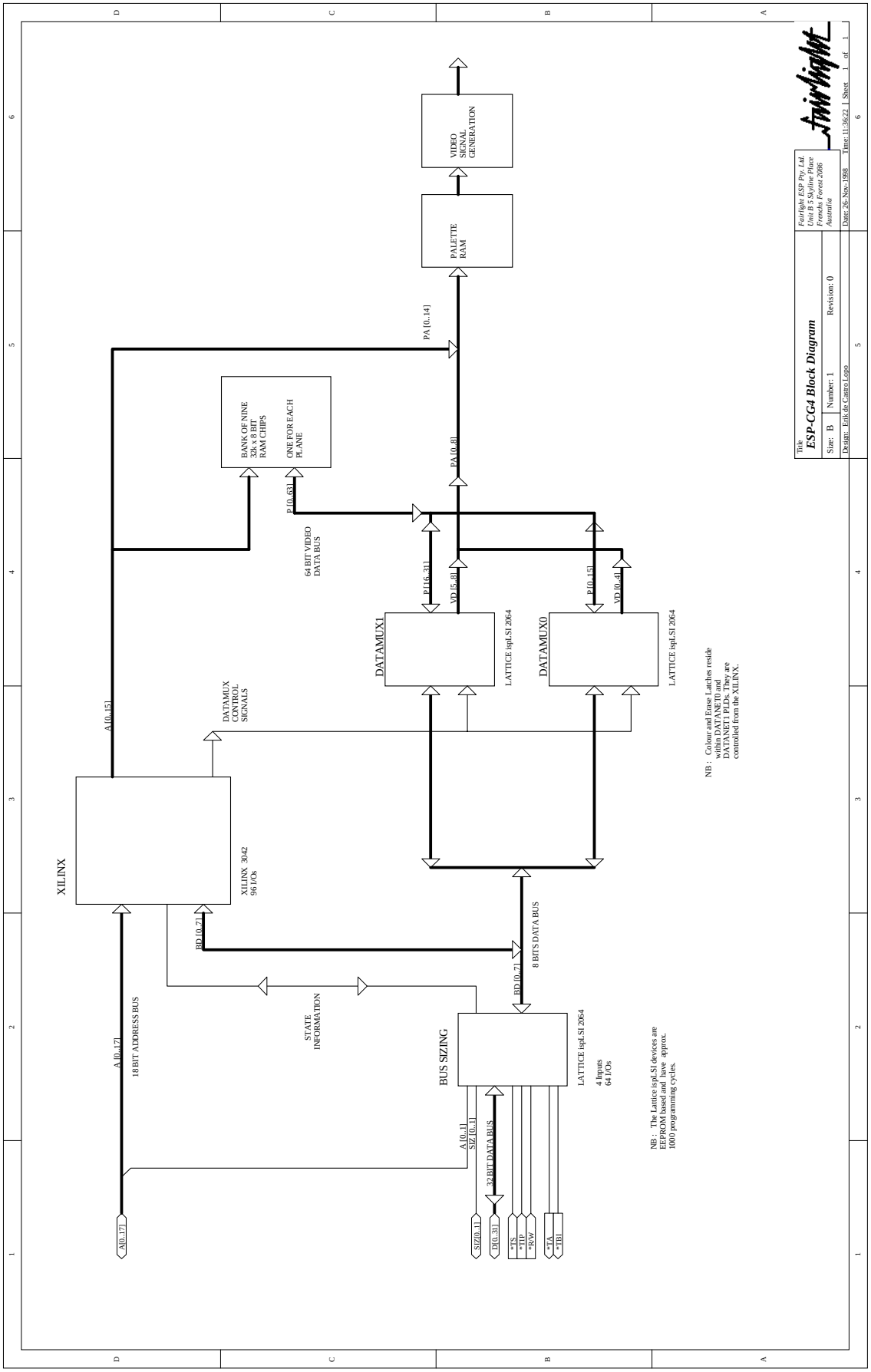
10.4.11 DIGITAL EDGE CONNECTOR



11.0 ESPCG4 Color Graphics Card



11.1 ESPCG4 Block Diagram



11.2 ESPCG4 Circuit Description

11.2.1 Document Revision

11.12.1996 v1.0 ecl: created

11.2.2 Terminology

SRAM	Static RAM
VRAM	Static RAM used for video data
PRAM	Static RAM used for palette data
WX	ESP-WX Waveform Executive
CG4	ESP-CG4 Graphics Card
HSSL	High Speed Serial Link for Amek console
OS	Operating System (OS9 for 68xxx)
FPGA	Field Programmable Gate Array

11.2.3 Introduction

The CG4 graphics card is designed specifically to operate with the WX but also to be software compatible with the ESP-CG3 graphics card. Included on the CG4 PCB is a HSSL for interfacing with the Amek mixing console. The use of programmable devices in the design allows the CG4 to be 99% software compatible with CG3 initially but also to allow later modifications to the existing hardware by changing the configuration data loaded into the two Xilinx devices. Expected enhancements include the addition of a third scrolling VRAM plane and the conversion of the 6 bit TTL colour video output to 12 bit colour, doubling the number of colours which may be displayed.

11.2.4 Installation

The CG4 connectors JP3 and JP4 plug onto connectors JP5 and JP9 of the WX respectively, with the CG4 components towards the WX card. JP1 is a 20 way IDC for connecting the video output to the ESP-RGB board, while JP2 is a 26 way connector for the HSSL.

11.2.5 General overview

All circuitry on the CG4 operates from two clocks. The 33MHz system clock is obtained from the WX via JP3 and buffered by the clock buffer chip U28. This clock drives all the graphics oriented hardware while a 20MHz crystal module, X1, clocks the HSSL circuitry.

The rest of the CG4 can be considered as six main functional blocks. The bus sizing block multiplexes the WX 32bit CPU bus onto the 8 bit CG4 local bus. The address control logic block multiplexes addresses from the WX CPU with internally generated video address lines to enable addressing of both the VRAM and PRAM as well as generating all video timing signals. The data multiplexer multiplexes the 8 bit CG4 local data bus onto the 72 bit VRAM address bus and combines the 9 video plane data streams to generate an 8 bit per pixel video data bus which feeds the video output block, which feeds the 8bit per pixel video bus through the palette SRAMs to generate a 12bit TTL colour signal. The last two blocks contain the video SRAM and the HSSL interface.

11.2.6 Theory of Operation (Graphics)

The CG4 is a highly specialised video graphics engine with a number of features to allow certain types of images to be displayed more efficiently than on a generic PC type graphics card. In particular CG4 has dedicated hardware to efficiently generate horizontal, vertical and 45 degree angle lines from software as well as allowing horizontal scrolling areas within static areas. These features are used extensively within the MFX3 disk recorder application.

Most of the complicated logic required to implement the CG4 is contained within two high density FPGA devices; the address control Xilinx (ADDX) and the data multiplexer Xilinx (DATAX). These devices store their configuration data internal to the device using SRAM which must be reloaded after each power up via signals XPROG, XINIT, LXSCLK, SD0XWFM and SD0XCGD from the WX. This operation is performed automatically by the CPU during the OS booting sequence, with the configuration file stored on the Flash ROMs of the WX or on the MFX3 hard drive. It is therefore possible to change the operation of the CG4 hardware by changing these configuration files. Changes already on the drawing board include the addition of logic for a third scrolling plane (the hardware has already been added), extra colours in the video output and changes to the number of pixels displayed on the screen.

Currently, CG4 has a screen size of 512 by 512 pixels, although with later enhancements it will be possible to increase the number of pixels on the screen. The VRAMs are arranged as nine separate planes (only eight are used in CG3 compatibility mode), three of which have horizontal scrolling capabilities. Ignoring the horizontal scrolling capabilities for the moment, the first pixel on the top line is generated by taking the least significant bit of the byte at address zero of each of the eight/nine VRAMs and forming an eight/nine bit wide signal. This signal is fed into the low eight/nine address lines of the PRAMs; the higher address lines acting as palette attribute bits (ie odd line, odd dot, flashing etc), generating at the data output of the PRAMs a value which when feed through a digital to analogue converter produces an analogue RGB value for that particular pixel. The second pixel on the top line is generated using a similar procedure on the second least significant bit of the zeroth byte and so on. The first line of 512 pixels is therefore generated using the first 64 bytes of the VRAMs, while the second line of pixels is generated using the second 64 bytes etc. The PRAMs perform a mapping from the video data to a particular colour on the screen (specified by the data values stored in the VRAMs). Software which wishes to display particular images on the screen therefore writes data to specific planes of the VRAMs depending upon which colour is to be displayed and the address specifies the location on the screen which is affected.

Three of the nine planes (only two are used for CG3 compatibility mode) are used when horizontal scrolling is required. Scrolling areas within static areas are produced by writing separte data to the scrolling and non-scrolling planes and manipulating the value of the scroll register. For a 512 by 512 pixel screen, the scroll register can hold a value between zero and 511, specifying the pixel offset between the static and scrolling data. Video data which one might think would be scrolled off the right hand side of the screen is in fact wrapped around to the left hand side of the screen on the same line. Video data on any line of a scrolling plane should therefore be considered more as a loop of pixels than a line.

Hardware assisted line drawing is performed by use of a screen pixel position register/counter on the CG4. Whenever the CPU directly accesses VRAM, the VRAM address is loaded into the screen position register/counter. By then accessing a special memory area outside the VRAM address map, the pixel at the currently stored location can be accessed, with the current location being modified after the access to move the current location up/down or left/right ready for the next access.

11.2.7 Detailed Description

11.2.7.1 Bus Sizing

(see 11.4.2 Bus Sizing schematic)

Bus sizing is performed totally within one Lattice ispLSI2064-80LT device located at U1 and transfers data between the 32 bit CPU data bus D[0..31] and the CG4's local 8 bit data bus SD[0..7]. Any transfer between the WX and the graphics hardware starts with the WX generating a transfer start signal *CGDTS. At the same time the WX CPU's *WR, SIZ[0..1] and low order address lines A[0..1] will fully specify the type of transfer ie, byte/word/long and read/write. The CG4 splits the MC68040 CPU's line (16 byte) transfers into four consecutive long transfers by asserting the transfer burst inhibit (*TBI) signal to the CPU at the end of the first long of a line transfer. For documentation on these CPU signals and the MC68040 data transfer size peculiarities, see [1].

When the bus sizing logic receives the *CGDTS signal it generates a transfer in progress signal (TRIP) for each byte of the transfer. The TRIP signal is sent to the address control Xilinx U3 (sheet 3) which which returns a transfer acknowledge (TACK) signal to the bus sizing Lattice, signaling that the current byte has been reached its destination. When all bytes in the current read/write operation have been tranfered, the Lattice generates a transfer acknowlegde (*TA) which signals the CPU that the current operation is complete. Each CPU to graphics hardware operation will therefore start with a *CGDTS and end with the CG4 generating a *TA, whether the operation is a byte, word or long transfer. Internal to the CG4, word and long operations will be broken into byte operations; with a TRIP and TACK signal for each byte transfer within the word or long transfer.

The bus sizing Lattice also generates two bits of address; GMA[0..1], which the address control Xilinx U3 uses instead of the CPU address bits A[0..1], in order to correctly address the 8 bit wide CG4 local data bus from the 32 bit wide CPU data bus.

Other signals of interest generated by the bus sizing Lattice are the qualified write enable signal (QWE) which is asserted whenever TRIP is asserted and the current operation is a write to the graphics hardware, and LBYTE[0..3], the bus sizing internal state signals.

Signals SDOCGD, SDOMIXR, *LISPEN, LMODE and LXCLK are used only to program the Lattice device.

11.2.7.2 Address Control Xilinx

(see 11.4.3 Address Xilinx schematic)

The address control Xilinx (ADDX, U3) interfaces to the bus sizing Lattice U1 (sheet 2) and the 68040 CPU with signals TRIP, QWE, TACK and *WR as described in section 5.1. ADDX has four main functions;

1) Perform adddress decoding; to allow the CPU access to VRAM and control registers within both ADDX and DATAX and to generate appropriate read/write signals for the VRAMs, PRAMs and DATAX.

2) To synchronise with the data multiplexer Xilinx U4 (DATAX) (datax.sch) using the SYNC signal, generate the video synchronisation signals (*VSYNC, *HSYNC, BLANK) and generate addresses for stepping through VRAM while generating the video output data.

3) To allow CPU access to the VRAM when it is not being used for video generation.

4) To disable video generation (*PALEN driven LOW) and allow CPU access to the PRAMs.

Input addresses are supplied to ADDX with signals GMA[0..1] and A[2..17] making up an 18 bit address bus. These address signals are multiplexed inside ADDX with internally generated video access addresses to provide the VRAM address signals RA[0..16], so that during CPU accesses GMA[0..1]/A[2..16] are fed directly to RA[0..16] whilst during video generation accesses, internally generated addresses drive RA[0..16]. In addition scrolling address lines SA[0..6] are generated by adding (ingnoring any carry which may be generated) the value of a horizontal scroll register (internal to ADDX) to RA[0..7] to produce the scrolling address lines SA[0..6].

During CPU access to VRAM, signal VRAMACC is driven high to indicate to DATAX that a VRAM access is taking place. ADDX also generates the appropriate output enable and write signals for the VRAMs (*RAMOE and *RAMWR). Individual output enables (*PEN[0..1]) and write (*PWR[0..1]) signals are generated for accessing the PRAMs. When the CPU accesses control registers inside DATAX, ADDX asserts DXSEL and either of DXWR and DXRD.

Control registers internal to ADDX may be accessed from software via the 8 bit data bus SD[0..7]. The address of these internal registers may change when the configuration file for ADDX is changed to modify existing features or add new features.

Palette address lines PA[8..14] generated by ADDX will be discussed in the section titled Video Generation.

Synchronisation of ADDX and DATAX is necessary to ensure that ADDX supplies the VRAM with video generation addresses and prevents CPU access when the video data is being loaded into the internal shift registers of DATAX. The SYNC signal is generated by DATAX and is low for one clock period of every eight periods of BCLKCGAD. The first five cycles of BCLKCGAD after the SYNC pulse are used for CPU access to the VRAM whilst the remaining cycles are used by the video generation circuitry.

Other signals of interest are the bit select lines BS[0..2] and BYTEMODE which are generated by ADDX for CPU access to the VRAMs. When BYTEMODE is HIGH VRAM is accessed in bytes of eight contiguous pixels while when it is LOW a single pixel within the byte (ie eight consecutive pixels) is accessed depending on the value of the three bit select lines.

11.2.7.3 Data Multiplexer and Video Shift Registers

(see 11.4.4 Data Multiplexer schematic)

The data multiplexer Xilinx (DATAX, U4) sits between the 8 bit sized data bus SD[0..7] and the 72 bit graphics data bus which is arranged as nine groups of 8 bits: DA[0..7], DB[0..7], DC[0..7], DD[0..7], DE[0..7], DF[0..7], DG[0..7], DH[0..7] and DZ[0..7]. DATAX contains an internal set of registers which drive the VRAM enable signals VRE[0..8], specifying which VRAM planes are accessed during a CPU read or write.

For a CPU byte write operation, the data arrives at the DATAX 8 bit port, is manipulated internally depending on the value of internal registers and is then placed on the nine 8 bit data buses Dx[0..7]. For byte read operations data arrives via the nine 8 bit data buses is combined internally to DATAX to generate an 8 bit output which is driven onto SD[0..8]. When writing to a particular bit within a byte (BYTEMODE is LOW), DATAX must first read the full byte from the nine 8 bit buses, modify the corect bit internally and then write the modified data back onto the nine 8 bit buses.

During video generation data is read from the VRAMs via the nine 8 bits buses (all of the planes are enabled) and loaded into a set of internal shift registers. The 72 bits read in this operation contains the data from all nine/eight planes for the display of eight consecutive pixels. The data

values for the eight consecutive pixels are then clocked output of DATAX via the palette address lines PA[0..8] over the following eight cycles of the 33mhz clock BCLKCGMX. PA[0..8] drive the low eight address lines of the PRAMs which convert which map the plane data values to colour values specified by the data contained within the PRAMs. When the PRAMs are being accessed by the CPU (*PALEN is LOW), PA[0..8] are tri-stated.

Most of the other signals connected to DATAX are generated by ADDX; VRAMACC is HIGH when the VRAMs are to be accessed by the CPU, *PALEN is LOW when the PRAMs are being accessed, *RAMWR and *RAMOE are the VRAM write and output enable lines which are also connected to the VRAMs. DXSEL, DXWR and DXRD are used to access registers internal to DATAX in conjunction with address lines RA[0..4]. Signals NC[0..4] and EIGHT are unused at present but may be used at some later date.

11.2.7.4 Video RAM

(see 11.4.5 Video RAM schematic)

The nine SRAMs which make up the VRAM bank are currently 32kbyte by 8 bit devices. This is the minimum size required to produce a screen image of 512 by 512 pixels. The RAMs are currently placed in sockets to allow 128k by 8 bit SRAMs when the screen image is enlarged in the future.

The VRAM chips share common output enable and write signals, *RAMOE ans *RAMWR. Address lines generated by ADDX (RA[0..16] and SA[0..6]) specify VRAM addresses, with only the VRAMs associated with the scrolling planes being connected to the scrolling address lines SA[0..6].

Each VRAM chip has its own enable signal, one of the VRE[0..8] lines, which allow individual VRAMs to be accessed even though they share common output enable and write signals. In addition, each VRAM has its own data bus which connects only to DATAX; one of the buses DA[0..7], DB[0..7], DC[0..7], DD[0..7], DE[0..7], DF[0..7], DG[0..7], DH[0..7] and DZ[0..7].

11.2.7.5 Video Generation

(see 11.4.6 Video Generation schematic)

The video generation hardware consists for two palette RAMs U14 and U15, two 22v10 GALs U16 and U17 and four tristate buffers. During video generation (*PALEN is HIGH) the palette address lines PA[0..14] are driven from two different sources; PA[0..8] carries the video plane data from DATAX whilePA[9..14] carries the palette attribute bits generated by ADDX. When the CPU accesses PRAM (*PALEN is LOW), video generation is halted resulting in a blank screen and palette address lines PA[0..14] are tristated. The address lines RA[0..14] are fed through tristate buffers U18 and U20 (which are tristated by *PALEN being HIGH) replacing PA[0..14]. The PRAMs share a common output enable signal *PALOE but have separate write signals *PWR0 and *PWR1. The data lines of the two PRAMs are connected to the sized data bus by bi-directional tristate buffers U19 and U21, which have separtate enable signals *PEN0 and *PEN1. GALs U16 and U17 take the video data from the PRAMs, add the correct blanking period and video synchronisation signals obtained from *HSYNC, *VSYNC and BLANK and generate 4 bits of colour for each of red, green and blue.

11.2.7.6 High Speed Serial Link (HSSL or Mixer) Interface

(see 11.4.7 Mixer Interface schematic)

The HSSL interface is a 1Mbit bidirectional full-duplex serial link with hardware handshaking designed specifically to interface with the Amek console used in FAME systems. All signals are transmitted over the HSSL cable in differential mode using an AM26LS31 differenial driver (U27) at the transmitter end and opto-couplers (U24, U25 and U26) at the receiver to electrically isolate the console from the MFX3 in order to prevent any possibility of ground loops. The HSSL cable carries data, clock and write signals as well as a receiever FIFO full signal, which is used in the transmitter control logic to hold off or halt transmission until there is room in the receiver's FIFO for another byte of data.

All of the HSSL control and CPU interfacing hardware is located in a Lattice ispLSI2064-80LT (WXMIXR, U2). Any CPU write to or read from the HSSL begins a HSSL specific transfer start signal, *MIXERTS, being generated on the WX. When the read or write operation is finished, WXMIXR sends a transfer acknowledge signal *TA back to the WX. The internals of WXMIXR includes a read only status register and a read/write control register.

To transmit a character on the HSSL, the CPU must first check the status register inside WXMIXER, to ensure that the transmitter FIFO's (U23) FIFO full flag is not asserted. If everything is OK, it may write a byte to the transmitter, with the 8 data bits being transferred from the CPU via the 8 least signifcant bits of the CPU data bus and the write signal for the FIFO being generating by WXMIXR. Whenever the transmit FIFO is not empty and the other end's receiver is not full (ie *RCVFF is HIGH), WXMIXR will load a byte from the transmit FIFO into an internal shift register and shift the data out serially (at 1/16th of the 20mhz clock) driving the data and clock signals XMTDAT and *XMTCLK. At the end of the byte transfer WXMIXR asserts the serial write signal *XMTWR.

Serial data is received from some transmitter via signals RCVDAT+, RCVDAT-, *RCVCLK+, *RCVCLK-, *RCVMW+ and *RCVWR-. Opto-couplers U24, U25 and U26 convert these differential signals into single ended signals RCVDAT, *RCVCLK and *RCVWR. *RCVCLK shifts the serial data RCVDAT into a shift register inside WXMIXR with a parallel output RD[0..7]. At the end of eight bits of data, the full transfered data byte exists on RD[0..7] and signal *RCVWR from the transmitter writes the byte into the receiver FIFO U22.

If there is data in the receive FIFO, a bit of the status register in WXMIXR is set and optionally an interrupt (*MIXERINT) can be generated. When the CPU reads data from the receive FIFO, WXMIXR generates the FIFO read signal *MRRD and the data is transferred over the least significant 8 bits of the CPU data bus D[0..31].

11.2.7.7 Expansion Connector and Clock Buffer

(see 11.4.8 Connector, Clock Buffer schematic

Connectors JP3 and JP4 connect the CG4 hardware to the WX. The clock buffer chip CY7B9920-7SC (U28), receives a 33MHz clock from the WX and buffers it to produce a number of separate clock signals for the rest of the board.

11.2.8 Programming the Lattice Devices

Both Lattice devices may be programmed by connecting a special download cable from a PC to JP8 of the WX, while the CG4 is attached to the WX and power is ON. See [3].

11.2.9 Testing and Diagnostics

Two OS-9 programs have been written to test the operation (CG4TEST) and diagnose faults (CG4DIAG) in the CG4. Both programs must be run with DIP switch #2 of the WX ON and a PC connected to the serial port JP1 of the WX so that all I/O can be viewed on the screen of the PC while testing is being carried out. In addition, when running CG4DIAG, DIP switch #3 must also be on to disable the 68040's Memory Management Unit.

11.2.10 Additional References

[1] Chris Alfred, Motorola MC68040 operation, Fairlight ESP.
[2] Motorola, MC68040 32 bit Microprocessor User's Manual.
[3] Chris Alfred, ESP-WX Waveform Executive Functional Description, Fairlight ESP.
[4] Lattice Semiconductor, Lattice Data Book 1994.
[5] Xilinx, The Programmable Logic Data Book 1994.
[6] Fairlight ESP, CDIAG v3.0.

11.3 ESPCG4 Field Diagnostics

11.3.1 Equipment

The following equipment is required :

a) An ESPWX processor board.

b) An ESPRIO card and a 26-way IDC loopback cable and plug for testing the high speed serial link on the ESPCG4. A description of this cable is included later in this section.

c) An IBM-PC compatible computer with at least a 386 processor running Microsoft Windows 3.1, Windows 3.11 or Windows 95, with a free serial and parallel port.

d) A cable to connect the ESPWX serial port to the PC.

e) A communications program such as Telix.

11.3.2 ESP-WX Setup Procedure

a) The ESPWX should be plugged into the MFX3^{plus} and the serial cable should be connected between the ESPWX and the PC. The 8-pole DIP switch at the front of the board should have switch 2 in the ON position with all other switches in the OFF position.

b) Telix on the PC should be set up to communicate on the correct serial port at 9600 baud with 1 stop bit, no parity bit and 8 data bits. With Telix running, the power supply to the ESPWX can be switched on. If correctly set up, the bootup message from the ESPWX should be displayed in the Telix window and should end up with a '#:' prompt.

If everything above has gone smoothly, it is now possible to test ESPCG4 cards.

11.3.3 ESPCG4 Test Procedures

11.3.3.1 General Field Diagnostic

Connect the 26-way IDC loopback cable (including the ESPRIO) to JP2 of the ESPCG4 and switch ON the MFX3plus. When the bootup process has finished, type the following command in the Telix window on the PC:

```
cg4diag <enter>
```

at the '#:' prompt. This program should run and print the following :

```
———=======++++++++++++++++=======———

       CG4 Diagnostics Program v1.00

———=======++++++++++++++++=======———

CG4 PCB Revision : 0x03

Testing clock for Address Xilinx (U3).

      Clock to current Xilinx OK.

Testing data lines for Address Xilinx (U3).

    Data bus SD[0..7] to current Xilinx OK.

Testing clock for Data Xilinx (U4).

    Clock to current Xilinx OK.

Testing input address lines for Address Xilinx (U3).

    Test completed : No errors.

    Input address bus, GMA[0..1] and A[2..17] to U3 is OK.

Testing communication lines between Xilinxes (U3 & U4).

    Test completed : No errors.

Testing registers in Xilinxes (U3 & U4).

    No Errors.

Testing VRAMs (U5, U6, U7, U8, U9, U10, U11, U12 and U13).

    VRAM Plane 0 (U 5) : 0 errors.

    VRAM Plane 1 (U 6) : 0 errors.

    VRAM Plane 2 (U13) : 0 errors.

    VRAM Plane 3 (U 7) : 0 errors.

    VRAM Plane 4 (U 8) : 0 errors.
```

```
VRAM Plane 5 (U 9) : 0 errors.
      VRAM Plane 6 (U10) : 0 errors.
      VRAM Plane 7 (U12) : 0 errors.
  Dual palettes have been detected.
  Checking PRAM (U3, U14, U15, U18, U19, U20 and U21).
      OSK palette : 0 errors.
      CMI palette : 0 errors.
      MDR palette : 0 errors.
  Testing HSSL (X1, U2, U22, U23, U24, U25, U26 etc).
      FIFO ready test      : zero errors.
      FIFO half full test  : zero errors.
      FIFO full test       : zero errors.
  Test completed. Board functioning correctly.
  ----=======++++++++++++++++++++----
```

11.3.3.2 General Functional Test

Connect the 26-way IDC loopback cable (including the ESPRIO) to JP2 of the ESPCG4 and switch ON the MFX3^{plus}. When the bootup process has finished, type the following command in the Telix window on the PC:

```
cg4test <enter>
```

at the '#:' prompt. This program should run and print the following :

```
----=======++++++++++++++++++++----
     CG4 Test Program
----=======++++++++++++++++++++----
CG4 PCB revision : 0x04
Test Xilinx load (y/n)? : y
Xilinx load sucessful (wbgs.bin).
Test read back registers (y/n)? : y
Control register (0x82FCC6): OK.
Scroll register   (0x82FCC8): OK.
Colour register   (0x82FCCA): OK.
```

```
Erase register     (0x82FCCB): OK.

Test palette RAM (y/n)? : y

Testing PRAM write then read.

      OSK palette : 0 errors.

      CMI palette : 0 errors.

      MDR palette : 0 errors.

Testing PRAM write then read.

      OSK palette : 0 errors.

      CMI palette : 0 errors.

      MDR palette : 0 errors.

Checking PRAM as BYTEs.

      OSK palette : 0 errors.

      CMI palette : 0 errors.

      MDR palette : 0 errors.

Test Video RAM (y/n)? : y

      VRAM Plane 0 : 0 errors.

      VRAM Plane 1 : 0 errors.

      VRAM Plane 2 : 0 errors.

      VRAM Plane 3 : 0 errors.

      VRAM Plane 4 : 0 errors.

      VRAM Plane 5 : 0 errors.

      VRAM Plane 6 : 0 errors.

      VRAM Plane 7 : 0 errors.

Test Video RAM AI (y/n)? : y

      VRAM Plane : 0 : 0 errors.

      VRAM Plane : 1 : 0 errors.

      VRAM Plane : 2 : 0 errors.

      VRAM Plane : 3 : 0 errors.

      VRAM Plane : 4 : 0 errors.

      VRAM Plane : 5 : 0 errors.
```

```
      VRAM Plane : 6 : 0 errors.

      VRAM Plane : 7 : 0 errors.

Test Video RAM across planes (y/n)? : y

      0 errors.

Test auto increment hardware (y/n)? : y

      Byte write, move down, starting from 0x828000.

      Byte write, move up, starting from 0x82BFFF.

Test auto increment hardware II (y/n)? : y

      Top line left to right.

      Right line top to bottom.

      Bottom line right to left.

      Left line bottom to top.

      Top left to centre.

      Top-right to centre.

      Bottom-left to centre.

      Bottom-right to centre.

Test auto increment hardware III (y/n)? : y

Test BitBox (y/n)? : y

Test BitBox II (y/n)? : y

Test colour III (y/n)? : y

Test horizontal scrolling hardware (y/n)? : y

Checking palette.

Checking PRAM as BYTEs.

      OSK palette : 0 errors.

      CMI palette : 0 errors.

      MDR palette : 0 errors.

----========++++++++++========----

      End of CG4 test program.

----========++++++++++=========----
```

11.3.4.3 Mixer Port Test

Connect the 26-way IDC loopback cable (including the ESPRIO) to JP2 of the ESPCG4 and switch ON the ESPWX. When the bootup process has finished, type:

```
hssltest <enter>
```

at the '#:' prompt. This program should run and print the following :

```
———========+++++++++========———

       ESP-CG4 HSSL Test Program

———========+++++++++========———

ESP-CG4 PCB Revision : 0x04

First HSSL test (y/n)? : y

      Reseting HSSL port.

      Status : OK.

      Two characters transmitted and received sucessfully.

Test HSSL ready operation (y/n)? : y

      RxFull  : FALSE   TxFull : FALSE

      RxHalf  : TRUE    TxHalf : TRUE

      TxReady : TRUE

      Characters transmitted : 688565

      Characters received    : 688306

      Zero errors.

Test HSSL half full operation (y/n)? : y

      RxFull : TRUE     TxFull : FALSE

      RxHalf : TRUE     TxHalf : TRUE

      Characters transmitted : 463962

      Characters received    : 463449

      Zero errors.

Test HSSL full operation (y/n)? : y

      RxFull : TRUE     TxFull : TRUE

      RxHalf : TRUE     TxHalf : TRUE

      Characters  transmitted  :  299983
```

```
        Characters  received       :  298959

        Zero   errors.

    Place  HSSL  in  loopback  mode  (y/n)?  :  n

    Detailed  HSSL  test  (y/n)?  :  n
```

11.3.4 Loopback Plug

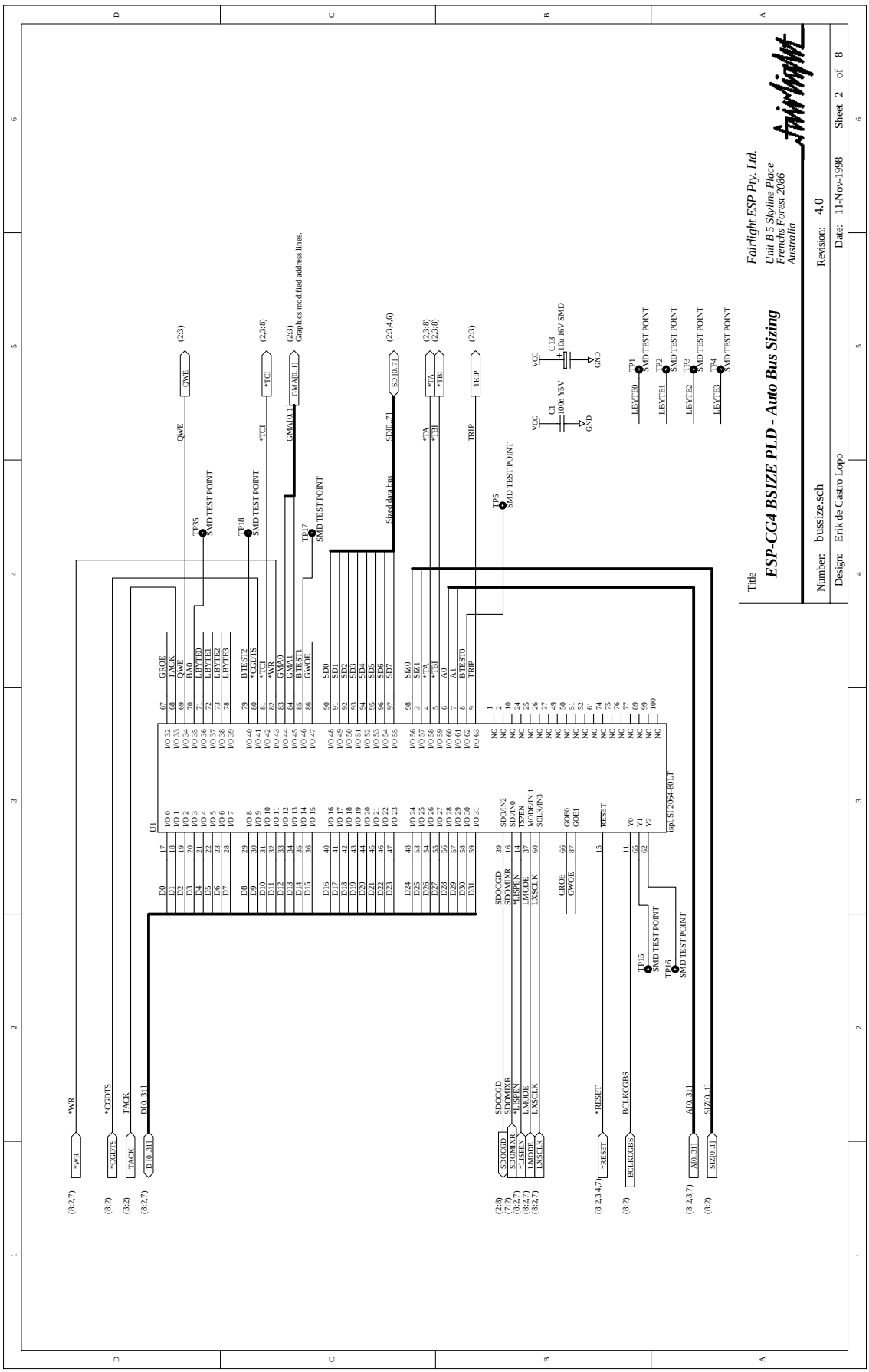
The loopback plug is made from a 25 pin male D connector. The following connections should be made on this D connector.

pin 2	<—>	pin 8
pin 3	<—>	pin 21
pin 4	<—>	pin 10
pin 5	<—>	pin 11
pin 14	<—>	pin 20
pin 15	<—>	pin 9
pin 16	<—>	pin 22
pin 17	<—>	pin 23

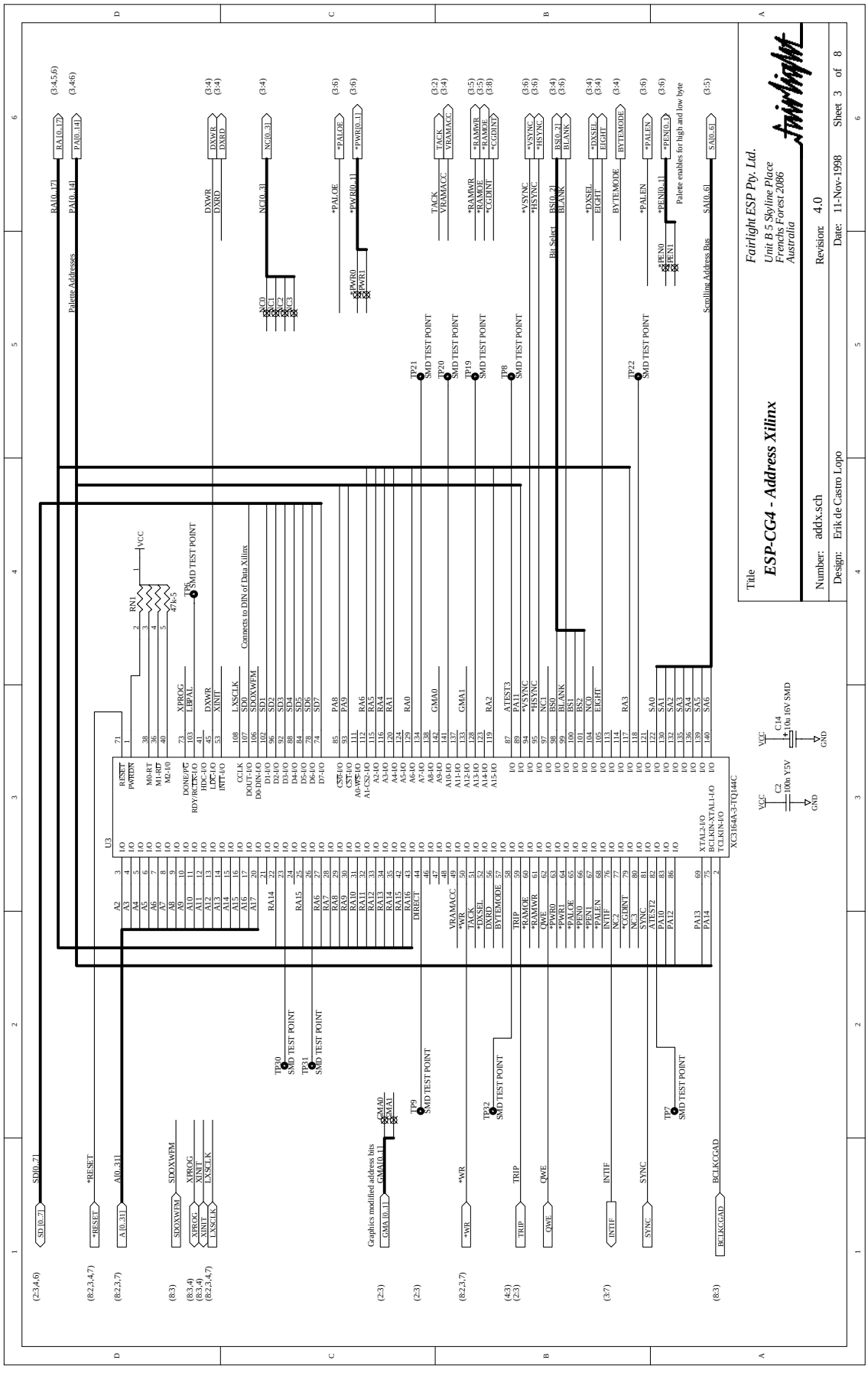
11.4 ESPCG4 SCHEMATICS

11.4.1 ESPCG4 INTERCONNECTING DIAGRAM

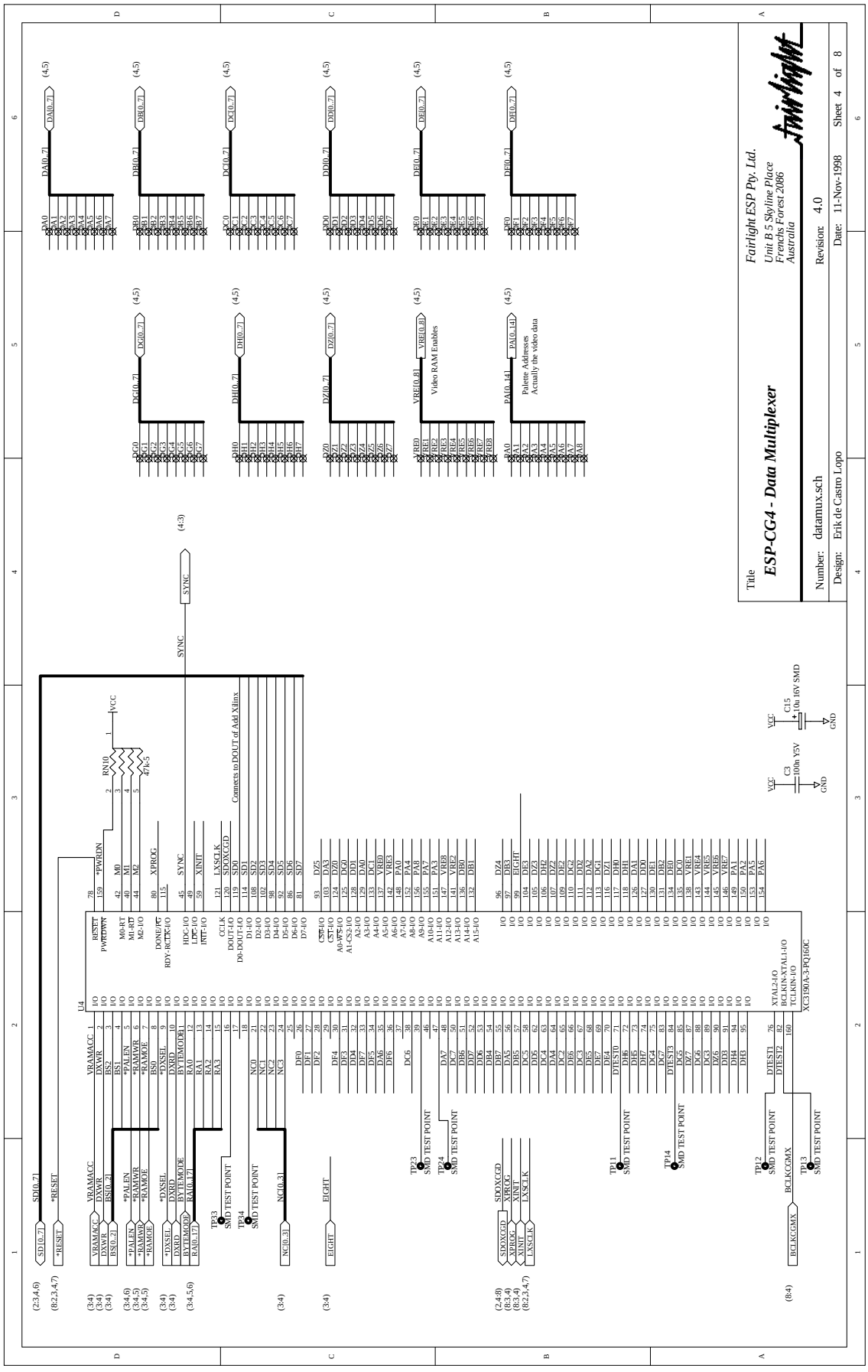
11.4.2 Auto Bus Sizing



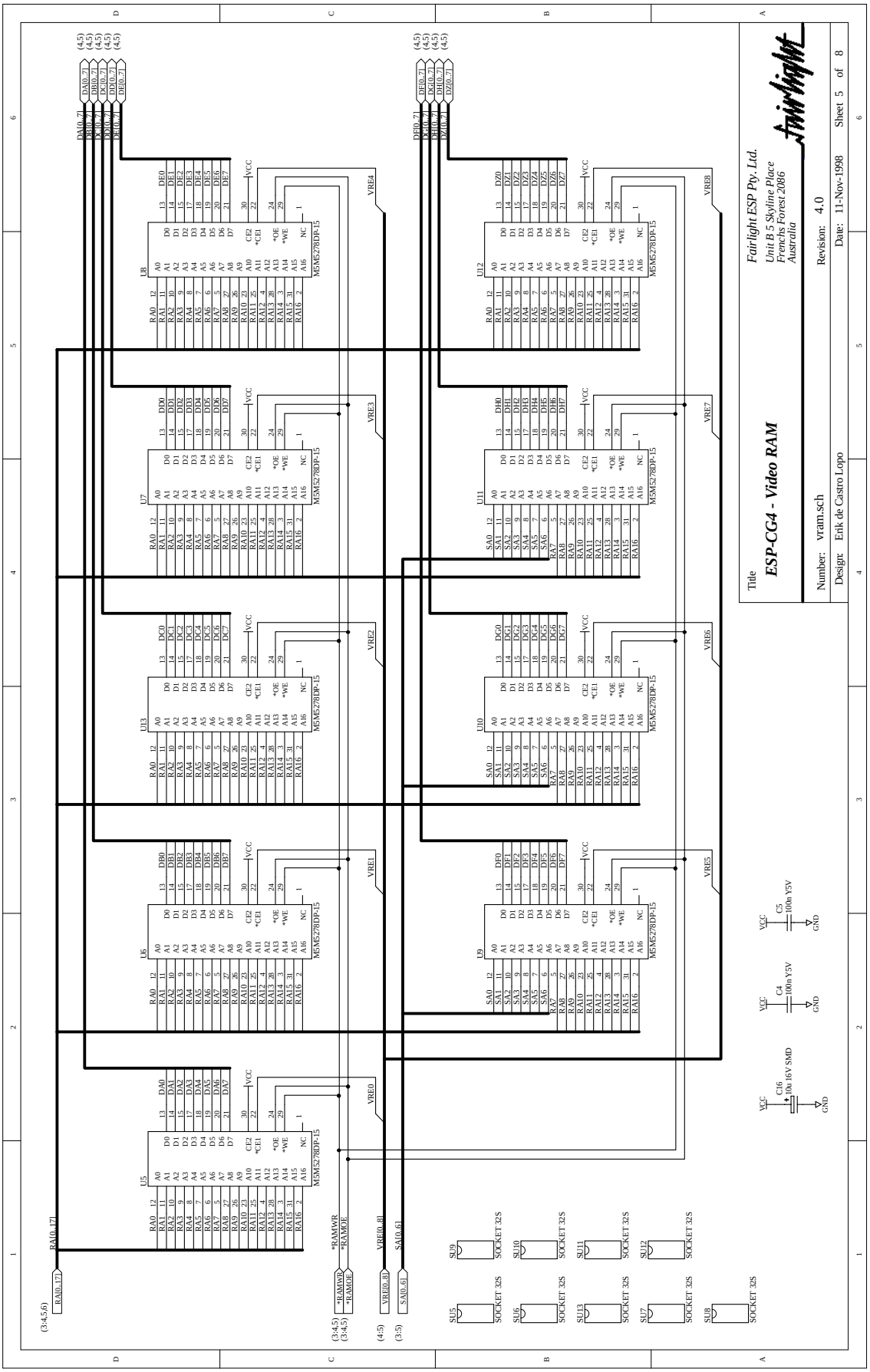
11.4.3 Address Xilinx



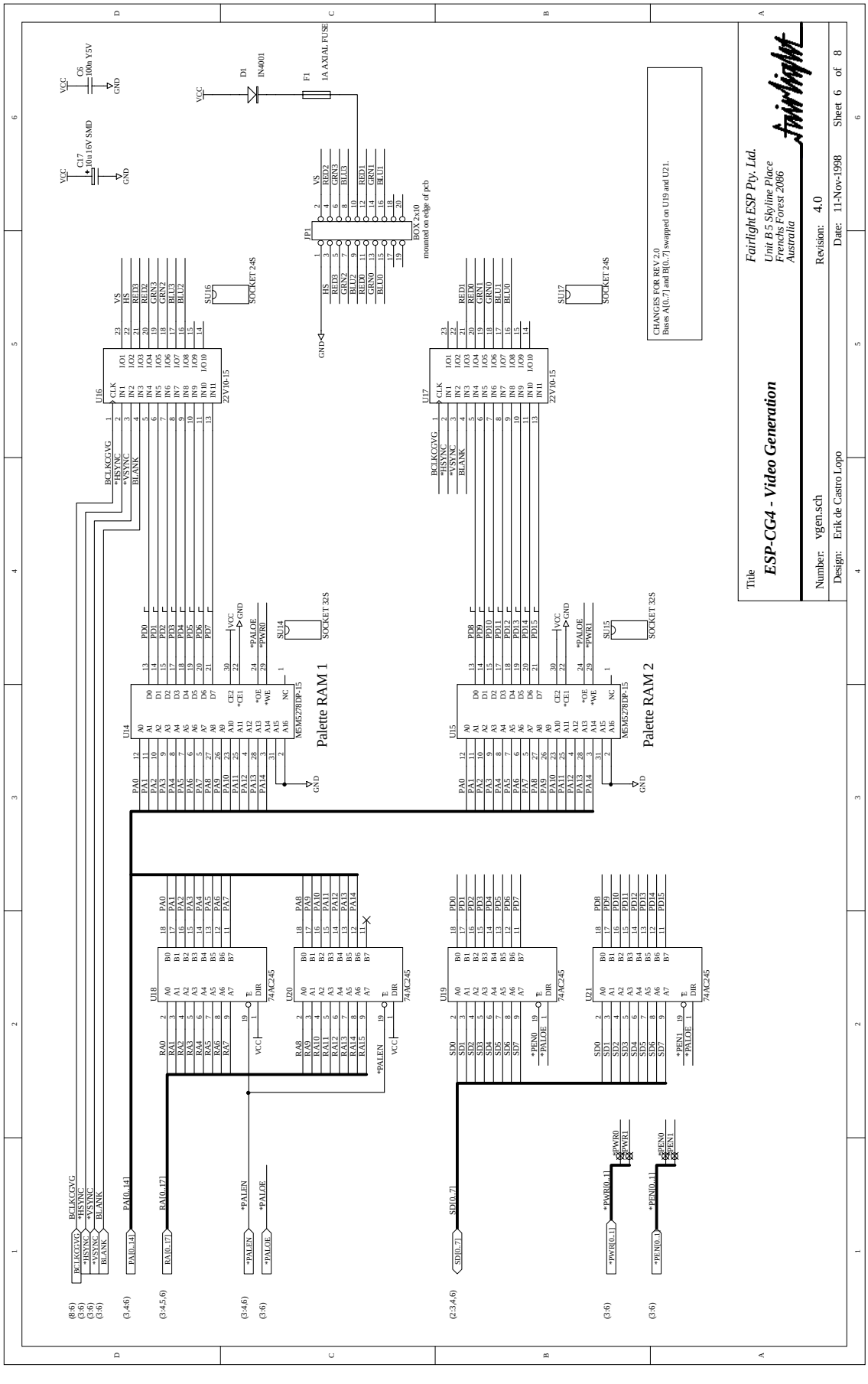
11.4.4 DATA MULTIPLEXER



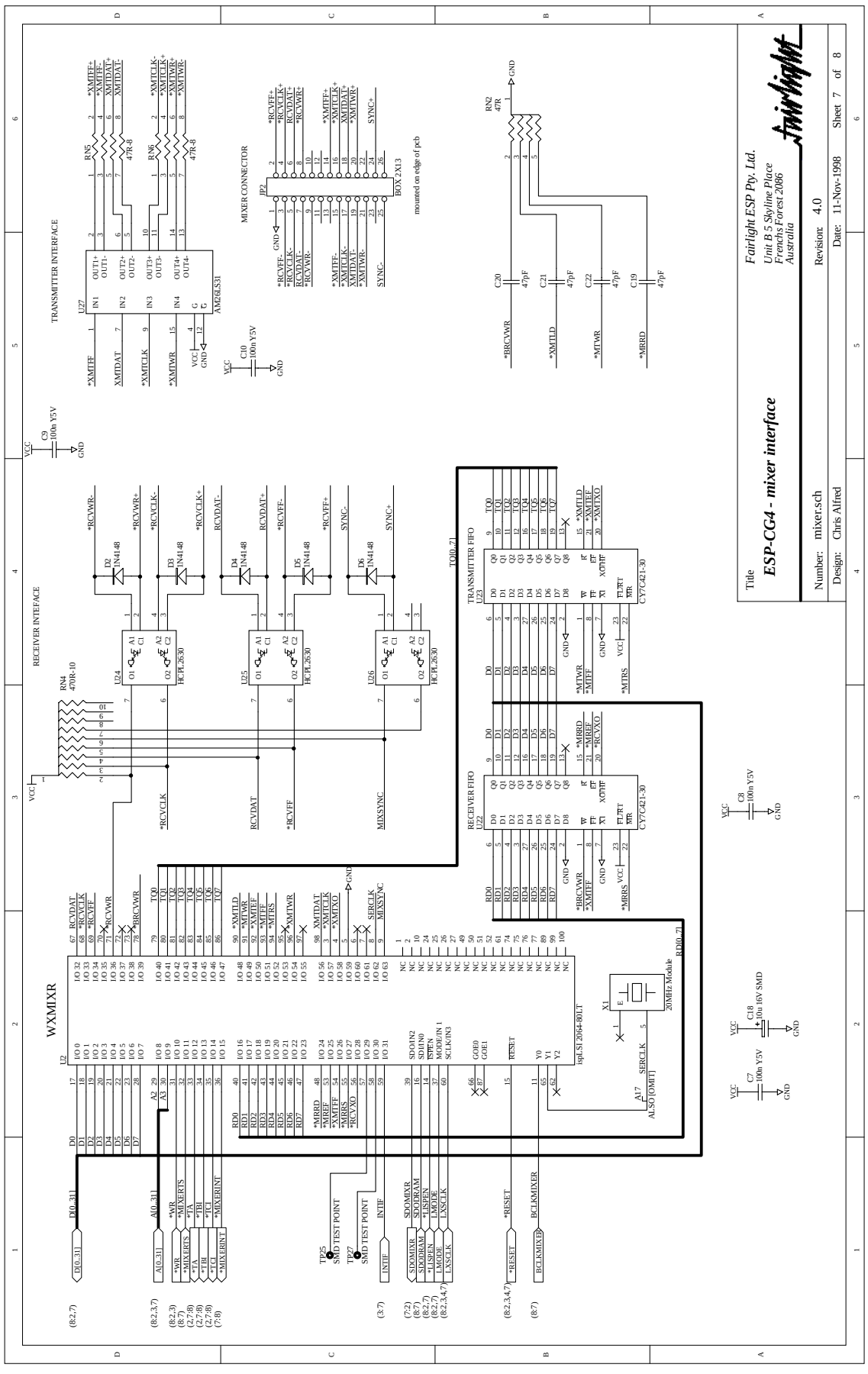
11.4.5 VIDEO RAM



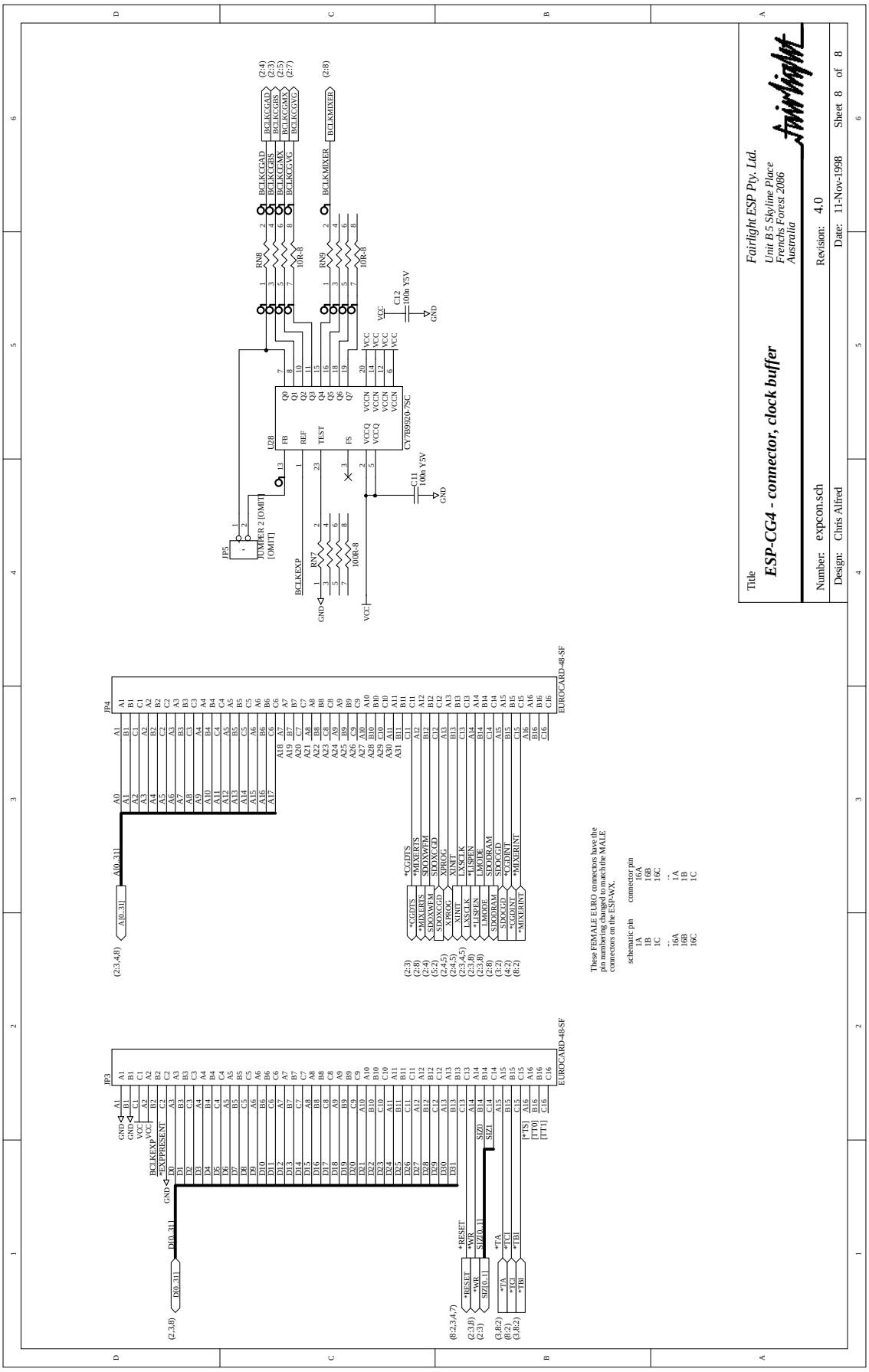
11.4.6 VIDEO GENERATION



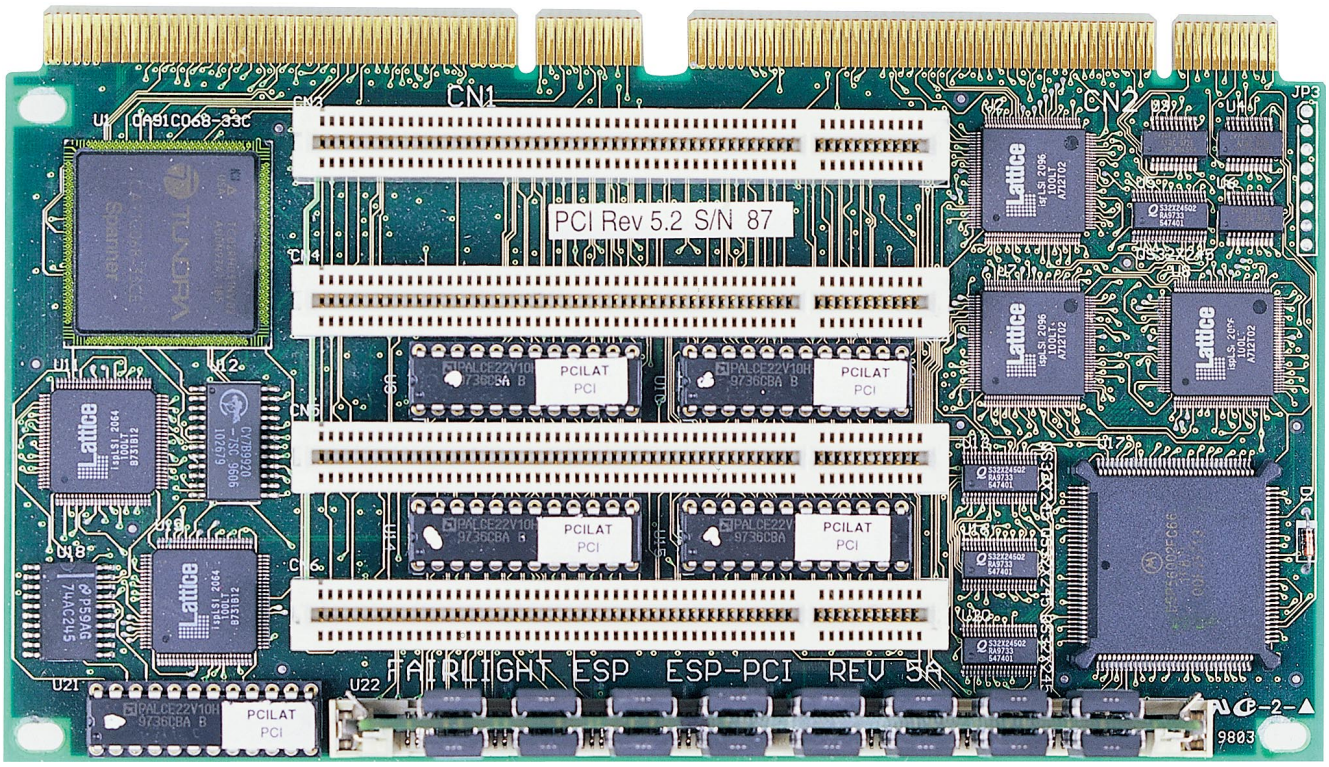
11.4.7 MIXER INTERFACE



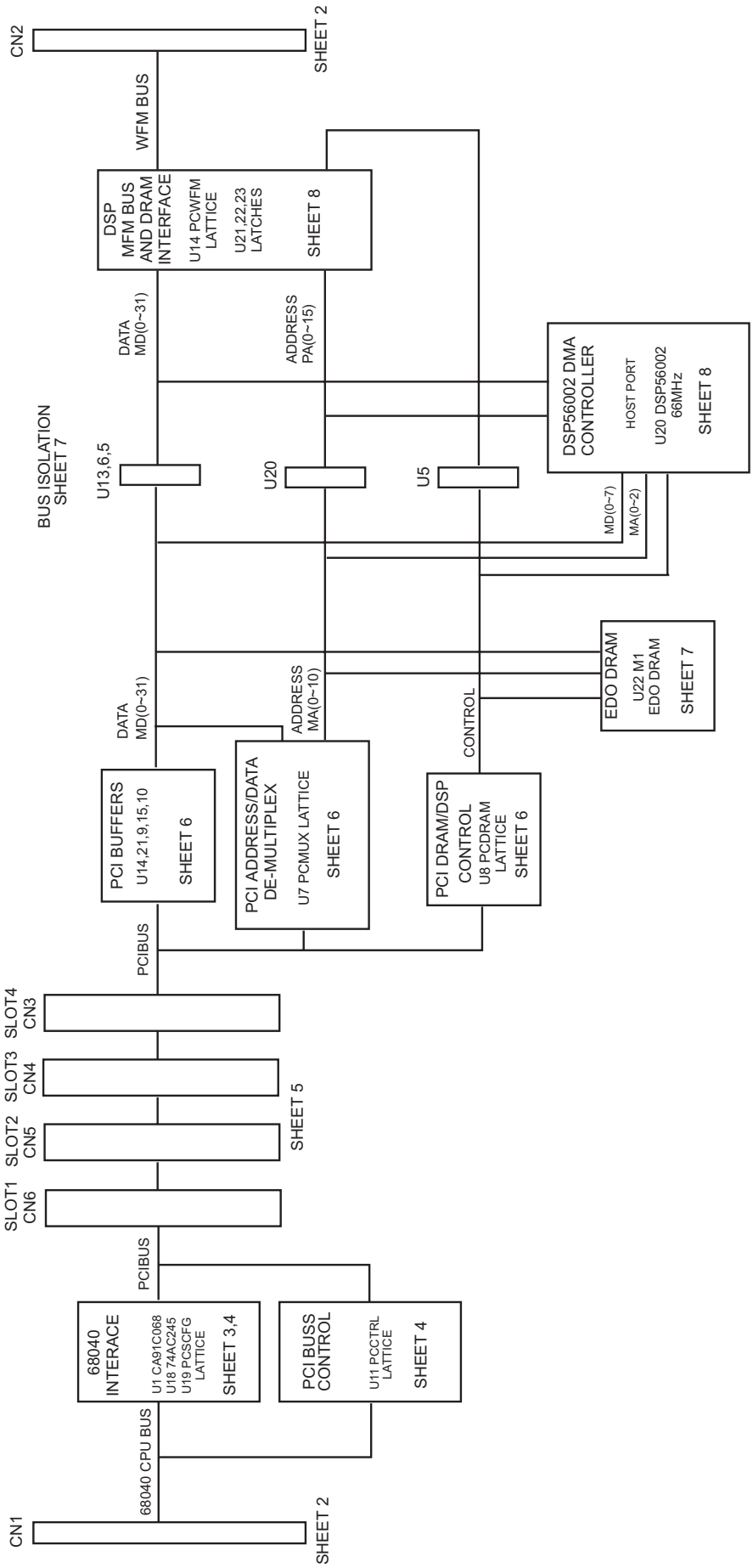
11.4.8 Connector, Clock Buffer



12.0 ESPPCI PCI Bus Interface Card



12.1 ESPPCI Block Diagram



12.2 ESPPCI Circuit Description

12.2.1 Document Revision

22.12.1997 v1.0 cea: created

12.2.2 Terminology

ESP-WX	ESP-WX Waveform Executive card
PCI	Peripheral Component Interconnect A third party defined bus used in PCs
ESP-PCI	ESP-PCI PCI interface card
WFM	The Fairlight Waveform Bus
DMA	Direct Memory Access Hardware designed to transfer data without CPU intervention
ESP-TS	Turbo SCSI card

12.2.3 Introduction

To allow Fairlight to use the many PCI compliant cards available to the PC world, the ESP-PCI card provides a PCI interface to the ESP-WX. It is connected as a daughter card at connectors CN1 and CN2 of the ESP-WX.

Included on the ESP-PCI is a 68040 (the CPU used on the ESP-WX) to PCI interface and support hardware, 4 PCI slots and a DSP driven interface to the WFM bus with 8M of DRAM for network packet buffering.

The main requirement for the ESP-PCI card was to provide adequate bandwidth for 24 tracks of audio playback across a 100BaseT network interface. Due to the large amounts of processing and guaranteed data transfer required for networking, a Motorola 56002 DSP is programmed as a DMA contoller to allow bursting of data to and from the WFM bus. The control information for the DMA transfers is held with the data in the ESP-PCI DRAM as a linked list read by the DSP. These transfers occur concurrently with network transfers into the DRAM from a third party network controller in the PCI slots. The same interface is used for SCSI cards placed in PCI slots.

12.2.4 Hardware Description

The ESP-PCI hardware is sectioned into the following functional blocks:

1. ESP-PCI clock distribution
2. 68040 PCI interface
3. PCI interface support
4. PCI slots
5. 8M DRAM shared with DSP and PCI
6. DSP DMA engine
7. WFM bus interface for DSP

12.2.4.1 ESP-PCI Clock Distribution

U12 (Cypress CY7B9920-7SC) phase locks the BCLKPCI 33MHz clock from the ESP-WX into 8 aligned and buffered clocks. Each of these clocks are damped with 10R resistors for clean edges.

12.2.4.2 68040 PCI Iinterface

The CA91C068 Spanner chip at U1 converts Motorola CPU transfers into PCI transfers. When power is applied and the PCI bus is un-reset (PCIRST# high), this chip is not accessable from the 68040 side and so U19 is programmed with a simple state machine to write the value 6 to configuration register 4 from the PCI side. Once done, the Spanner chip appears at memory address $0000F800. As this conficts with the 68040 requiring Flash ROMs at this address, an addressable latch on the ESP-WX. Writing any data to $008C0000 selectes Flash ROMS (default after RESET), writing any data to $008D0000 selects the Spanner chip.

During normal PCI operation, U19 drives the *CBE0..4 lines via U18 (74AC245) using the *CBEDIS signal for the 68040 transfers.

12.2.4.3 PCI Interface S support

U11 provides the decoding for PCI accesses. Any access in the range $10000000-$3FFFFFFF performs a normal PCI access. Any access in the range $40000000-5FFFFFFF asserts the IDSEL line as selected in the control register and performs a PCI configuation cycle.

All arbitration for PCI accesses are handled by U11. The *REQ0..6 signals are requests, and the *GNT0..6 are the corresponding grant signals. *REQ0 has the highest priority.

The ESP-PCI control and status registers are also in U11. The format of these registers are set-out below. These registers are all byte wide.

PCI cards present register ($60000003 read only)

Bit 1..0	PCI slot 1 presence bits
Bit 3..2	PCI slot 2 presence bits
Bit 5..4	PCI slot 3 presence bits
Bit 7..6	PCI slot 4 presence bits

Control register ($60000007 read/write)

Bit 2..0	CFGID2..0 Configuration select Selects 1 of IDSEL0..4 to be asserted during a configuration cycle.
Bit 3	*RST Active low PCI bus reset. Set low at power on. Must be set to use ESP-PCI card.
Bit 4	IOSPACE Enables access to PCI I/O space.
Bit 5	reads as 0
Bit 6	read only PERR PCI bus parity error status
Bit 7	read only SERR PCI bus system error status

DSP control register ($6000000B read/write)

Bit 3..0	PCISEL3..0 Selects base address of ESP-PCI [not used]
Bit 4	*DSPRST active low DSP reset. Must be set high to use DSP.
Bit 5	LOCK Used to grant exclusive access for the 68040 to the PCI bus.
Bit 6	reads as 0
Bit 7	DSPIRQ DSP interrupt to ESP-WX status

Revision register ($6000000F read only)

Returns the PCB revision of the ESP-PCI card.

12.2.4.4 PCI SLOTS

CN6,CN5,CN4,CN3 are PCI slots 1 to 4 respectively. These are standard 5V PCI slots.

12.2.4.5 8M DRAM SHARED WITH PCI AND DSP

The 8M DRAM at U22 is dual ported between the PCI bus and the DSP at U17. The DSP has the higher priority to the DRAM. All data held in the DRAM is little-endian.

For PCI accesses, U8 provides the arbitration decoding and controls the DRAM. U7 provides the addresses and the write data. As the Lattice devices are not PCI compliant, the AMD pals at U14,21,9,15,10 are used to drive control and read data to the PCI bus.

When the DSP gains access to the DRAM via the *DSPREQ (DSP request) and *DSPACK (DSP acknowledge), the DSP bus is connected to the DRAM via the QuickSwitches at U20,13,16,5. The control is provided by addressable latches in the Lattice at U2. The state of the addressable latches is set by any read or write access to the following addresses by the DSP by decoding lines PA11 to PA15:

$A000-$A7FF	set *DSRAS0,*DSRAS2 low
$A800-$AFFF	set *DSRAS0,*DSRAS2 high
$B000-$B7FF	set *DSRAS1,*DSRAS3 low
$B800-$BFFF	set *DSRAS1,*DSRAS3 high
$C000-$C7FF	set *DSCAS0..*DSCAS3 low
$C800-$CFFF	set *DSCAS0..*DSCAS3 high
$D000-$D7FF	set *DSWE low
$D800-$DFFF	set *DSWE high
$E000-$E7FF	set *DSOE low
$E800-$EFFF	set *DSOE high

The PA10..1 address lines are used for the memory address lines. PA0 is used to select either *EL or *EU to select which 16 bits to access. As the DSP is only 24 bits, all data is handled as 16 quantities from the DSP side. The DSP is also big-endian, and so the bytes are swapped in the QuickSwitches.

12.2.4.6 DSP DMA ENGINE

During normal operation, the DSP is loaded with a program to read linked lists of DMA commands held in the DRAM. The DSP then performs the operation of transferring data to or from the WFM bus and DRAM and optionally imnterrupts the ESP-WX via *DSPIRQ.

12.2.4.7 WFM BUS INTERFACE FOR DSP

U2 also includes addressable registers to provide access to the WFM bus. Any access to $8000-87FF will arbitrate for the WFM bus and start the address assertion. The data written at this address is latched by U4,3,6 which becomes the WFM address. The top WA25 line is handled separately as an I/O pin via signal WA25I. To transfer the data, the access is performed via a read or write from $8800-8FFF. U2 will hold the DSP via *PWT until the transfer is complete.

12.2.5 Installation of ESP-PCI

When first installing the ESP-PCI, the system must be booted from the ESP-TS card and install the new software. New Flash ROMS with the ESP-PCI drivers blown. Once this is done, the jumpers at JP13 on the ESP-WX can be added and the ESP-WX with ESP-PCI and PCI SCSI installed by replacing the ESP-WX card in the ESP-TS slot. The SCSI cable is connected to the PCI SCSI card and the system should boot.

12.3 ESPPCI Field Diagnostics

12.3.1 Setup for diagnostics

12.3.1.1 Running from Stand-Alone ESP-WX

Minimum configuration:

1. ESP-SC
2. ESP-WX
3. Monitor
4. MFX keyboard
5. ESP-PCI under test
6. SYMBIOS DC-390U SCSI card plugged into PCI slot 1 (right most ESP-PCI slot)

12.3.1.2 Running from Complete System

Minimum machine configuration:

1. ESP-SC
2. ESP-DCC
3. ESP-TS
4. ESP-WX (remove all jumpers at JP13)
5. Monitor
6. MFX keyboard
7. Hard disk including pcidiag diagnostics connected to ESP-TS card.
   Files required on disk: pcidiag
   /dd/usr/esppci/pcidiag.lod
   /dd/usr/esppci/pciwfm.lod
8. ESP-PCI under test
9. SYMBIOS DC-390U scsi card plugged into PCI slot 1 (right most ESP-PCI slot).

12.3.1.3 ESP-WX U2 DIP Switch Settings

1 OFF
2 OFF
3 OFF
4 OFF
5 ON
6 OFF
7 OFF
8 OFF

12.3.2 Starting the Diagnostics

12.3.2.1 From Stand-Alone ESP-WX

Power-on machine and wait for booting to complete.

You should see:

```
ROM:
```

Type: pcidiag -rspd

12.3.2.2 From Complete System

Power-on machine and boot.

After 2 pages of startup text you should see:

```
OS-9/68K  V3.0     Waveform  Executive  -  68040     97/12/16  03:14:45
User name?:
```

Type: mfx<Return>

You should see:

```
Process #36 logged on    97/12/16 03:14:46
Welcome!
Fairlight OS9 Ready
mfx:
```

Type: pcidiag -rspd

12.3.2.3 Further Diagnostics

Once the above tests have all passed, the pcidsp program is used to futher test the ESP-PCI. See Section 12.4 ESPPCI DSP Field Diagnostics for usage.

12.3.3 PciDiag Command Details

The pcidiag program consists of several test groups each with sub-tests.

To run a test group, type pcidiag -# where # is the highlighted letter listed below. To run a specific sub-test, type pcidiag -#=n where n is the sub-test number.

To run several test groups, type pcidiag -<list> where <list> is a list of the highlighted test letters below.

e.g.	pcidiag -rspdmit	run all tests
	pcidiag -r=2 -m=1	run r sub-test 2, m sub=test 1

If the -a option is added, all memory accesses are displayed. This is only really useful for the r,s,p,d tests as the output can become quite large.

If the -v option is added, a verbose error report is generated to help locate faults.

r register tests

1. PCI cards present mask
2. control register test
3. dsp control register test
4. revision

s Spanner chip PCI interface tests

1. Spanner vendor ID
2. Spanner mapping

p PCI bus tests

1. Slot IDs
2. test pci data bits
3. test dram data bits
4. DSP IVR register bit test

d DRAM tests

1. write all 0's
2. write all 1's
3. data walking 0's
4. data walking 1's
5. address bits low
6. address bits high
7. inverted walking address

The order of the tests have been specifically designed to get the simplest portions of the ESP-PCI card running first.

As the pcidiag program is subject to improvements, typing pcidiag -? will show the latest list of test groups and sub-tests.

12.3.4 Notes on ESP-PCI Basic Operation

As U1, U19, U11 are connected to the CPU bus, if any of these are faulty or soldered incorrectly, it is possible that the CPU will be unable to run.

All clocking on the card is derived from the BCLKPCI signal and phase-lock regenerated by U12.

The PCI bus is little-endian as is all the data held in the DRAM at U11. This means that a write from the CPU of $12345678 will appear on the PCI bus and in the DRAM as $78563412. All tests display values from the CPU's perspective. To help in conversion, these are the byte orders on the busses (Note that the bits within the bytes are in the same order):

CPU	PCI	DRAM (U11)
D7..D0	AD31..AD24	MD31..MD24
D15..D8	AD23..AD16	MD23..MD16
D23..D16	AD15..AD8	MD15..MD8
D31..D24	AD7..AD0	MD7..MD0

12.3.5 Test Descriptions

12.3.5.1 Register tests

These tests check the data, address and control signals to U11 - the main control and status device. An access starts with a 30nS pulse on *PCITS (PCI transfer start) from the ESP-WX and completes with a 30nS pulse on *TA (transfer acknowledge) generated by U11 when the data is accepted on write or ready on read.

12.3.5.1.1 PCI cards present mask

Reads from the byte PCI cards present status at address $60000003 in U11. Each one of the 4 PCI slots has two presence detect signals #PRSNT1 and #PRSNT2 which are connected to U11 and internally pulled up by U11. All third party PCI cards must tie one or both of these signals low to indicate the presence and type of card as an inverted 2 bit code. The test displays the 2 bit code (un-inverted) for each slot starting at slot 1. A value of 0 indicates no card present.

12.3.5.1.2 Control Register Test

Checks accesses to the byte wide control register at address $60000007 in U11. This register only uses the low 5 bits and so the top 3 bits are always 0.

12.3.5.1.3 DSP Control Register

Checks accesses to the byte wide control register at address $6000000B in U11. This register only uses the low 5 bits and so the top 3 bits are always 0.

12.3.5.1.4 Revision

Reads from the byte PCB revision register at address $6000000F in U11. This register reports the value on pins 7 (msb),97 and 96 (lsb) with the top 5 bits set to 0.

12.3.5.2 Spanner Chip PCI tests

The Spanner chip (U1) is a Motorola 68040 to PCI interface chip. When power is applied, this chip is not accessable from the ESP-WX. Straight after a PCI bus reset (*RST asserted and released via the control register in U11) U19 performs two PCI writes to U1 registers to enable accesses from the ESP-WX. After this, U19 supports U1 by controlling U18 and signals *CBE0..3 during accesses from the ESP-WX to PCI.

Once U1 is accessable to ESP-WX, it appears at address $0000F800. As this conflicts with the flash ROMs on ESP-WX an addressable latch on ESP-WX selects either the flash ROMs or U1. Any byte write to $008D0000 selects U1, any byte write to $008C0000 selects flash ROMs (the default state after reset).

All configuration registers in U1 appear as little endian, and so all bytes are swapped.

12.3.5.2.1 Spanner Vendor ID

A write to $008D0000 maps U1 at address $0000F800. Address $0000F800 is read and should contain $57100048. As this access is to U1's PCI configuration ID register, a successful PCI cycle must be performed.

12.3.5.2.2 Spanner Mapping

A write to $008D0000 maps U1 to $0000F814. A write of $00000020 to U1's configration register at $0000F814 remaps U1 configuration registers to $2000F800. $2000F800 is read and checked for a PCI ID of $57100048.

12.3.5.3 PCI Bus Tests

12.3.5.3.1 Slot IDs

For each of the PCI slots, writing the slot number (1..4) plus 8 (the *PCIRST bit) to $60000007 asserts the appropriate IDSEL line from U11 to select the slot for access its configuration registers. An access to $4000000 accesses the configuration space of the card with the IDSEL asserted. At the first address ($4000000), there is a unique code for each PCI card brand and type. This test displays this value for all cards detected as present (as per test 5.1.1). This test thus checks PCI configuration accesses.

12.3.5.3.2 Test PCI Data Bits

$09 is written to $60000007 to select slot 1 for configuration. The configuration register at $4000002C is read-back and is used to perform a bit test on the data bits.

12.3.5.3.3 Test DRAM Data Bits

A bit test is performed on address $38000000 (the base address of the 8M of DRAM at U22 on the ESP-PCI card. These accesses are actually via the PCI bus which is decoded by U8 to generate the required control signals to U22 DRAM. The memory address is multiplexed by U7. During writes to the DRAM, the data from the PCI bus is passed via U7. During read from the DRAM, the data is driven and latched by U14,21,9,U15 and PCI control is latched by U10. These programmable devices are PCI compliant and are configured as 10 bit latches clocked by pin 1 and output enabled by pin 13.

12.3.5.3.4 DSP IVR Register Bit Test

The IVR register (interrupt vector register) at address $3C00000C is a read-back register in the Motorola 56002 at U17. This register is part of the 56002 host port. The data and address lines are connected to the DRAM lines and uses the same paths as for DRAM accesses. Decoding and control of the host port access is via U8.

12.3.5.4 DRAM Tests

The DRAM on the ESP-PCI at U11 appears at CPU address $38000000 to $387FFFFF. The PCI bus must not be in reset (i.e $60000007 register bit 3 set) for this DRAM to be accessable.

By analysing the results of these tests it is possible to determine whether there is an open, short or stuck bit.

12.3.5.4.1 Write All 0's

The DRAM is filled with $00000000 for its complete range and read-back.

12.3.5.4.2 Write All 1's

The DRAM is filled with $FFFFFFFF for its complete range and read-back.

12.3.5.4.3 Data Walking 0's

The DRAM is filled with $00000000 for its complete range. For each of the 32 bits, $38000000 is written with that bit low and all others high and checked. All other addresses are checked to be $00000000.

12.3.5.4.4 Data Walking 1's

The DRAM is filled with $00000000 for its complete range. For each of the 32 bits, $38000000 is written with that bit high and all others low and checked. All other addresses are checked to be $00000000.

12.3.5.4.5 Address Bits Low

For each DRAM address bit, $00000001 is written to the address with the address bit low and all others high. Other addresses are written as $00000000.

12.3.5.4.6 Address Bits High

For each DRAM address bit, $00000001 is written to the address with the address bit high and all others low. Other addresses are written as $00000000.

12.3.5.4.7 Inverted Walking Address

For each DRAM address, the inverted value of the address is written and verified.

12.3.5.5 PCI DMA Tests

For DMA operations to work (now that the PCI bus is verified to be oprational), the PCI slot arbitration must be working. All PCI arbitration is performed by U11 using signals *REQ0..6 and *GNT0..6 with *REQ0 granted the highest priority.

12.3.5.5.1 PCI DMA Memory to Memory

Half of the NCR SCSI card internal memory is filled with a random pattern and the other half filled with $FFFFFFFF. The NCR SCSI card is setup to use its own DMA controller to copy the random half to the $FFFFFFFF half.

12.3.5.5.2 PCI DMA DRAM to DRAM

Half of the DRAM is filled with a random pattern and the other half filled with $FFFFFFFF. The NCR SCSI card is setup to use its own DMA controller to copy the random half to the $FFFFFFFF half.

12.3.5.5.3 PCI DMA DRAM to DRAM Burst

Half of the DRAM is filled with a random pattern and the other half filled with $FFFFFFFF. The NCR SCSI card is setup to use its own DMA controller with long bursts to copy the random half to the $FFFFFFFF half.

12.3.5.6 DSP WFM Interface Tests

The 56002 DSP is loaded via the host port. For these tests, the /dd/usr/esppci/pcidiag.lod program is loaded into the DSP.

12.3.5.6.1 Starting DSP

The test program is loaded via the host port. Any value written to the host port HD registers (4 bytes, one each at $3C000010 (msb) $3C000014, $3C000018 and $3C00001C), is read back from these addesses. This is a simple way to prove that the DSP loaded correctly.

12.3.5.6.2 DRAM DSP Write, CPU Read

A random pattern is written to the ESP-PCI DRAM using the DSP test program and verified by the CPU.

12.3.5.6.3 DRAM CPU Write, DSP Read

A random pattern is written to the ESP-PCI DRAM using the CPU verified by the DSP test program.

12.3.5.6.4 WFM DSP Write, CPU Read

A random pattern is written to the DCC memory using the DSP test program and verified by the CPU.

12.3.5.6.5 WFM CPU Write, DSP Read

A random pattern is written to the DCC memory using the CPU verified by the DSP test program.

12.3.5.7 DSP DMA List Tests

The /dd/usr/esppci/pciwfm.lod program used for normal disk recorder operation is loaded for these tests. The DSP polls the ESP-PCI DRAM for a liked list of DMA commands to transfer data to and from the WFM and ESP-PCI DRAM.

12.3.5.7.1 DSP Software

After the DSP is loaded, $97 is written to the command register at $3C000014. Once this value has changed to $17, then the command is complete and the software version number is visible as a 24 bit number spread across addresses $3C000014, $3C000018, $3C00001C as a 12 bit revision and 12 bit version number. For Rev 5 ESP-PCI cards this should be v13.2.

12.3.5.7.2 DSP DMA DRAM to DCC

The ESP-PCI dram is filled with random data and a linked list command instructs the DSP to copy this data to the DCC. Once complete, the CPU checks the transfer.

12.3.5.7.3 DSP DMA DCC to DRAM

The DCC memory is filled with random data and a linked list command instructs the DSP to copy this data to the ESP-PCI DRAM. Once complete, the CPU checks the transfer.

12.3.6 References

1. Spanner User Manual, Newbridge Microsystems, 1995.

2. Lattice Semiconductor Data book 1996,
   Lattice Semiconductor Corporation, 1996.

3. Cypress Data Book - Memories, DataCom, FCT Logic,
PC products, Cypress Semiconductor, May 1995.

4. PCI Local Bus Specification - Revision 2.1,
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5. PAL Devices Data Book and Design Guide 1996,
Advanced Micro Devices Inc, 1996.

6. QuickSwitch Products, Quality Semiconductor Inc, 1995.

7. 1995 DRAM Data Book, Micron Technology Inc, 1995.

8. DSP56002/DSP56L002 24 Bit Digital Signal Processor -
Technical Data Document number DSP56002/D Rev 2, Motorola Inc 1995.

12.4 ESPPCI DSP Field Diagnostics

12.4.1 Introduction

The pcidsp diagnostics are to be used after the pcidiag diagnostics have been run and passed successfully.

12.4.2 System requirements

To execute the diagnostics, the following is required.

A hard disk with v15.1.04 or higher software installed.

MFX3^{plus} PCI system at least one ESPDCC installed.

12.4.3 Running the diagnostics

Boot to OS9. Once booted, you should see the mfx: prompt.

Type: pcidsp -lrw.

The tests will run and upon successful completion, you will see:

```
testing dsp linked list command processing ... PASS
testing read from wfm ram to pci dram ........ PASS
testing read from pci dram to wfm ram ........ PASS
```

Any errors will be displayed on the screen.

12.4.4 Command Details

The pcidsp diagnistic is executed with command options. These options can be seen by using pcidsp -?. You will see:

```
pcidsp  v1.4  -  ESP-PCI  DSP  diagnostics
```

usage: pcidsp [options]

options:

-l	dsp linked list processing test
-r	read from WFM memory test
-w	write to WFM memory test
-z	verbose output level (extra -z for more)
-f=<file>	load dsp with <file>

12.4.4.1 -l Option

All of the available PCI DRAM (U22) is allocated to the test and a linked list of commands is written into this memory by the WX. The 56002 DSP (U20) is instructed to execute the linked list of commands by the WX via the DSP host port which is interfaced to the PCI bus. The linked list is approx 131000 no-operation commands. As each packet is processed, the DSP writes status back to the command packet and the WX checks that the DSP executes all commands.

This test effectively tests the DSP's ability to read and write to PCI DRAM memory.

12.4.4.2 -r Option

All of the available PCI DRAM (U22) is allocated to the test and a single command packet is written to the PCI DRAM to instruct the DSP to copy from WFM memory on the first DCC to the PCI DRAM memory. The WX fills the source and destination with a different random pattern and instructs the DSP to start the command via the host port. The WX waits for the copy to complete and then checks the validity of the copy.

This test checks reads from WFM memory by the DSP.

12.4.4.3 -w Option

All of the available PCI DRAM (U22) is allocated to the test and a single command packet is written to the PCI DRAM to instruct the DSP to copy from PCI DRAM to WFM memory on the first DCC. The WX fills the source and destination with a different random pattern and instructs the DSP to start the command via the host port. The WX waits for the copy to complete and then checks the validity of the copy.

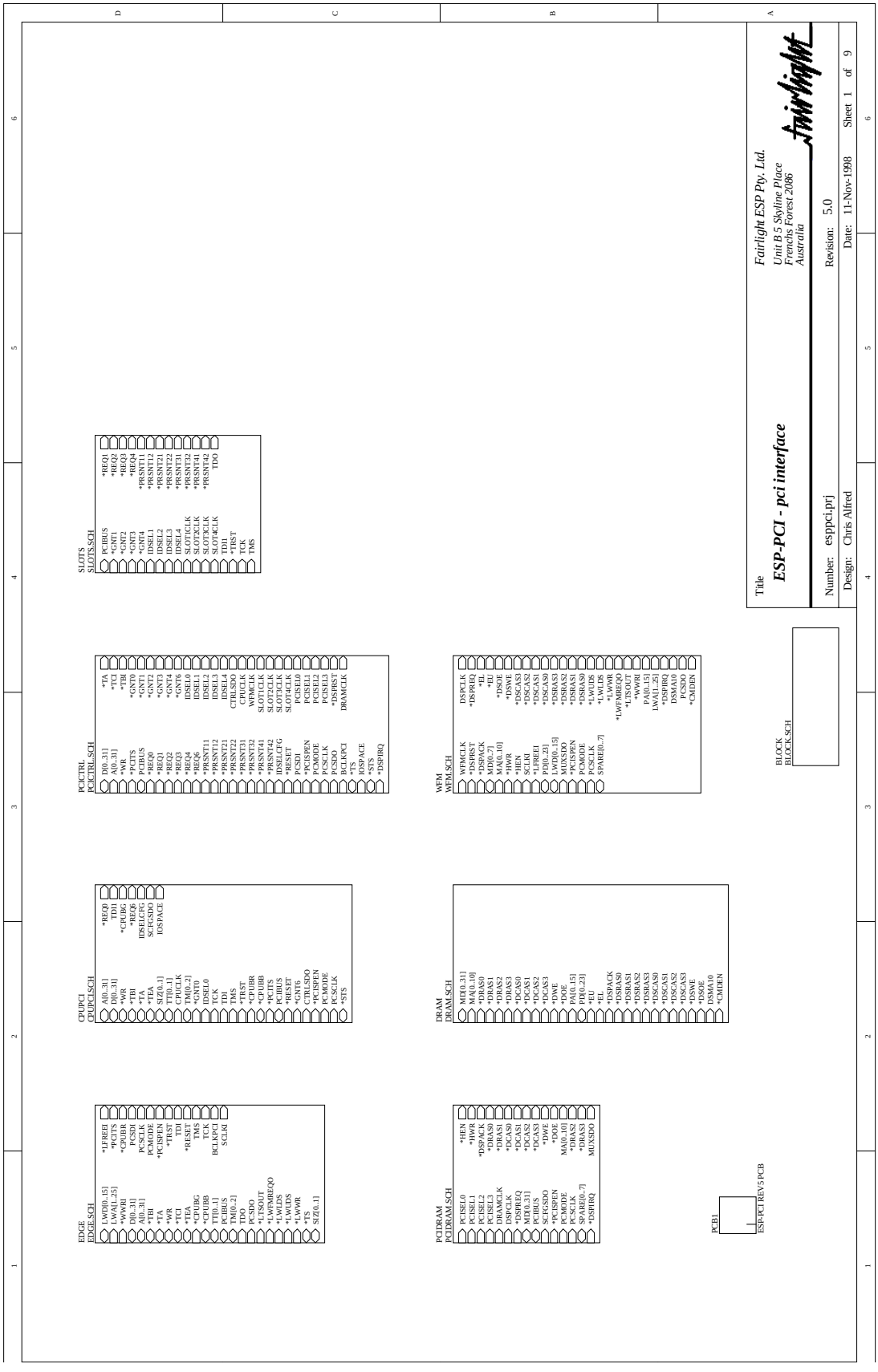
This test checks writes to WFM memory by the DSP.

12.4.4.4 -z Option

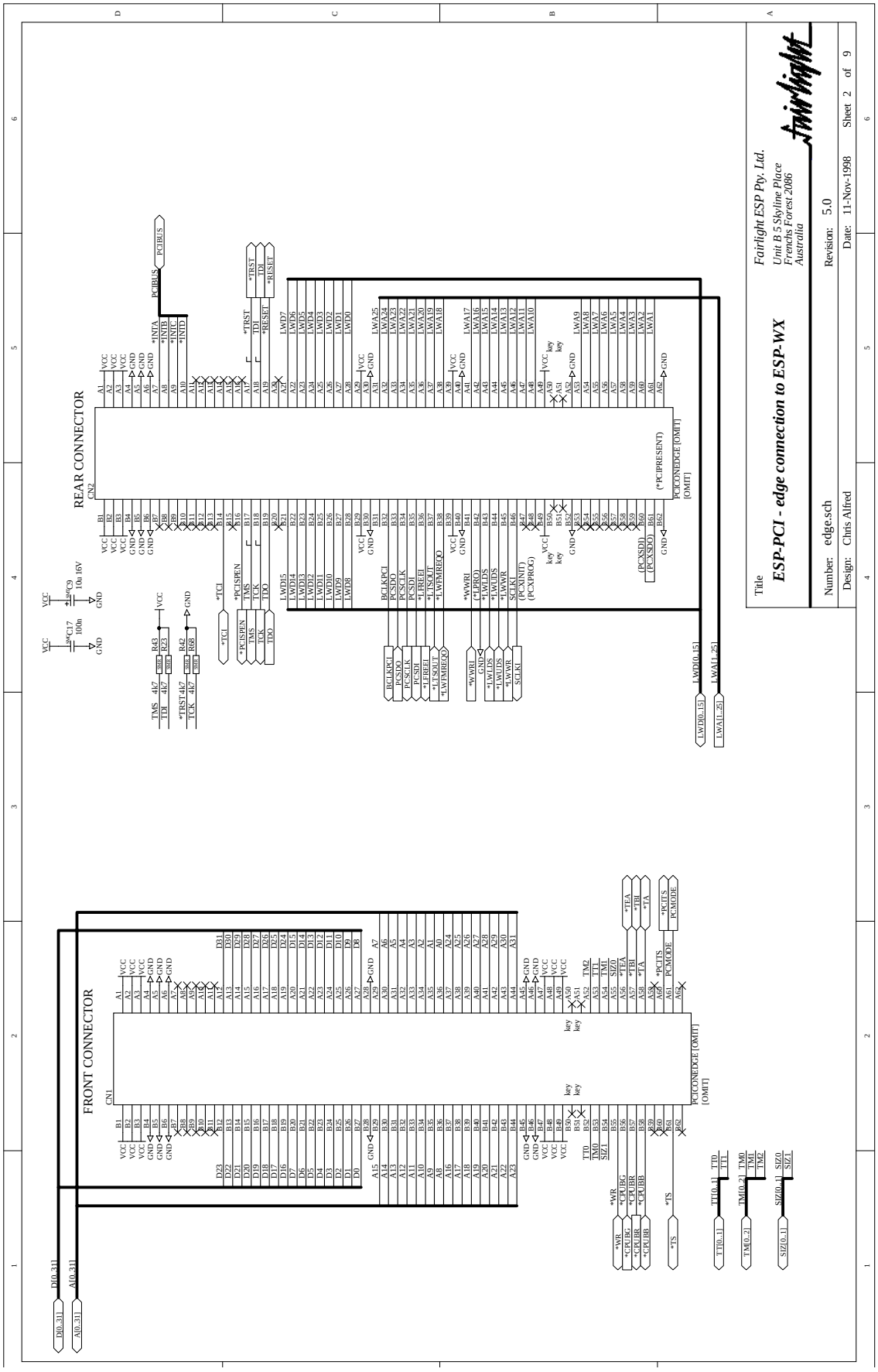
When this option is used more information regarding the progress of test is displayed. More -z options can be added for more detailed information.

12.5 ESPPCI SCHEMATICS

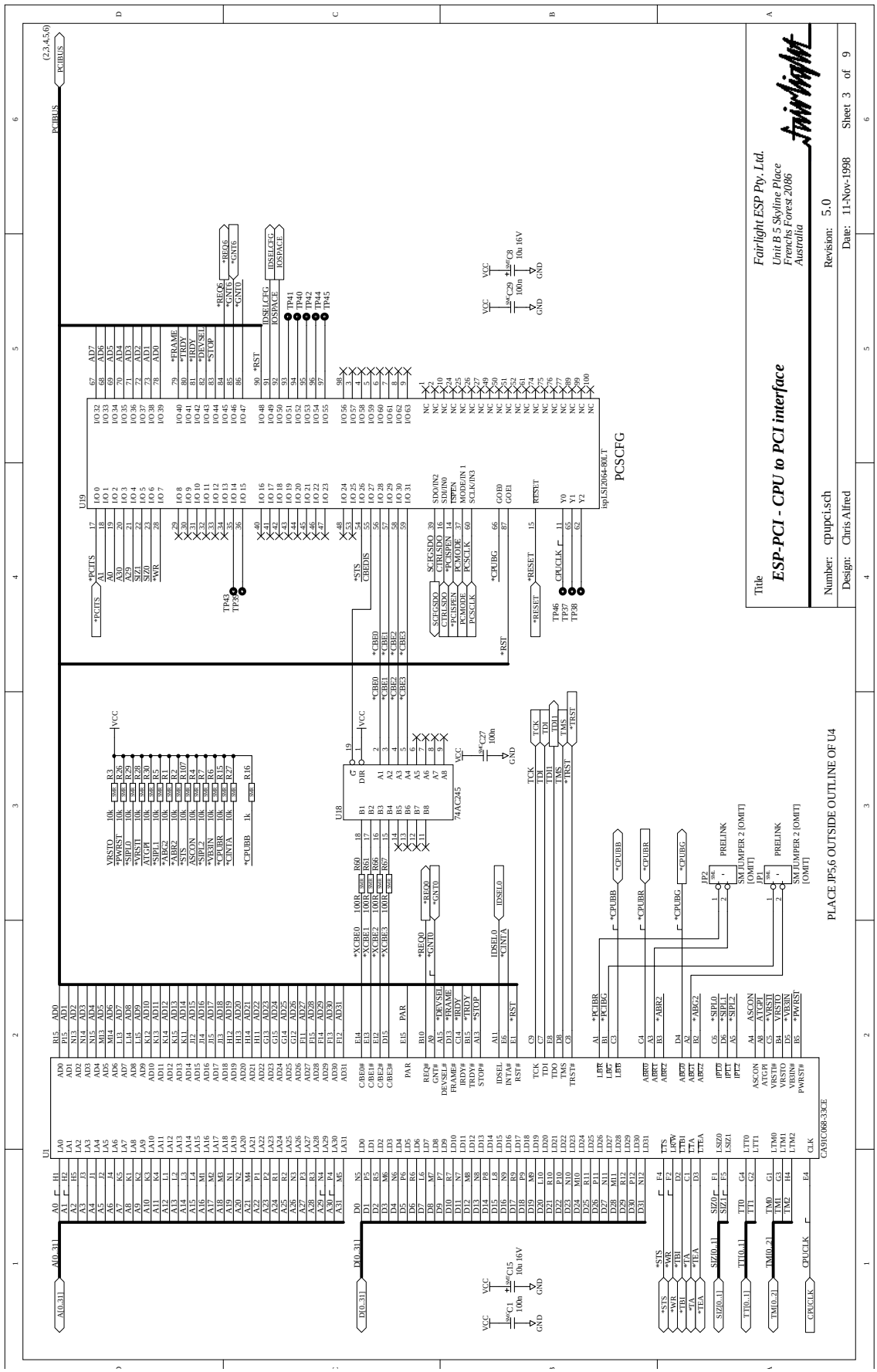
12.5.1 ESPPCI INTERCONNECTING DIAGRAM



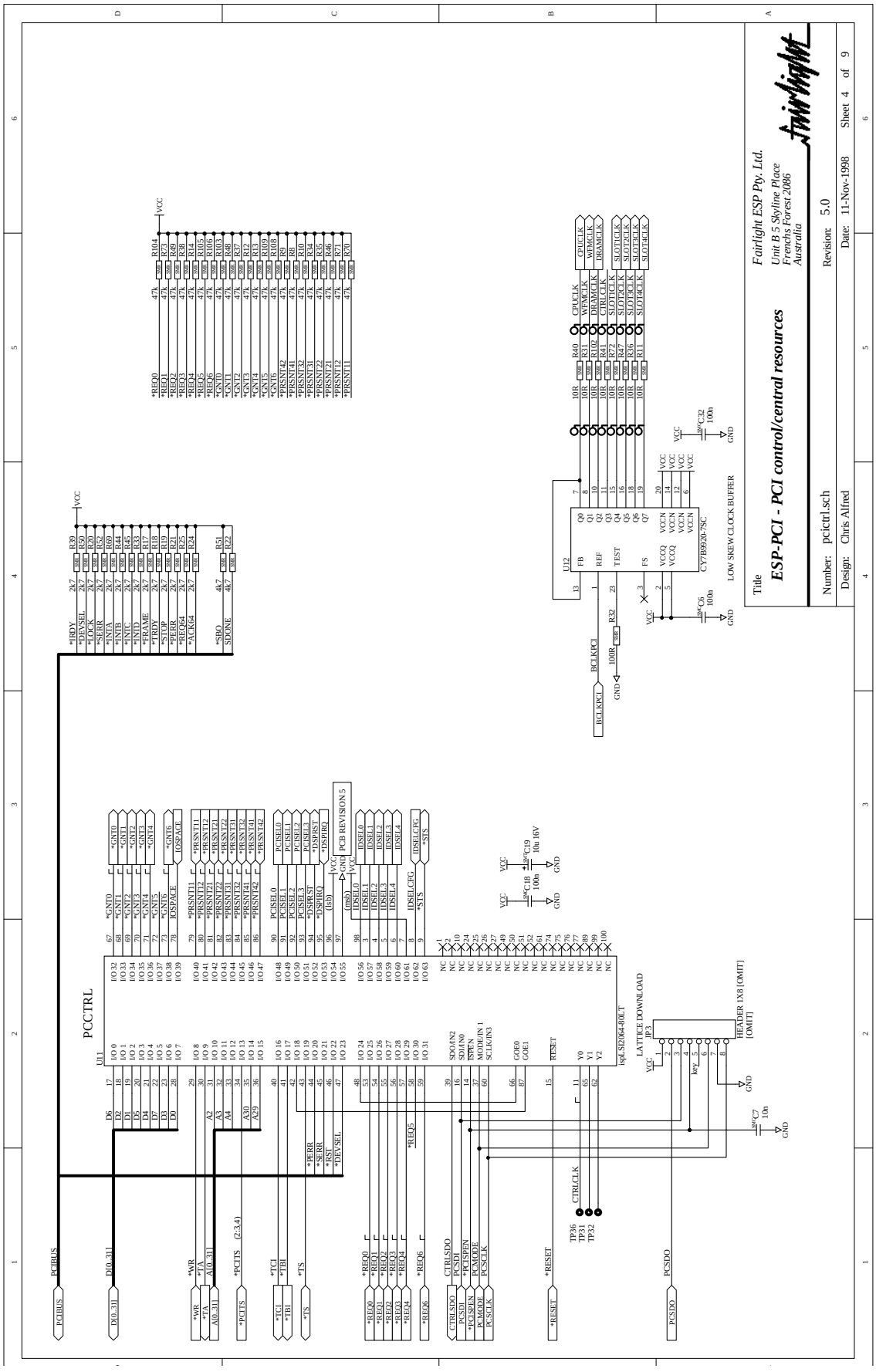
12.5.2 EDGE CONNECTION TO ESPWX



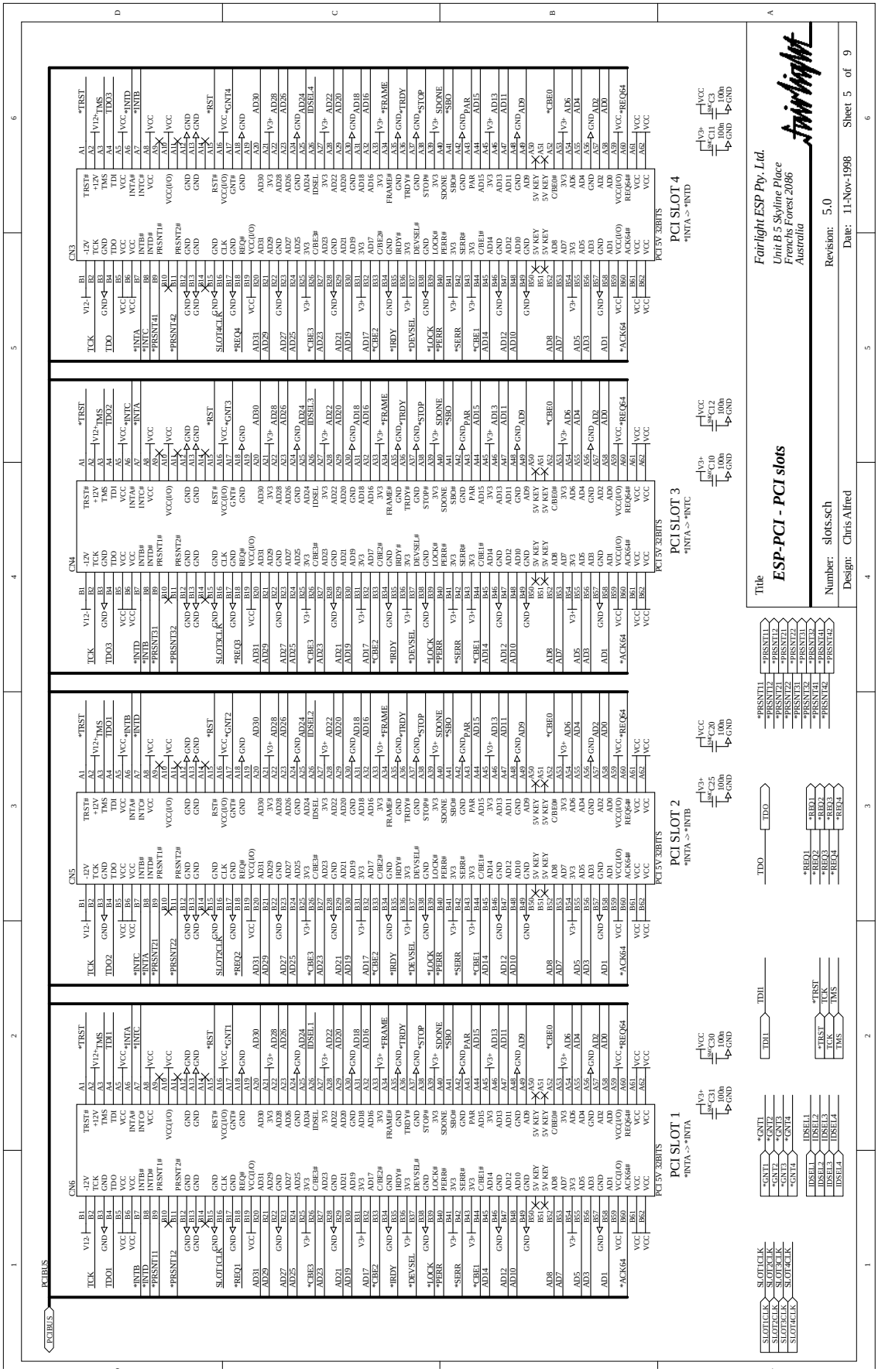
12.5.3 CPU to PCI Interface



12.5.4 PCI CONTROL/CENTRAL RESOURCES

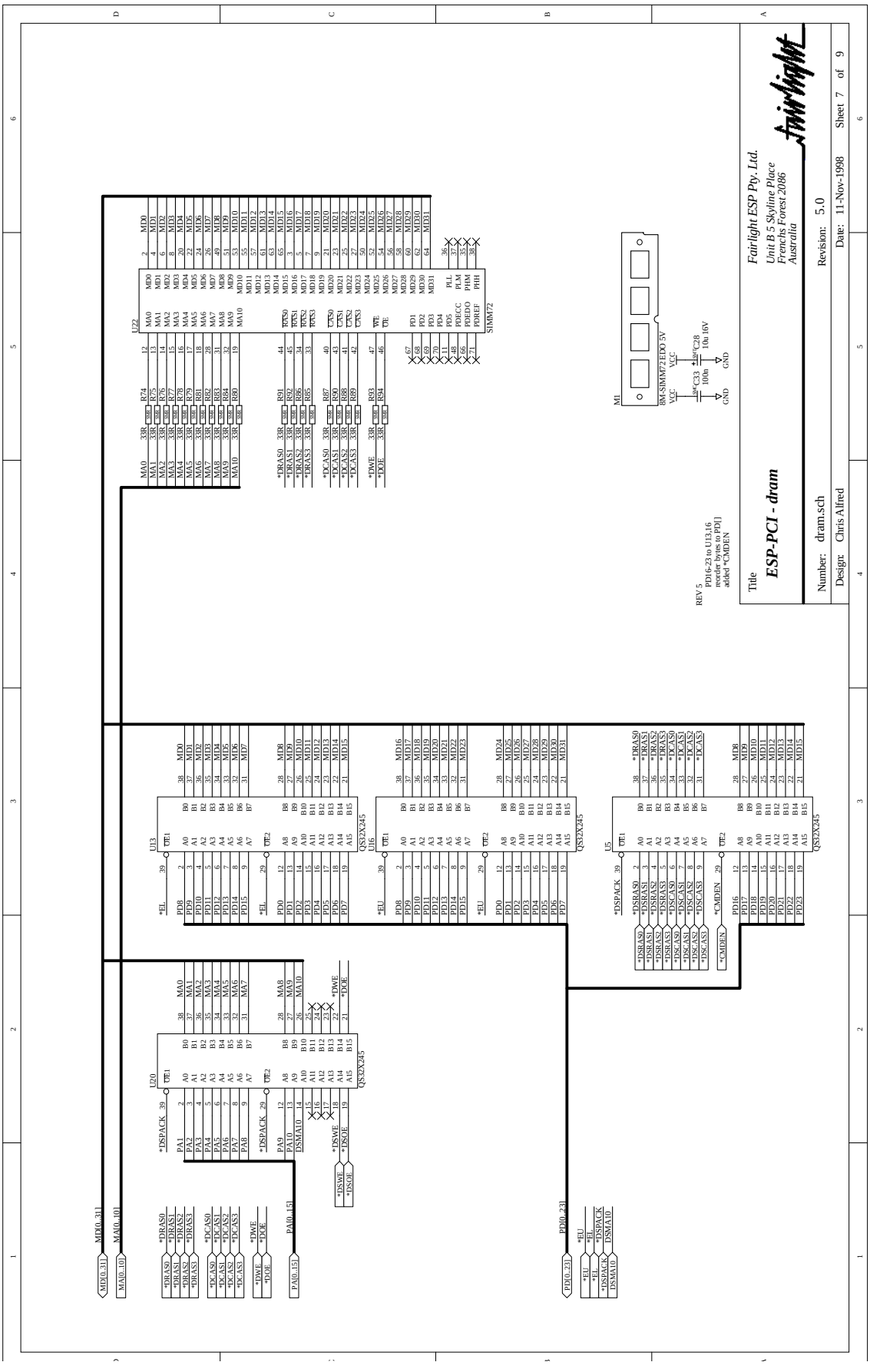


12.5.5 PCI SLOTS

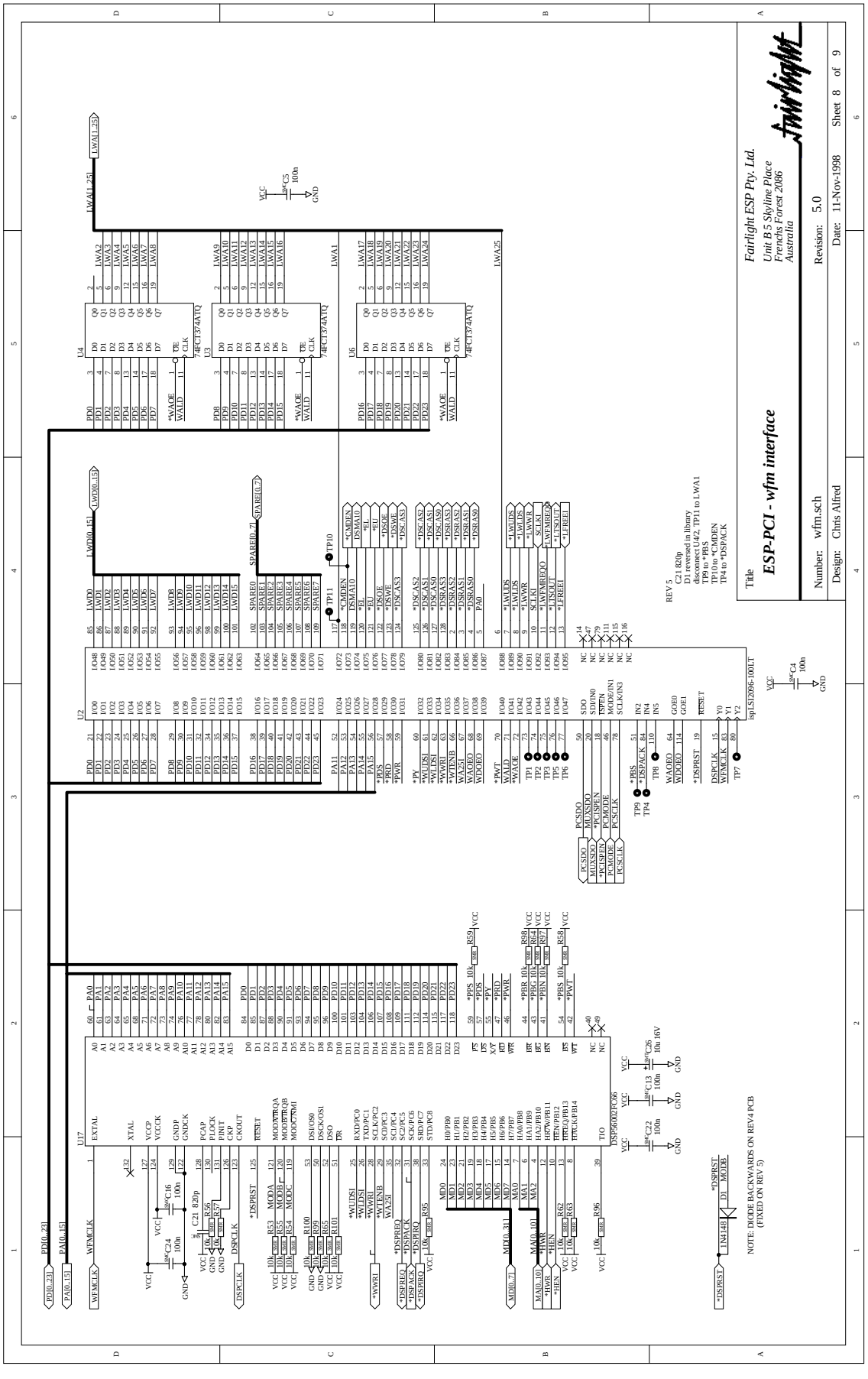


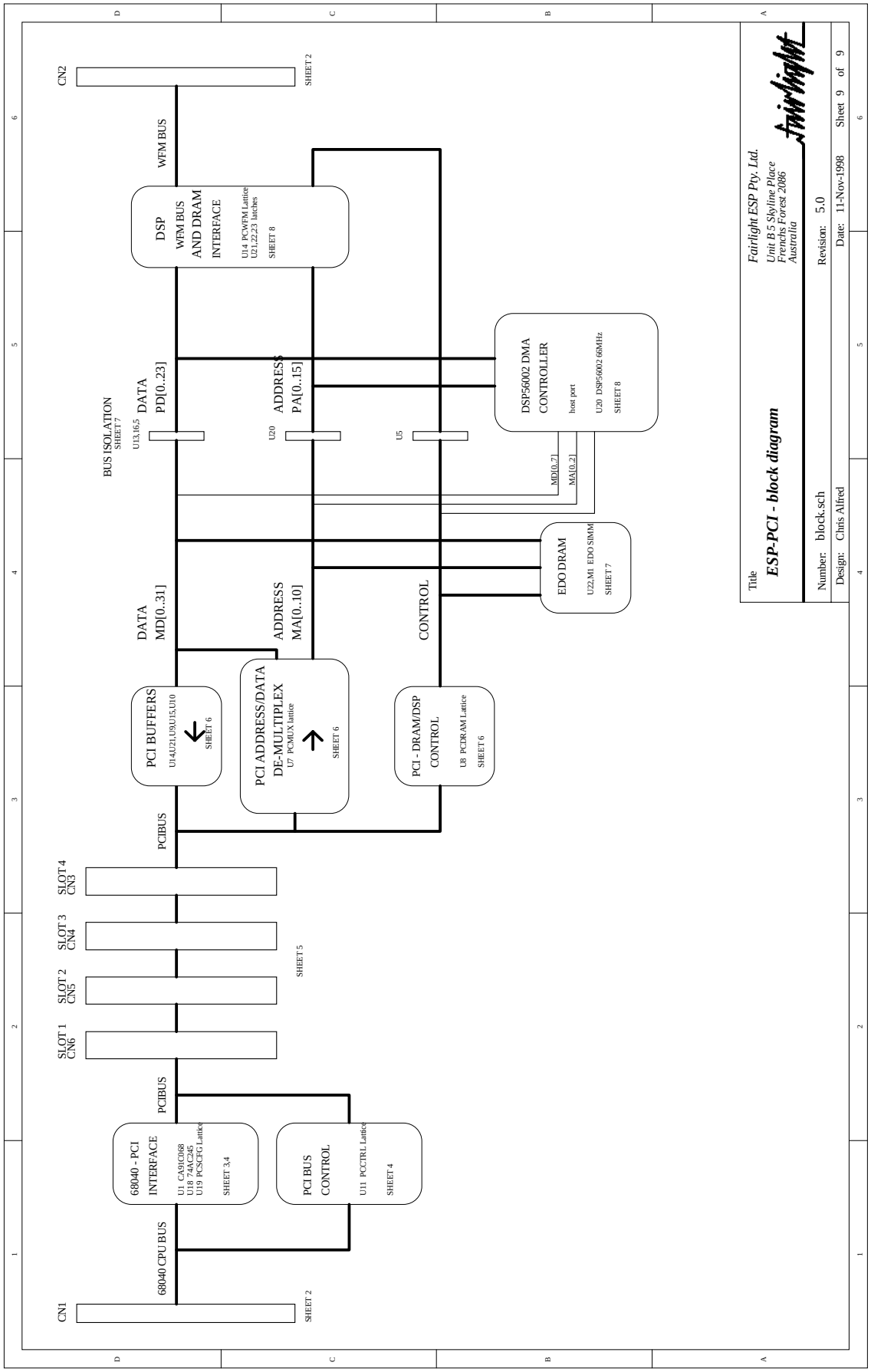
12.5.6 PCI DRAM INTERFACE

12.5.7 PCI DRAM



12.5.8 WFM Interface




CN2
SHEET 2
WFM BUS
DSP
WFM BUS
AND DRAM
INTERFACE
U14 PCWFM Lattice
U21,22,23 latches
SHEET 8
DSP56002 DMA
CONTROLLER
host port
U20 DSP56002 66MHz
SHEET 8
BUS ISOLATION
SHEET 7
U13,16,5
DATA
PD[0..23]
U20
ADDRESS
PA[0..15]
U5
MD[0..7]
MA[0..2]
EDO DRAM
U22,M1 EDO SIMM
SHEET 7
DATA
MD[0..31]
ADDRESS
MA[0..10]
CONTROL
PCI BUFFERS
U14,U21,U9,U15,U10
SHEET 6
PCI ADDRESS/DATA
DE-MULTIPLEX
U7 PCMUX lattice
SHEET 6
PCI - DRAM/DSP
CONTROL
U8 PCDRAM Lattice
SHEET 6
PCIBUS
SLOT 4
CN3
SLOT 3
CN4
SLOT 2
CN5
SLOT 1
CN6
SHEET 5
PCIBUS
68040 - PCI
INTERFACE
U1 CA91C068
U18,19 AM2245
U19 PCSCFG Lattice
SHEET 3,4
PCI BUS
CONTROL
U11 PCCTRL Lattice
SHEET 4
68040 CPU BUS
CN1
SHEET 2
Title
ESP-PCI - block diagram
Number: block.sch
Revision: 5.0
Design: Chris Alfred
Date: 11-Nov-1998
Sheet 9 of 9
Fairlight ESP Pty. Ltd.
Unit B 5 Skyline Place
Frenchs Forest 2086
Australia
fairlight

12.6 PCI SCSI Card

The SCSI Controller approved for use with the Fairlight MFX3plus is the SYMBIOS SYM8100S (earlier product code was previously NCR8100S).

This controller uses the SYMBIOS (NCR) PCI to SCSI chipset 53C810.

Identification of the controller can be performed by visual inspection and the following routine should be followed:

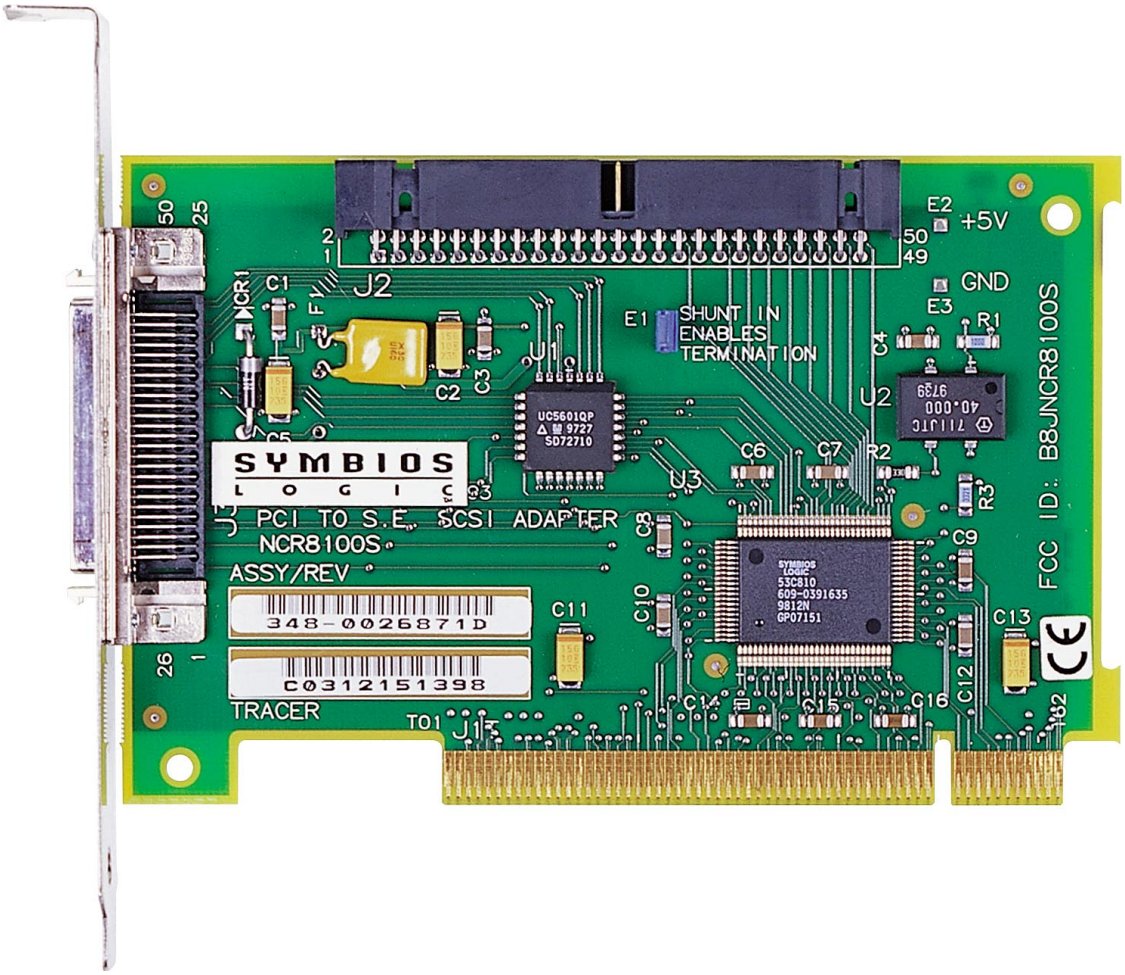
1. Verify that the product details located on the component or solder side of the SCSI controller card corresponds to model listed above.

2. If the internal SCSI cable is a single cable that ends at the SCSI card, ensure that the jumper that enables termination of the SCSI card is inserted. This will be the case with nearly all newer MFX systems.

   In the case of upgraded older systems, the SCSI cable may loop back to a second SCSI connector on the rear panel. In this case, the termination jumper should be removed, and Active teminators used at the end of each of the SCSI chain.

   The termination resistor should also be removed if the high-density connector is used for diagnostic purposes.

3. Ensure that the 50-way IDC connector on the cable being used for connecting SCSI drives to the controller is clean and that no pins are damaged or bent.



SYMBIOS Model SYM8100S PCI SCSI Adaptor

12.7 PCI 100BaseT Card Considerations

The PCI network adapter card approved for use in MFX3^{plus} is a 100BaseT controller manufactured by Intel. Depending on the model and manufacturing date, the actual layout of the PCB and number of chips mounted on the card might vary.

Currently, only network controllers based on Intel i82557 or i82558 chipsets are supported by MFX3^{plus}. Use of PCI network cards not approved by Fairlight ESP is not recommended.

The original i82557 Intel chipset has been upgraded to i82558 and is 100% compatible with the earlier one. However, this might not be the case in the future.

Identification of the PCI network adapter card is performed by the following routine:

1. Check that the rear panel of the controller has at least one RJ45 data connector.

2. Check the labelling on the rear panel. Different models will have different text. The number of LEDs will vary from 1 to 3 (some or all of these LINK, ACT, 100TX). Other text located on the rear panel might include INTEL PRO/100 or PRO100/10.

3. Inspect the LAN controller chipset - ensure the chipset used on the card is i82557 or i82558. Typically, the LAN chipset would be the largest IC on the card.

4. Look for the label that lists ethernet address, serial number and board ID number (PWA) assigned to the card. The ethernet address consists of 12 hexadecimal digits. A bar code would be printed above the numbers.

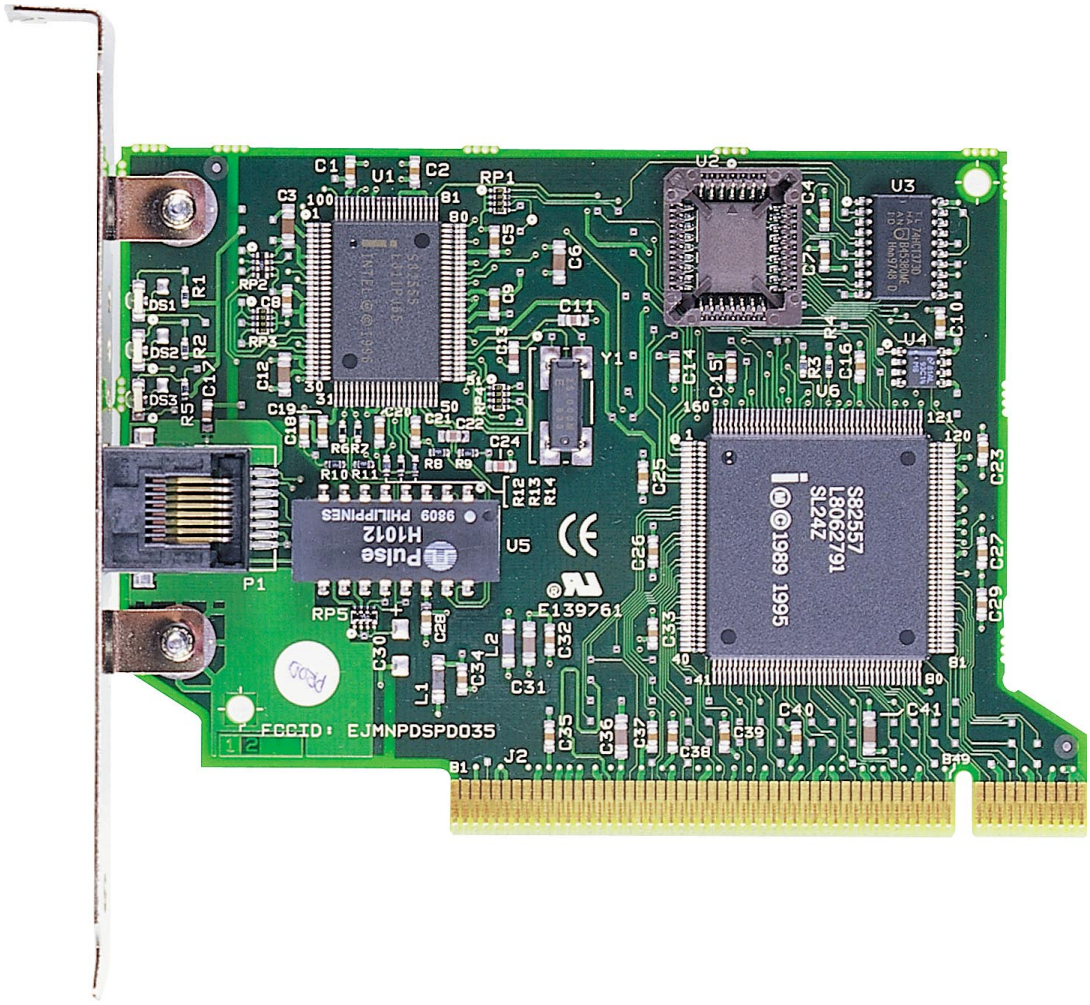
Example: 00A0C98F93A1 38713 678400-001

The last number (678400-001) is the manufacturer's board ID number and in general the first six digits must correspond to the ID described in the table below. If not, please contact Fairlight ESP or your local Authorised Fairlight dealer or technical support engineer. Alternatively, the latest technical information concerning Intel products can be found at:

http://support.intel.com/support/network/

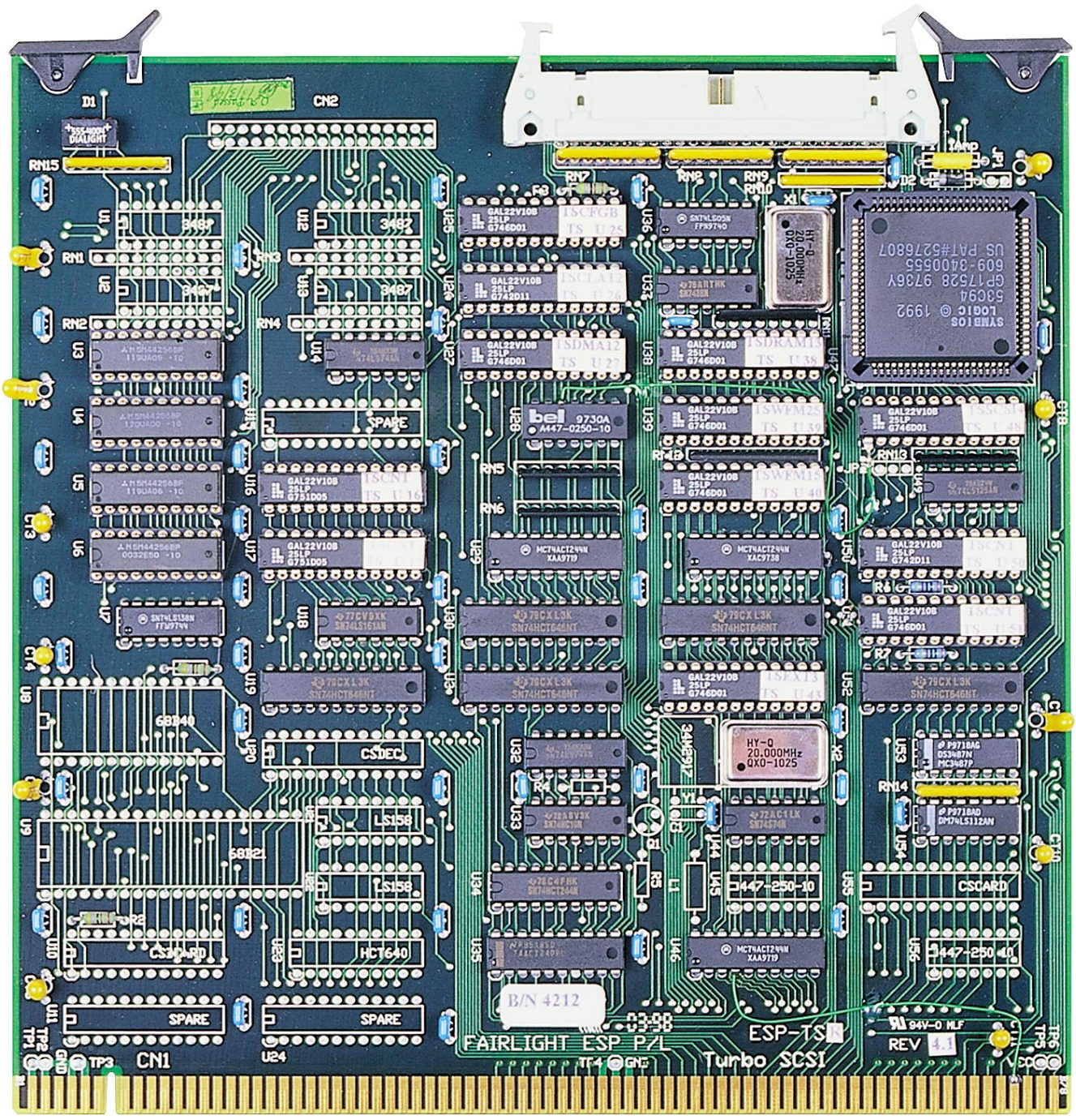
The following table lists currently approved Intel LAN controllers:

Board ID Number (PWA)	Intel Part Number	Additional Information
352509-xxx 661949-xxx 667280-xxx 678400-xxx	PILA8465B	EtherExpress™ PRO/100B PCI adapter(TP) Model B, Full Duplex, 3 LED's
668081-xxx 689661-xxx	PILA8460	PRO/100+ PCI (TP) 82558, Full Duplex, 3LED's

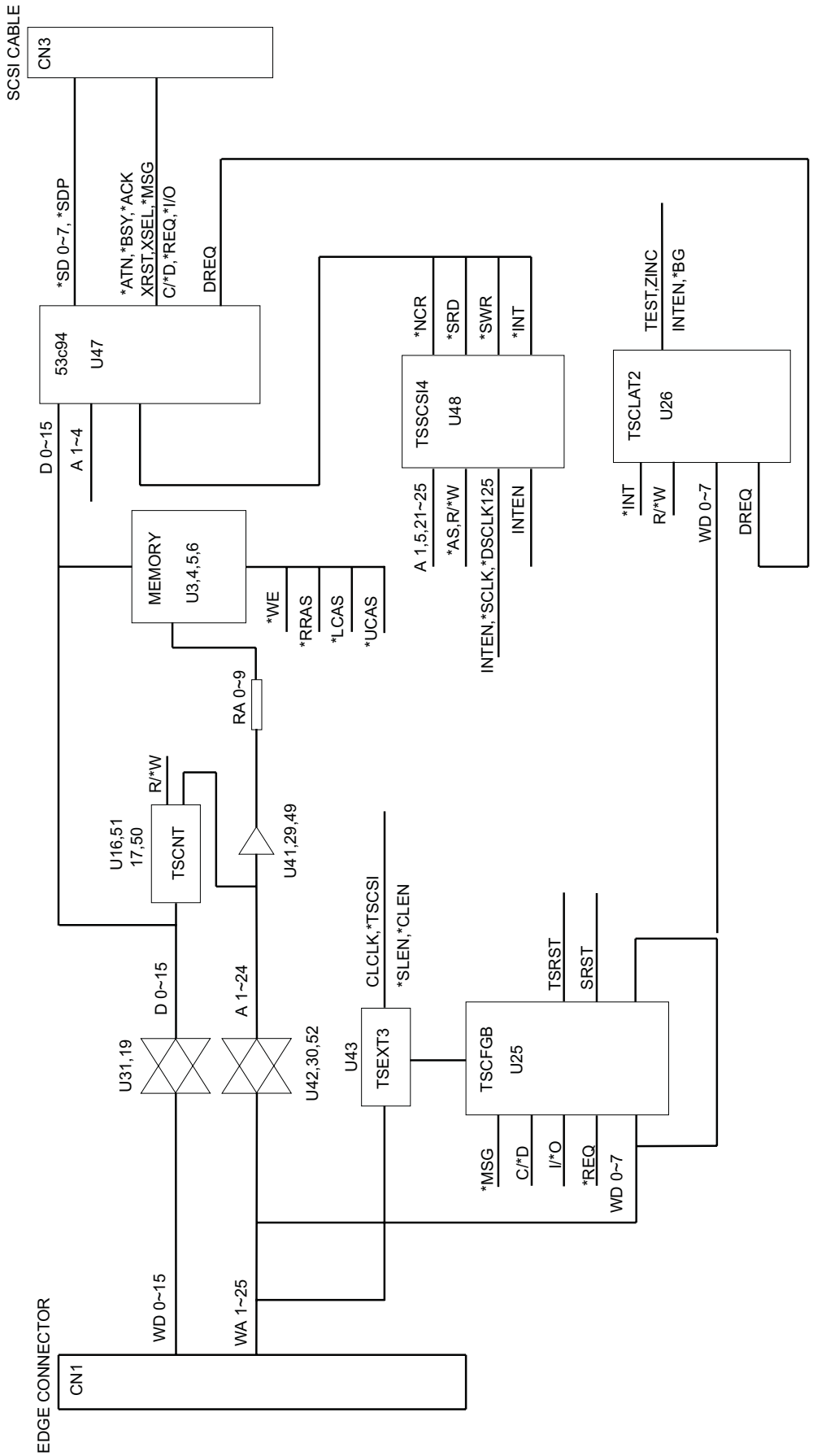


EtherExpress Model PRO/100B PCI 100BaseT Network Adaptor ID 678400-001

13.0 ESPTSR Turbo SCSI Card



13.1 ESPTSR Block Diagram



TSR BLOCK DIAGRAM

13.2 ESPTSR Circuit Description

13.2.1 Terminology

TSCSI	ESPTSR Turbo SCSI Card
WX	Waveform Executive PCB
WFMBUSS	Waveform Bus
WFMRAM	Waveform RAM

Signals which have been buffered are prefixed by 'B' (eg. RA once buffered becomes BRA).

Signals which have been latched are prefixed by 'L'

Active low signals are preceded by (*)

13.2.2 Overview

The Turbo SCSI card (TSCSI) main features are:

(1) 512k bytes of on card DRAM;

(2) The ability to DMA 16 bit SCSI data directly to WFMRAM without affecting the WX operation or speed;

(3) A WFMBUSS time slice chaining system to allow multiple Waveform Bus masters. The Turbo SCSI card transfers SCSI data, via its own DMA path, directly to the Waveform Buss.

13.2.3 Detailed Description

The TSCSI card hardware resides in the top 8MB of Waveform memory (WX addresses 5000000..5FFFFFF).

Throughout this documentation, the addresses are referred to as the hexadecimal address accessed by the Waveform Executive. To convert the addresses to the physical address which appears on the Waveform Buss, subtract 2000000.

13.2.3.1 TSCSI Timing Source

(see 13.4.2 ESPTSR Edge Connector, 13.4.4 ESPTSR Waveform Bus Interface schematics)

All timing for the TSCSI is generated from *SCLK (U35 74HCT240) delayed by U28 (447-250-10 delay line) to produce delayed images of * SCLK. The notation used to name the delayed *SCLK signals is to prefix the name with 'D', and suffix the name with the delay (eg. *DSCLK100 is *SCLK delayed by lOOnS).

13.2.3.2 Waveform Bus Decoding

(see 13.4.4 ESPTSR Waveform Bus Interface schematic)

The ESPTSR card resides in the 5800000..5FFFFFF address range.

5800000 59FFFFF TSCSI on-board DRAM

5C00000 5C0001F	NCR SCSI chip
5C00020 5C00023	TSCSI DMA address registers
5F00001	TSCSI control read/write register
5F00003	TSCSI status register

For accesses in the range 5800000..5EFFFFF, TSEXT3 (U43 22V10) asserts the *TSCSI signal to indicate that the data is for on-card (internal) devices. The 8 bit control and read-back status registers are implemented as two TSCLAT PALS (U25,U26 22V10). As the internal devices cannot be accessed while the TSCSI is transferring SCSI data via DMA, the TSCLAT PALS appear external to the card (directly on the WFMBUSS) to allow TSCSI transfers to be controlled at any time (eg. aborting a TSCSI DMA transfer).

Writes to the control register addresses assert CLCLK (control latch clock) low during the low period of TSEXT3 pin 13 (*SCLK). The data present on WDO..WD7 is latched by the TSCLAT Pals on the rising edge of CLCLK. Reads from the control register assert *CLEN (control latch enable) allowing TSCLATs to enable the previously written control data on to WDO..WD7. *CLEN is asserted for 300nS starting at the rising edge of TSEXT3 pin 1 (*DSCLK100).

The control register bit assignments and their active state functions are as follows

Bit 7	[Spare]	
Bit 6	[Spare]	
Bit 5	TSRST	TSCSI interface reset
Bit 4	SRST	SCSI buss reset
Bit 3	TEST	Enable Turbo SCSI DMA test mode
Bit 2	ZINC	Zero increment DMA addresses
Bit 1	INTEN	Enable TSCSI interrupts to WS (Level6)
Bit O	*BG	TSCSI buss granted to WFMBUSS masters

A read from the status register asserts *SLEN to allow the TSCLATs to enable the data present on their status input pins to WDO..WD7 for 300nS starting at the rising edge of TSEXT3 pin 1 (*DSCLK100).

TSCSI status bits:

Bit 7	*MSG	SCSI buss *MSG signal
Bit 6	C/*D	C/*D
Bit 5	V*O	V*D
Bit 4	*REQ	*REQ
Bit 3	[Spare]	
Bit 2	*INT	TSCSI interrupt request
Bit 1	R/*W	TSCSI DMA transfer direction
Bit0	DREQ	NCR DMA request

13.2.3.3 STATUS LEDS

(see 13.4.4 ESPTSR Waveform Bus Interface schematic)

The four stares LEDs report the following stares when lit:

(TOP LED)	*BG	TSCSI in DMA transfer
*VTERM		SCSI buss termination voltage present
*INT		No TSCSI interrupt request pending
RESET		TSCSI card in reset

13.2.3.4 Waveform Bus Interface

(see 13.4.4 ESPTSR Waveform Bus Interface schematic)

All Waveform Buss transfers are controlled by the TSWFM15 (U40 22V10) and TSWFM25 (U39 22V10) PALS. TSWFM15 converts the WFMBUSS control signals to internal TSCSI control signals during non-DMA transfers by WFMBUSS buss masters. TSWFM25 handles the WFMBUSS arbitration and generates the WFMBUSS control signals for the TSCSI DMA transfer.

The address buss is buffered by bidirectional 74HCT646 (U42,U30,U52) buffers to allow both WFMBUSS masters to accesses the TSCSI internal devices; and the TSCSI to DMA to WFMRAM by asserting its own addresses. The *ADIRN selects the direction of address transfers (0 = WFMBUSS to TSCSI); and *AEN is asserted to enable address transfers

The data buss is buffered by bidirectional 74HCT646 (U31 ,U19) buffers. The direction is controlled by *DDIRN (O = WFMBUSS to TSCSI); and enabled by *DEN.

13.2.3.5 Waveform Bus Free Slice Detection

(see 13.4.4 ESPTSR Waveform Bus Interface schematic)

The time slices on the WFMBUSS are shared by all WFMBUSS masters with the following priorities:

Highest	Refresh cycles (*RPEND asserted)
WS accesses	(*WSWFM asserted)
TSCSI	(*TSOUT asserted)
Lowest	Future buss masters

U10C (74HC10) detects when no requests higher than the TSCSI card are pending. If this is the case, then *TSIN is asserted to indicate a free WFMBUSS slice. If the TSCSI is not requesting a WFMBUSS access for SCSI DMA, then *TSOUT is asserted to the WFMBUSS. In order for multiple masters to exist on the WFMBUSS, *TSOUT (which becomes *TSIN) would be chained in a similar way. On the rising edge of *SCLK, TSCSI samples *TSIN to determine whether slices are free. *TSOUT low at the rising edge of *SCLK indicates that the slice is not used by any WFMBUSS masters.

13.2.3.6 Internal DRAM

(see 13.4.2 ESPTSR Edge Connector, 13.4.5 ESPTSR DRAM schematics)

Accesses in the range of 5800000..59FFFFF, and refresh cycles (*WREF=O) are detected and latched by TSDRAM13 (U38 22V10) on the rising edge of TSDRAM13 pin 1 (*DSCLK125). If any accesses must be held off due to a refresh cycle, then *DTACK will be held inactive - note that only TSCSI DMA directly to its internal DRAM will ever be held off in this way as there is no WFMBUSS activity during refresh cycles.

CAS-before-RAS refreshing. The *MUX signal is buffered by U46 (74HCT244) to generate *DRA to enable the row address via U41 (74ACT244) and U49C,D (74LS 125); and also inverted by U35B (74HCT240) to generate *DCA to enable the column address via U29 (74ACT244) and U49A,B (74LS 125).

TSCSI local DRAM is configured as 256k x 16bits (using 44256s) or 1M x 16 bits (using 441024s). JP 1 is used to select the type of DRAMs used:

Pins 1,2 shorted	441024 1M x4bit DRAMs
Pins 2,3 shorted	44256 256k x 4bit DRAMs

The Turbo SCSI card normally has 256k x 16 bits installed which will appear in the address range 5800000..587FFFF.

13.2.3.7 DMA Address Registers

(see 13.4.6 ESPTSR SCSI Interface schematic)

16 bit writes to 5C00020 (MSW) and 5C00022 (LSW) load the start address for TSCSI DMA transfers into the TSCNT DMA address counters (U16,U51,U17,U50 22V10). The 32 bit value written to the DMA counters is the WAVEFORM BUSS WORD ADDRESS (ie. WS address minus 2000000 and shifted right 1 bit), with bit 31 the DMA DMA direction (0 = WRITE to WFMRAM). If the DMA is to TSCSI internal DRAM, the DMA will be directly to the DRAM without using WFMBUSS slices.

Writes to the DMA address registers are latched on the rising edge of *DMAHI or

*DMALO when *DMALD is low

NOTE: the TSCSI is incapable of transferring DMA data directly to WX local memory (it is impossible), and so must be DMAed to TSCSI internal DRAM and later DMAed by the WX to its own local memory.

13.2.3.8 SCSI Data DMA

(see 13.4.6 ESPTSR SCSI Interface schematic)

The sequence used to setup a TSCSI DMA transfer is:

(1) Load the DMA address registers with the start address and DMA direction;

(2) Setup the NCR SCSI chip for the transfer (the DMA transfer count is held in the NCR chip);

(3) Set *BG=I to start DMA process;

(4) wait for TSCSI interrupt;

(5) set *BG=0.

*BG may reset low prematurely to halt a DMA transfer.

While *BG is high, TSDMA12 (U27 22V10) samples the NCR DMA request signal (DREQ) on the rising edge of its pin 1 (*DSCLK225). If such a request is detected, then TSDMA will assert its acknowledge signal (*DACK), *AS, *UDS, *LDS, *DMAHI and *DMALO. *DACK will be held low until a *DTACK signal is detected during *SCLK=0 indicating a successful transfer to the internal DRAM (via TSDRAM) or WFMBUSS (via TSWFM25). All DMA transfers are synchronised to the WFMBUSS slice and are 16 bits wide. A successful DMA transfer terminates with *DACK being raised, and simultaneously, *DMAHI and *DMALO will go high to clock the DMA address counters to the next address. If the ZINC (zero increment) control bit is set, then the address counters will not increment their address

13.2.3.9 SCSI Bus Interface

(see 13.4.6 ESPTSR SCSI Bus Interface schematic)

The NCR53C94 is accessed on even address boundaries in the range SC00000..SC0001F as decoded by TSSCSI14 (U48 22V10). Accesses assert *NCR and one of *SWR (write to NCR SCSI chip) or *SRD (read from NCR SCSI chip). As the NCR53C94 is an INTEL type chip, the high and low bytes of the data are swapped to conform with the MOTOROLA high-byte-at-low-address format used by MFX3plus.

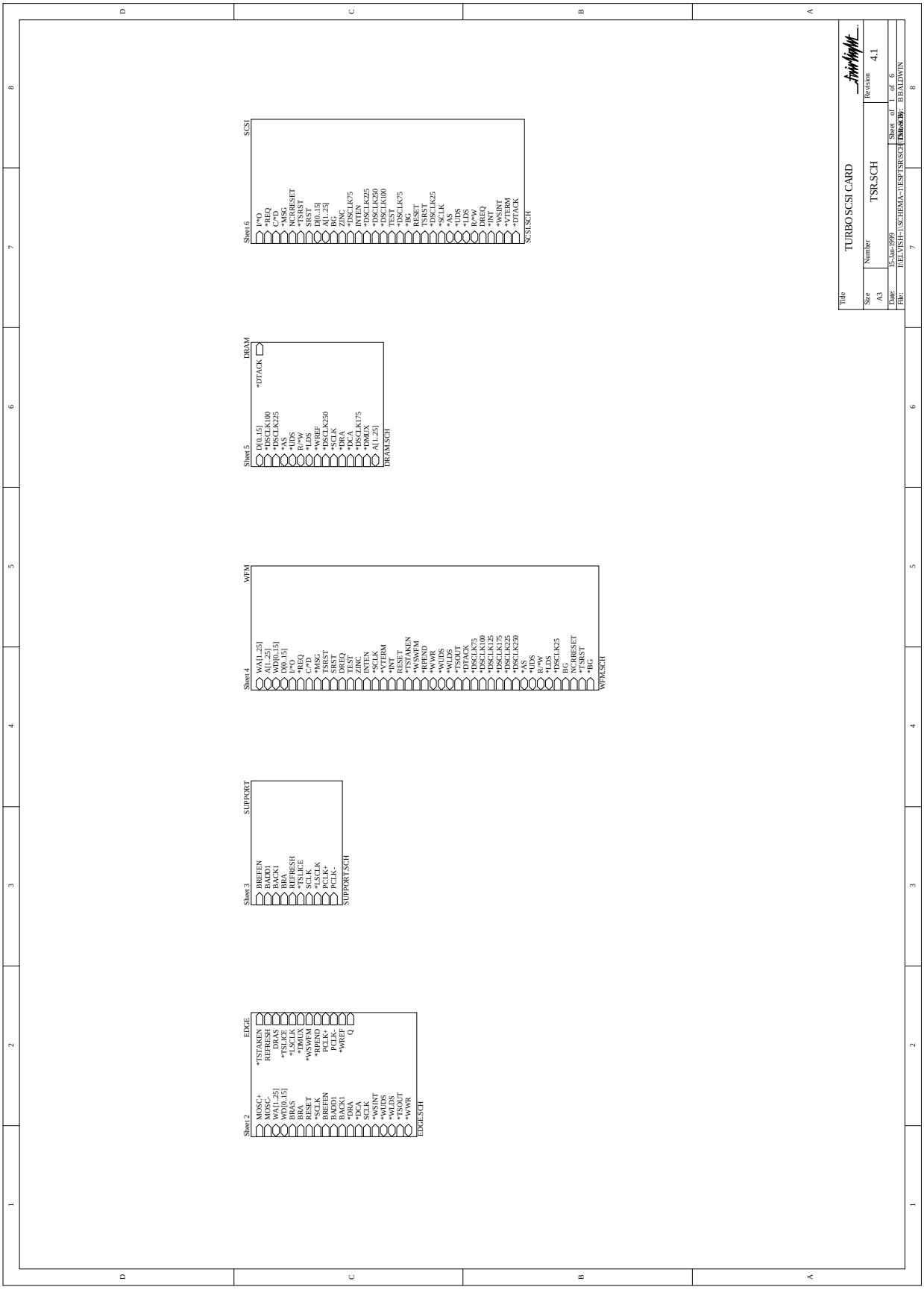
TSCSI provides a single ended asynchronous SCSI interface directly from the NCR53C94 to the SCSI connector CN3. Note that the termination resistors RN7, RN8, RN9 (220R/330R) must only be installed if TSCSI is the last SCSI device on the SCSI chain.

Shorting JP2 connects +5V via diode D2 (1N4001) and fuse F1 (1A) to the SCSI termination voltage pin 26 on CN3. D 1 and F 1 are provided to protect the MFX3plus power supply in case of incorrect SCSI cable connection.

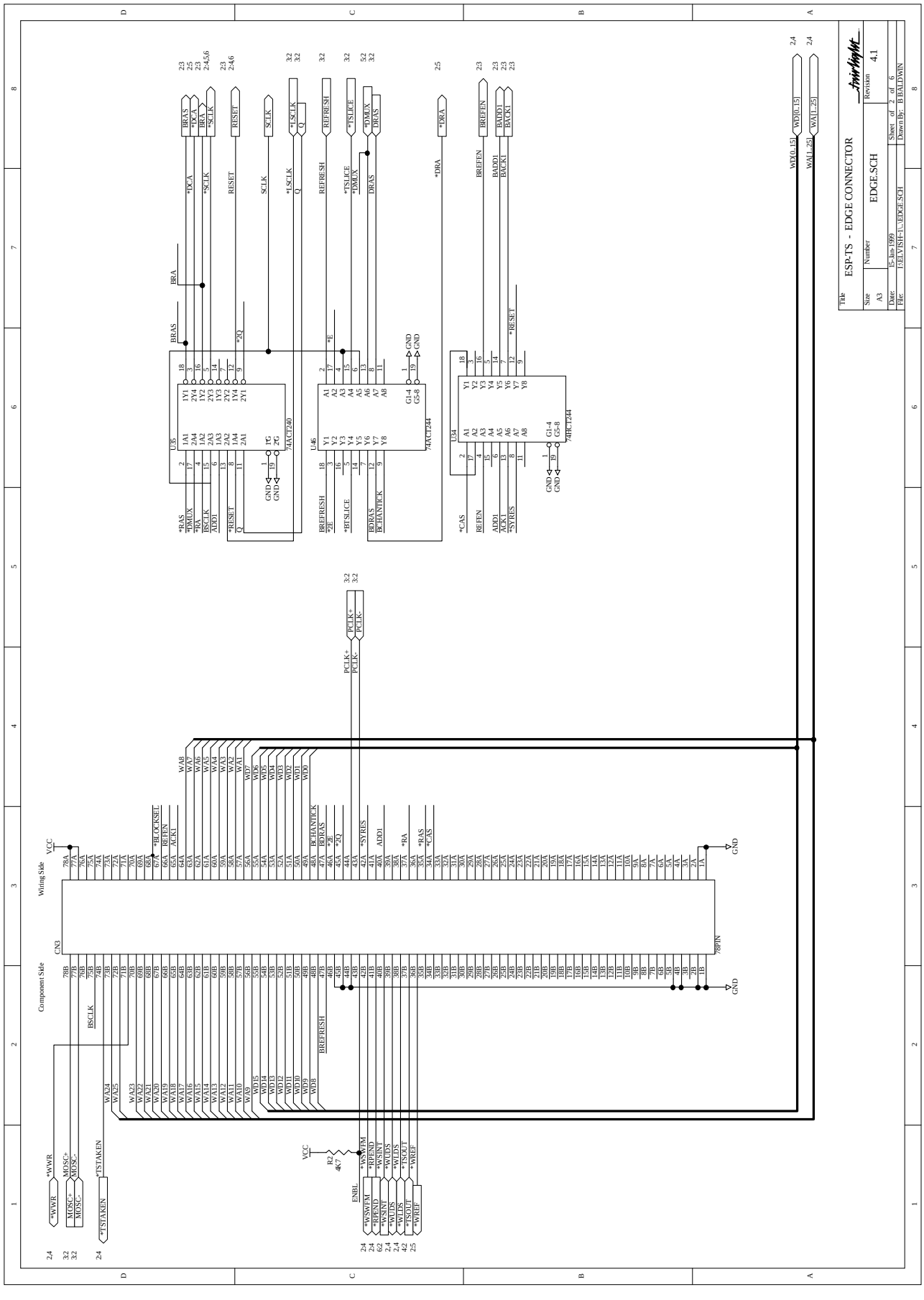
Interrupts from the NCR53C94 (*INT) are gated with the control register INTEN (TSCSI card interrupt enable) by TSSCSI14 PAL (U48), to the WFMBUSS as WSINT (edge connector pin 40B). WSINT is connected to Interrupt Level 6 on the Waveform Executive. Note that WSINT is an active high tri-state interrupt signal shared by all future WFMBUSS masters.

13.3 ESPTSR SCHEMATICS

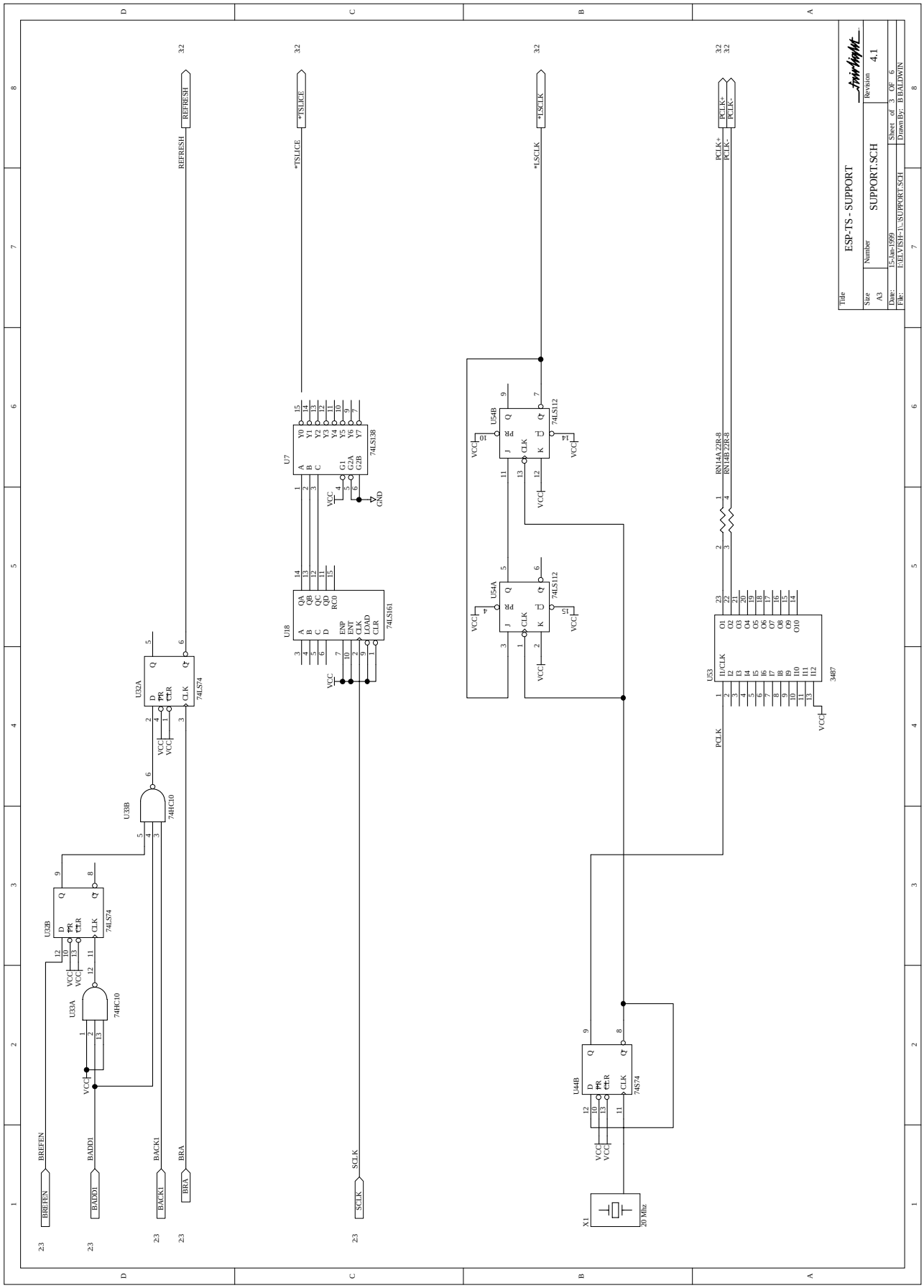
13.3.1 ESPTSR INTERCONNECTING DIAGRAM



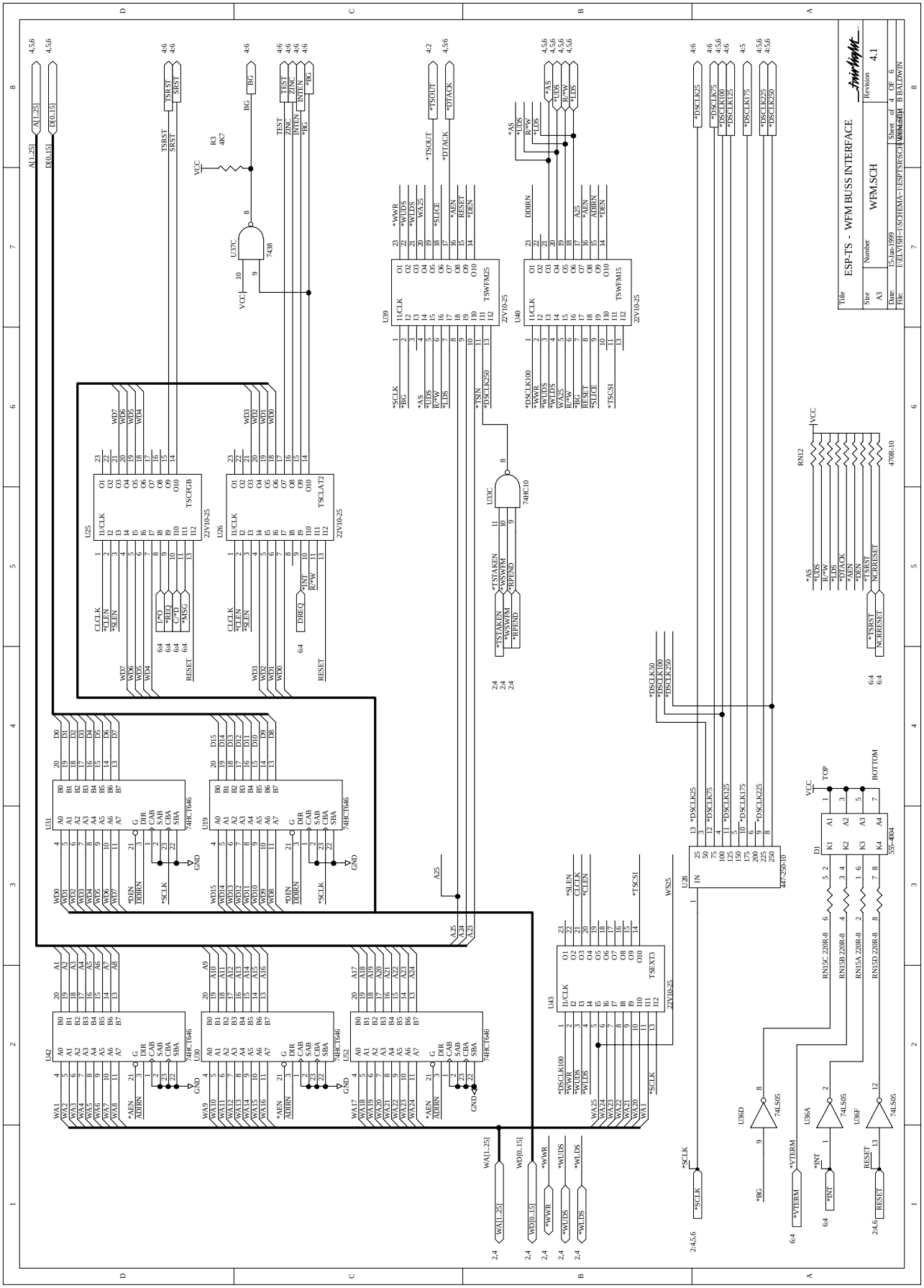
13.3.2 ESPTSR EDGE CONNECTOR



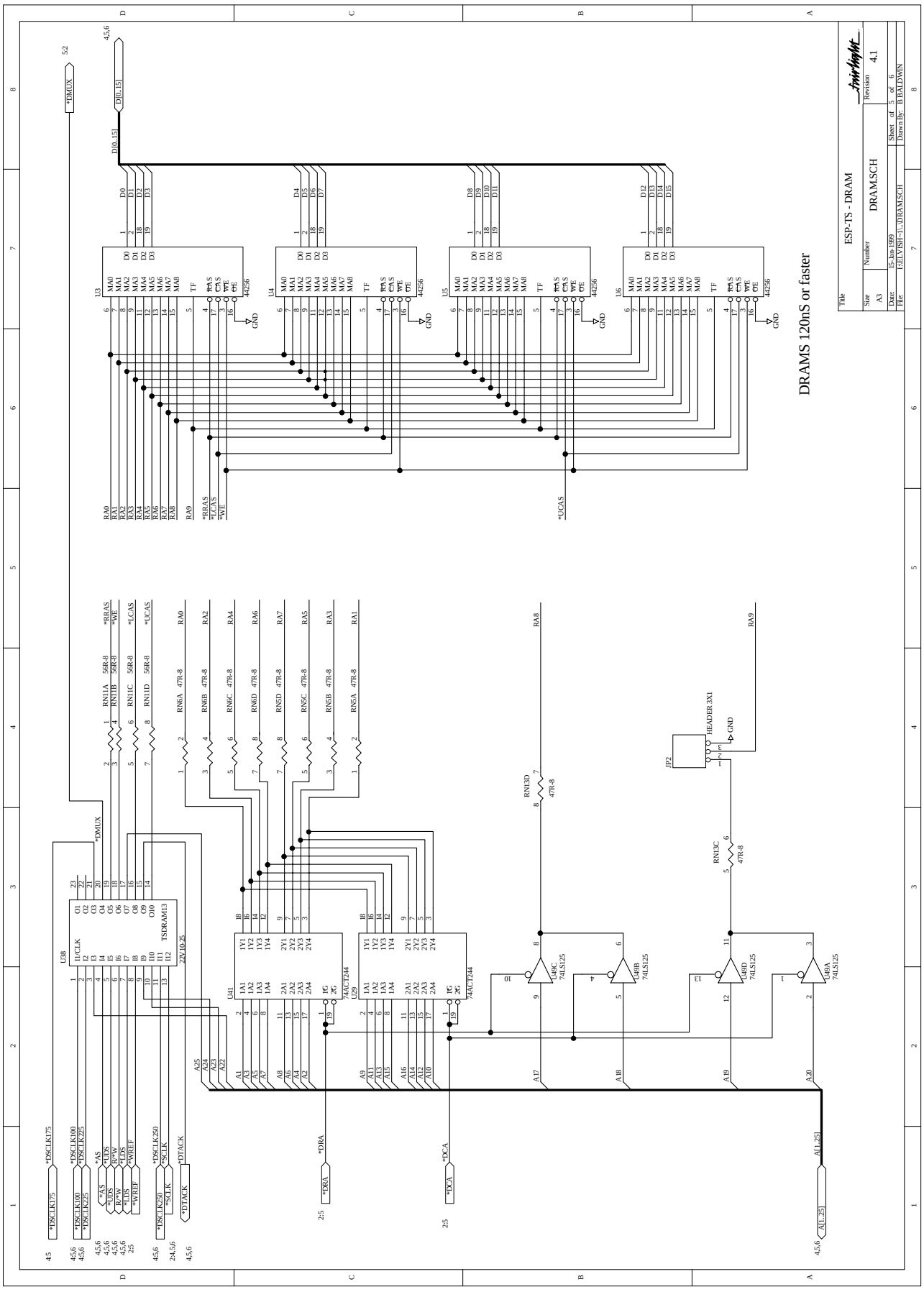
13.3.3 ESPTSR SUPPORT



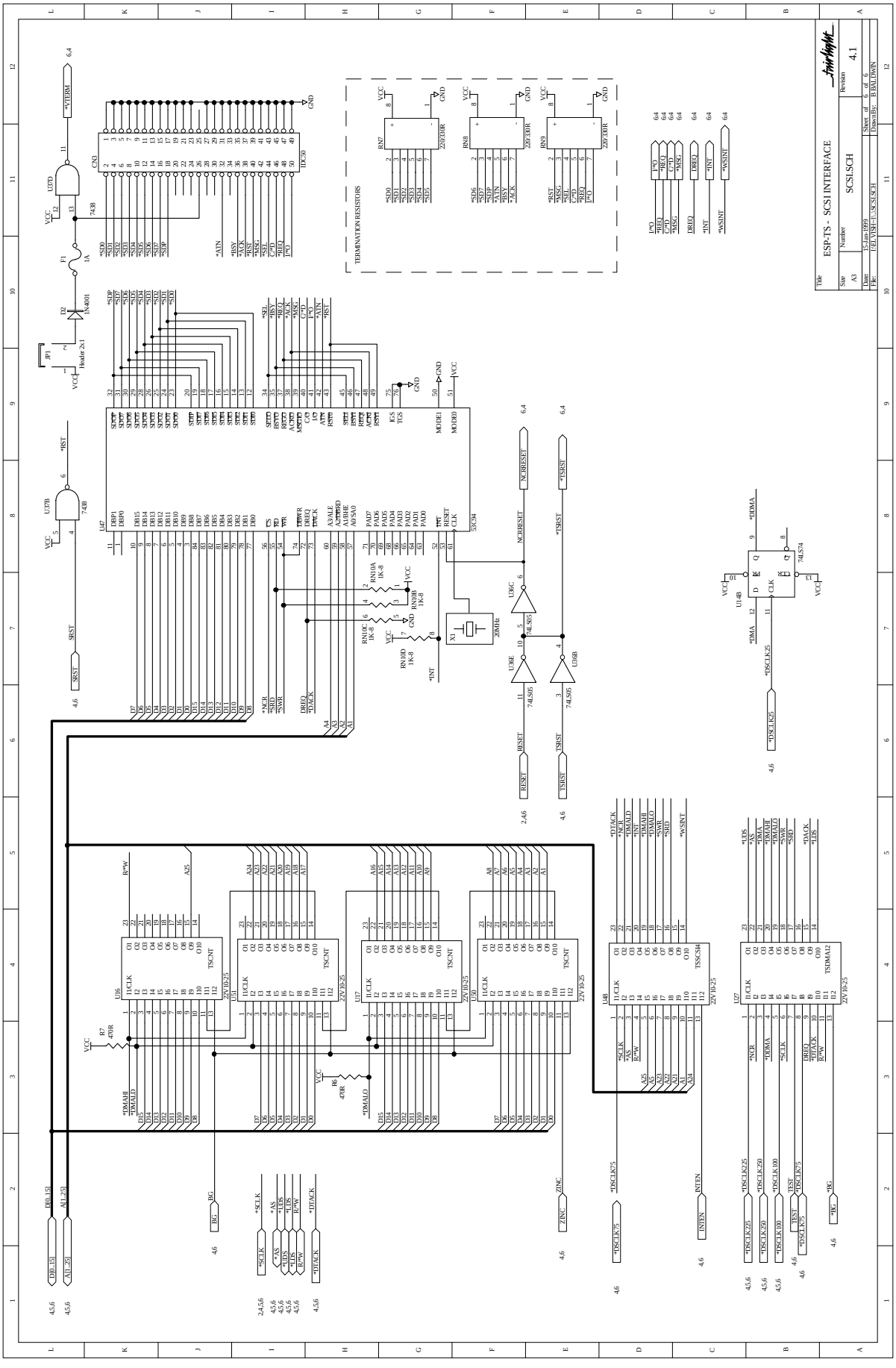
13.3.4 ESPTSR WFM Bus Interface



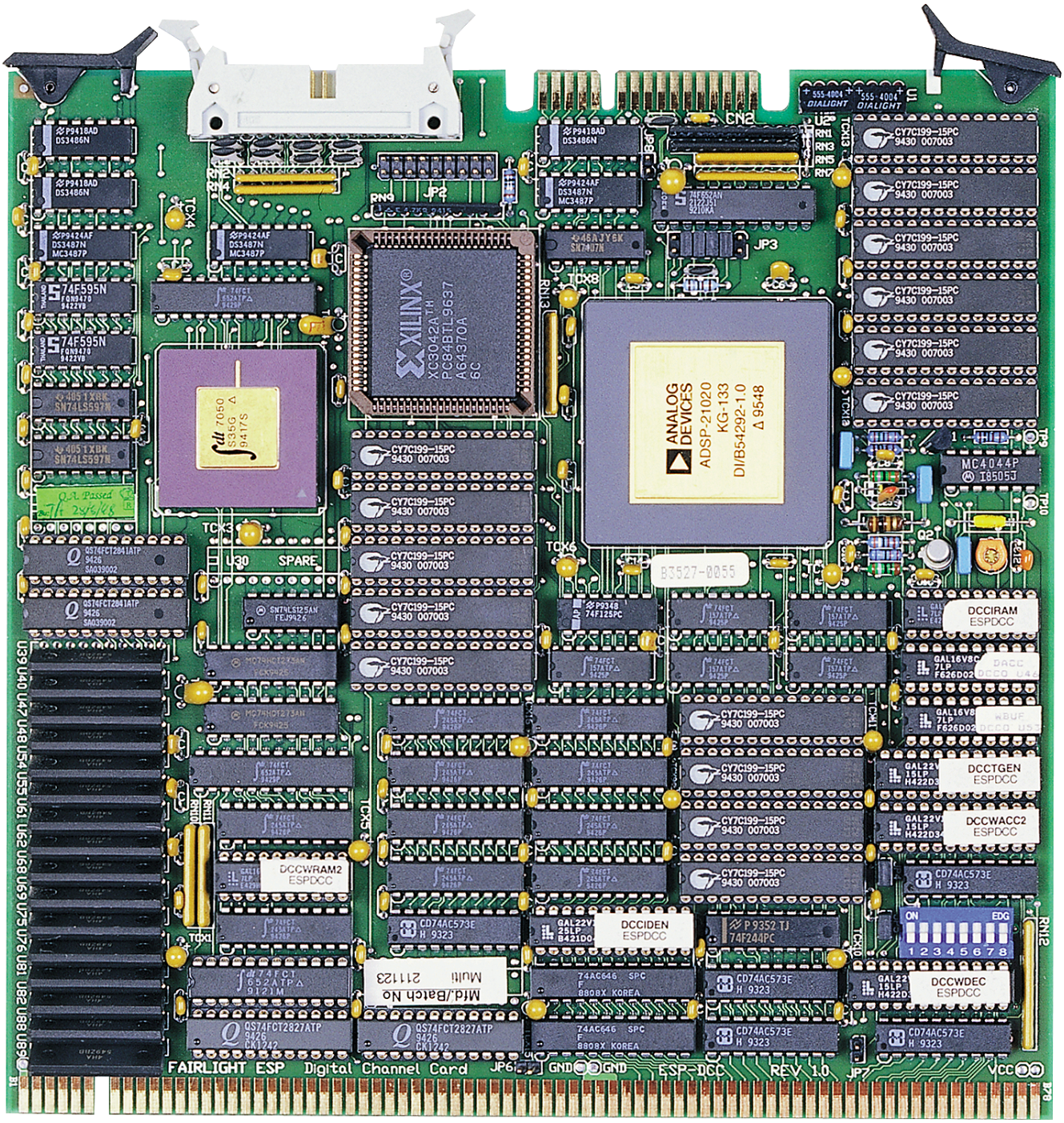
13.3.5 ESPTSR DRAM



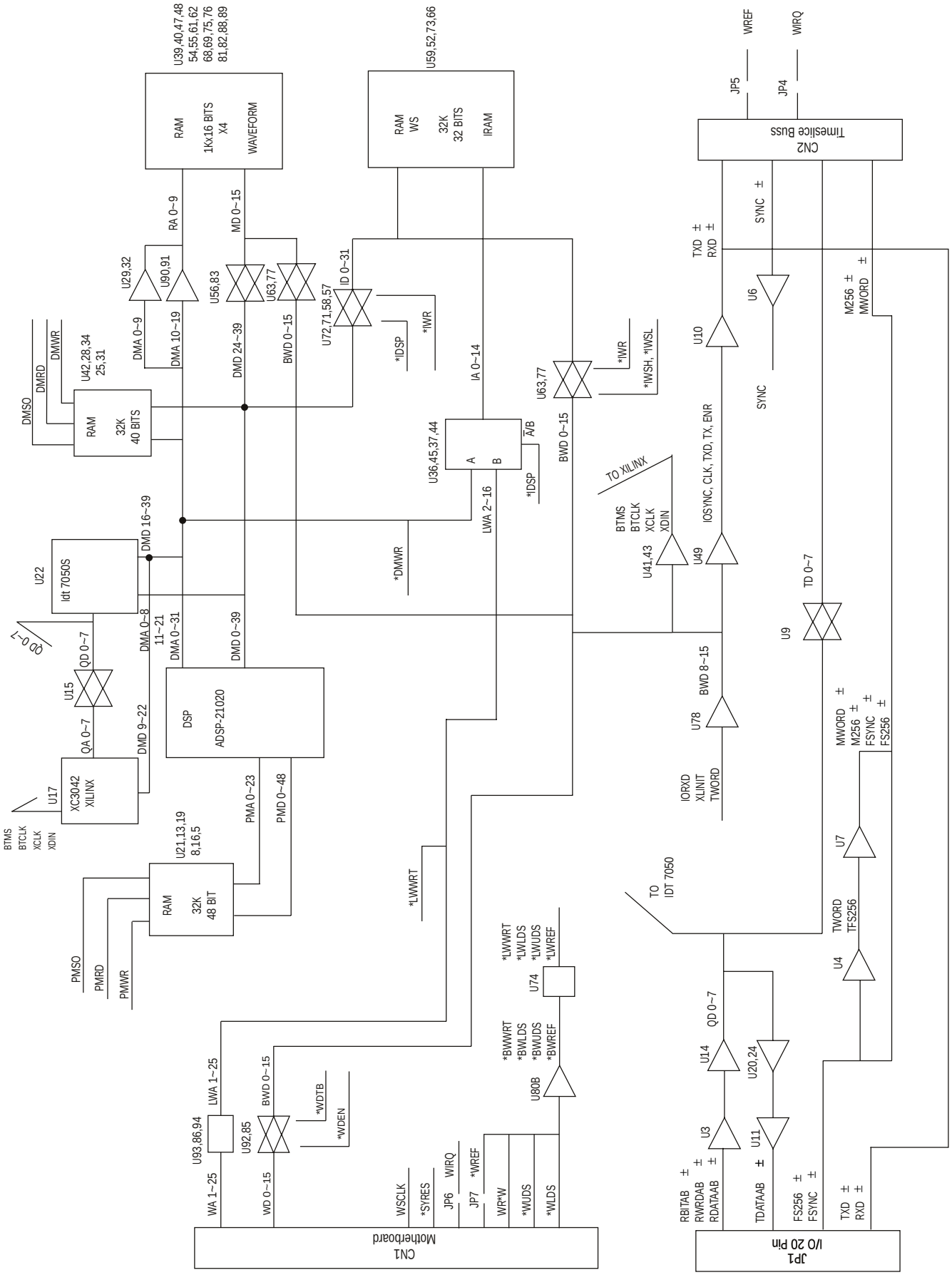
13.3.6 ESPTSR SCSI INTERFACE



14.0 ESPDCC Digital Channel Card



14.1 ESPDCC Block Diagram



14.2 ESPDCC Circuit Description

14.2.1 Document Revision

03.08.1994 v0.x

14.2.2 Terminology

AIO	Analog I/O Card (ESP-AIO)
DCC	Digital Channel Card (ESP-DCC)
DIO	Digital I/O Card (ESP-DIO)
DSP	Digital Signal Processor
IRAM	Interface RAM
QPRAM	Quad-Port RAM
SC	Sync Card (ESP-SYN)
SRAM	Static RAM
SRC	Sample Rate Conversion
SSI	Synchronous Serial Interface
TSB	Timesliced Sample Bus
WBUS	Waveform Bus
WRAM	Waveform RAM
WX	Waveform Executive

14.2.3 Overview

14.2.3.1 Clock Subsystem

The 33MHz clock is derived from the 3.3MHz WBUS signal SCLK by way of a phase-locked-loop. An MC4044 phase detector drives a 66MHz varactor-controlled VCO. The 66MHz clock is used by DCCTGEN to derive all other on-board timing signals including the 33MHz clock and the reference signal SREF which is locked to SCLK by the MC4044. This ensures minimum skew between the various timing signals.

14.2.3.2 DSP Subsystem

The DCC uses an Analog Devices ADSP21020-KG133, which has a 30nS cycle time and executes an instruction in every cycle; one instruction may conditionally perform up to three floating point arithmetic operations as well as two 40 bit data transfers. The part generates a 133MHz internal clock by phase locking to the 33MHz external bus clock.

Working memory for program and data storage is provided by 32k x 48 bits SRAM on the program memory (PM) bus and 32k x 40 bits SRAM on the data memory (DM) bus. 15nS SRAM is used to enable no wait-state operation.

14.2.3.3 WBUS Interface

The DCC occupies several address segments on the waveform bus as follows:

02000000-027FFFFF	WRAM mask C
04000000-047FFFFF	WRAM mask B
05000000-057FFFFF	WRAM mask A
05A00000-05A07FFF	IRAM mask A
05A40000-05A47FFF	IRAM mask B
05A80000-05A87FFF	IRAM mask C
05AC0000-05AC7FFF	control/status registers (mask A only)
05B00000	write to mask A
05B40000	write to mask B
05B80000	write to mask C
0x02000000+(cardID&7)*0x00400000	WRAM direct (top 4MB) (if DIPsw 5 ON)

All DCCs in a system reside at the same addresses. Cards are selected by writing a 16 bit mask to one of the mask registers (A, B or C). A card becomes selected if the bit corresponding to the card ID is set in the mask. Writes to the mask registers must always be 16 bits wide. The mask register cannot be read back. The 4 bit card ID is set via DIP switches 1..4

Mask A is intended to be used for software accesses, since the control/status registers can only be accessed via this mask. Masks B and C are intended for DMA channels.

In addition to the three mask-controlled 8MB windows into WRAM, a separate “direct” window into the top 4MB of WRAM can be enabled via DIP switch 5. This window is not controlled by any mask register and occupies an address on the WBUS which depends on the low 3 bits of the card ID.

14.2.3.4 IRAM Subsystem

The interface RAM (IRAM) subsystem provides 32k x 32 bits (128MB) of SRAM which can be accessed by the DSP and from the WBUS. DSP accesses normally incur only one wait state but additional DSP wait states are inserted if the DSP access would otherwise collide with a WBUS access.

The floating point extension field of the DSP data bus (bits 0..7) is not driven on DSP read cycles and will contain garbage data.

14.2.3.5 WRAM Subsystem

The waveform RAM is organised as 4M x 16 bits (8MB) of 70nS DRAM and can be accessed by the DSP and from the WBUS. WRAM cycles are 150nS long and are synchronised to the WBUS. This guarantees a minimum of one DSP access cycle every 300nS. If no WBUS or refresh cycle is taking place then the DSP may use every WRAM cycle.

The 16 bit waveform data appears on the upper 16 bits of the DSP data bus. The lower 16 bits of the 32 bit integer field are read as zeros and ignored on writes. The floating point extension field is not driven on reads and will contain junk.

DSP accesses can be in either foreground or background mode. In foreground mode the DSP waits for the access to be completed before continuing. This results in a minimum of 5 wait states. Additional wait states are inserted if necessary to synchronise with the next WRAM cycle, or if the next WRAM cycle is taken by a WBUS access or refresh cycle.

Background mode allows the DSP to continue executing instructions whilst the WRAM access takes place. In the case of a background write the data and address are latched and the

data written to WRAM in the next available WRAM cycle. A background read cycle latches the address and causes the data at that address to be read from WRAM and latched in the next available WRAM cycle. The data read by the DSP is the data which was latched by the previous background read cycle. A pre-read cycle must be executed to load the first data word into the latch.

If the DSP accesses WRAM in any mode before a previous background request has been completed then extra wait states are inserted until the background access is complete.

Background accesses which are not held up for this reason incur only one wait state.

Care must be taken to ensure that only one software process at a time uses the background read function, otherwise the latched data will be corrupted.

14.2.4 DCC I/O Subsystem

14.2.4.1 Quad-Port RAM

The QPRAM acts as the interface between the DSP and the I/O section of the digital channel card. This device has 1024 bytes of static RAM which can be accessed simultaneously by four independent ports. Three of the four ports are connected to the DSP data memory bus and the fourth to the 8 bit I/O bus which feeds the SSI and TSB ports and which is controlled by the Xilinx Gate Array.

The QPRAM is configured logically as 256 sample words of 32 bits each. It is divided into four “pages” of 64 samples each. The first three pages are used for the TSB interface and SSI output ports. The fourth page is further subdivided into two 16 x 64 bit input buffers which are filled by the SSI input ports.

The three ports connected to the DSP allow it to read or write a 24 bit sample in one access (with one wait state). The remaining 8 bits of each word in the QPRAM do not generally change with each sample and can be setup once during initialisation. The high order address bits are used to determine which bytes of the sample word in QPRAM are read or written by the DSP when it accesses the QPRAM.

On writes to QPRAM the data on the high 24 bits of the DSP data bus are written. On read cycles the high 24 bits of the data bus are driven by the QPRAM; the low 8 bits of the 32 bit integer field are set to zero by the Xilinx. The 8 floating point extension bits are not driven and will contain garbage.

The QPRAM has an access time of 35nS, thus with a 33MHz (30nS) system clock the minimum QPRAM cycle period is 60nS.

14.2.4.2 Timesliced Bus Interface

The TSB provides a sample-synchronous bidirectional communication path between all DCCs in the system. In addition the sync card has an output-only TSB port which is used to transmit transport control commands to the DCCs.

The TSB is an 8 bit wide data bus (TD0..7) controlled by a single active low strobe line (*TSBEN). Each TSB cycle is 180nS long and consists of a 60nS enable phase followed by a 120nS data phase. The enable phase of a cycle may overlap the data phase of the previous cycle to give an effective cycle time of 120nS for consecutive cycles.

During the enable phase *TSBEN is asserted by the TSB master for 60nS; this allows sufficient time for TSB receivers to synchronise *TSBEN to their 33MHz clocks and initiate TSB

cycle processing. During the data phase the TSB data lines are driven for the full 120nS and the data is latched by TSB receivers after nominally 90nS. A large margin is allowed for synchronisation errors.

TSB cycles are grouped into sample “slots” of 3 cycles or 24 bits each (MS byte first). The slots are numbered sequentially starting from zero at the TSB trigger point. This is defined to be 7/8 of the way through a master clock sample period (which is the point at which the SSI transmitter logic begins fetching the first byte for the next sample). The TSB trigger point is common to all cards in the system since it is synchronised to the master clock.

At any given time the TSB may be either active or idle; when the TSB is active one card (the TSB Master) is transmitting to the TSB and all others are receiving. Each card is allocated a certain number of slots during which it is the master, and begins transmitting as soon as the appropriate slot number is reached; thus no common timing or arbitration logic is required. Once all cards have transmitted their data (ie there is no card programmed to become master at the next slot) the TSB becomes idle until the next TSB trigger point.

It is up to the controlling software to ensure that allocated slot numbers do not overlap (which would result in a bus collision) and that there are no gaps (which would cause the TSB to become prematurely idle, since no card would assume mastership). One card on the TSB must be programmed to be “first master”, in which case it assumes mastership of the TSB immediately after the TSB trigger point. If a sync card is present then it will generally be the first master, however a DCC can also be programmed to be first TSB master if required.

Although the TSB cycle timing is derived from the 33MHz clock on each DCC (which is in turn synchronised to the 3.3MHz system global SCLK signal), the inter-cycle timing is determined solely by the current TSB master. TSB receivers do not make any assumptions about when to expect the next TSB cycle, and process the incoming data and strobe signals as completely asynchronous (to the on-board 33MHz clock). Slot numbers are determined “on the fly” by counting TSB cycles.

The TSB data bus is connected to a 74F652 bidirectional data latch on the DCC. Data is transferred to and from the QPRAM under control of the Xilinx.

Data is stored in QPRAM according to TSB slot number. Thus the array of data in QPRAM is referred to as the “TSB image”, since it represents a snapshot of all data transferred over the TSB during a given sample period.

There are three complete TSB images in QPRAM, referred to as the PREVIOUS, CURRENT and NEXT pages. Data transfers to and from the TSB always access the CURRENT page. At the TSB trigger point the three pages are rotated so that CURRENT becomes PREVIOUS and NEXT becomes CURRENT.

Data written by the DSP to the NEXT page during the current sample period will be transmitted over the TSB during the next sample period. The PREVIOUS page contains a complete image of all TSB transfers performed during the previous sample period, including the data written by this DSP to the NEXT page two sample periods ago.

This allows the TSB image in the PREVIOUS page to be processed by software without regard to the source of the data.

The DSP should not access the CURRENT page because the data is changing and will be meaningless. In addition, care must be taken to ensure that the DSP is not accessing the TSB image at the TSB trigger point. In practice this is achieved by doing all TSB image accesses in the master sample interrupt handler; the interrupt is also generated at the TSB trigger point.

The DSP can determine the current page by reading the Xilinx status register. This must also be synchronised with the sample interrupt to ensure valid data.

Each TSB image in the QPRAM is 64 samples long; however the last four slots of each page are used by the SSI output ports and should not be used for TSB transfers; thus a maximum of 60 TSB slots can be supported by the hardware.

TSB transfers always access the high 24 bits of the 32 bit sample in QPRAM (byte offsets 0, 1 and 2). The low byte remains unchanged.

Each change of TSB mastership incurs a dead period of 180nS. The sync card requires about 250nS after the TSB trigger point to get going. Thus assuming a maximum sample rate of 48k + 15% and 6 changes of bus mastership (sync card & 6 DCCs) we can calculate the guaranteed minimum number of TSB slots available as (1000000/(48*1.15) - 250 - 180*6) / (120 * 3) = 46 slots.

14.2.4.3 Synchronous Serial Interface (SSI) Ports

There are two SSI stereo input ports and two SSI stereo output ports. Each port consists of three balanced (RS422) signals: data, bitclock and wordclock. The rising edge of wordclock begins a new sample period, during which 64 bits of data are transmitted on the data line. Data is clocked out of the transmitter on the rising edge of bitclock and latched by the receiver on the falling edge.

The 64 data bits encode two sample values; one for the left channel and one for the right channel. Various data formats are possible; the format used by the DIO card encodes the left sample MSB first in the first 32 data bits and the right sample in the second 32 data bits. Thus during the left sample period wordclock is high, and during the right sample period low. In general samples contain less than 32 significant bits; the unused bits are set to zero.

Each output port on the DCC consists of a 74LS597 double buffered 8 bit shift register feeding an MC3487 RS422 transmitter. Since all MFX3 outputs are synchronous only one pair of timing signals is used for both output ports. The bitclock is replaced by the master clock 256 * Fs timing signal.

Each input port consists of an MC3486 RS422 receiver followed by a 74F595 double buffered 8 bit shift register.

Data transfers between the QPRAM and the SSI ports are controlled by the Xilinx. The data transfer to or from the holding register of the shifter takes place whilst the previous 8 bits are being shifted out or the next 8 bits shifted in. Thus a full 8 bit period (at least 2.2uS) is available for the data transfer.

14.2.5 Xilinx Gate Array

The Xilinx Gate Array on the DCC is responsible for controlling the operation of the serial interface ports, timesliced bus and quad-port RAM by generating the appropriate control and address signals. In addition the low 16 bits of the data bus (integer field) are driven low by the Xilinx during DSP reads from waveform memory.

The Xilinx configuration program is loaded serially via the DCC control latch which sits on the waveform bus. The DSP has no access to this control latch.

The following description refers to the X1 program which is used for MFX3^{plus} operation.

14.2.6 Xilinx Configuration Program X1

14.2.6.1 General

The X1 program's main function is to control the flow of data between the QPRAM and the I/O devices (SSI shift registers and TSB data buffer). The 33MHz system clock is used as the primary global clock signal. To achieve reliable operation at this speed very heavy use is made of pipelined synchronous logic. Almost all logic stages contain only one level of CLBs between registers.

The X1 program contains a number of interconnected functional blocks which correspond to the source files (sub-sheets):

Control/Status registers
DSP data bus interface
SSI transmitter control
SSI receiver port A control
SSI receiver port B control
SSI receiver port A/B multiplexing
TSB control
TSB address generation
QPRAM arbitration & timing
QPRAM control signal generation
QPRAM address multiplexing
QPRAM address bus interface

14.2.6.2 Control/Status Registers

DSP data bus interface

This section includes the interface to the DSP control and address signals.

The main control register provides the following functions:

TSB Mastership Start Slot Number minus one	6 bits
TSB Mastership End Slot Number	6 bits
TSB First Master Enable	1 bit
SSI Transmitter Direct Read	1 bit
Master Clock DIO Slave Enable (inverted)	1 bit
Master Clock DIO Master Enable	1 bit

The auxiliary control register provides the following functions:

QPRAM Enable	1 bit

There are two status register locations which access respectively the A and B SSI receiver ports. The high bits of the status register are common to both locations:

SSI receiver port A/B timing	10 bits (A/B)
TSB current page number	2 bits (common)
Sync input	1 bit (common)

Control logic decodes the DSP address and control lines and generates clock signals for the two

control registers and output enables for the status registers. The DSP data bus is driven by the Xilinx in four modes:

Status register A read	assert D15..0 with RX port A status
Status register B read	assert D15..0 with RX port B status
Waveform RAM read	assert D15..0 with zero data
QPRAM read	assert D7..0 with zero data

14.2.6.3 SSI TRANSMITTER CONTROL

Most of the transmitter logic is common to the two output ports since all MFX3 outputs are synchronised to the common master clock.

There are two modes of operation for the transmitter ports. When DIRECT mode is selected data is read from the SSI transmitter locations in QPRAM and loaded directly into the shift register chips. In INDIRECT mode the data read from the SSI transmitter locations in QPRAM is latched and then used to address QPRAM in a second cycle. The data read in the second cycle is loaded into the shift register chips.

The first cycle (and only cycle in DIRECT mode) always accesses fixed locations in the CURRENT page of QPRAM; the second cycle accesses the PREVIOUS page. The fixed locations accessed by the first cycle are:

slot number	transmitter channel
60	port A left side (first 32 bits)
61	port A right side (second 32 bits)
62	port B left side (first 32 bits)
63	port B right side (second 32 bits)

INDIRECT mode allows the SSI transmitter locations in QPRAM to be programmed with the TSB slot numbers from which data is to be transmitted. Thus data transmission from an arbitrary TSB slot is achieved without intervention from the DSP.

The high 6 bits of the indirect address specify the slot number from which data is to be read; the low 2 bits specify the byte within the 32 bit sample word for the specified slot.

The SSI transmitter logic receives as input the two master clock signals FS256 and WCLK. FS256 is divided by 4 yield the bit clock for the transmitter shift registers. After eight bit clocks the signal TBYTE is asserted to transfer the next byte from the holding register into the shift register. The trailing edge of TBYTE is synchronised and latched to generate the transmitter request signal TREQ.

Once asserted, TREQ remains active until both transmitter ports have been serviced. This requires 2 QPRAM cycles in DIRECT mode and 4 QPRAM cycles in INDIRECT mode.

The SSI transmitter logic is also responsible for generating the TSB trigger signal and DSP interrupt at the 7/8 point in the master clock sample period. The interrupt line is asserted for 60nS.

14.2.6.4 SSI RECEIVER PORT A CONTROL

SSI receiver port B control

SSI receiver port A/B multiplexing

Each receiver port takes two inputs - word clock and bit clock - and generates a byte strobe to

transfer data from the shift register to the holding register at the end of each byte. At this time a QPRAM request is also asserted to transfer the data into the receiver queue in QPRAM.

The receiver queue contains 16 L/R pairs of samples, which allows the DSP to read input samples from QPRAM in a block for greater efficiency. The current queue pointer can be read from the status register.

The receiver ports are in general asynchronous to the master clock. In order for the DSP to implement the sample rate conversion (SRC) algorithm the ratio of the receiver sample rate to the master clock sample rate is required. This is measured by latching the values of the receiver bit counter and queue pointer at each TSB trigger point, which yields the required ratio to an accuracy of 10 bits maximum.

The receiver logic operates synchronously to the 33MHz system clock, so that the latching of the bit counter and queue pointer values is not subject to race conditions.

14.2.6.5 TSB CONTROL

The TSB control logic operates in either TSB master mode or as a TSB slave (receiver).

In slave mode the incoming TSB enable strobe *TSBEN is synchronised to the local 33MHz clock and generates TCLKI which latches the TSB data during the data phase, and the internal QPRAM request signal TSREQ.

When TSBEG is asserted by the TSB address generator logic the TSB controller enters master mode at the beginning of the next slot. In master mode QPRAM requests are generated automatically and *TSBEN is driven onto the TSB.

The assertion of TSEND causes slave mode to be reentered at the end of the current slot.

If the TSFIRST control bit is set then master mode is entered immediately after the TSB trigger occurs.

14.2.6.6 TSB ADDRESS GENERATION

The TSB address counter is cleared by the TSB trigger pulse (TSTRIG) and incremented after each TSB cycle. The two low bits of the counter are the byte address within the slot and are incremented modulo 3, since the TSB transfers three bytes per slot.

Two address comparators generate signals to control entry and exit from TSB master state. TSBEG is asserted during the slot prior to the first master slot; TSEND is asserted during the last master slot.

TSTRIG also causes the current page counter (TSCUR0..1) to be incremented modulo 3.

14.2.6.7 QPRAM ARBITRATION & TIMING

QPRAM cycles are 60nS long and can begin at any 30nS system clock interval.

The QPRAM arbitration logic is primarily concerned with servicing TSB requests, since the TSB is the highest bandwidth I/O device. Other I/O devices are “slotted in” between TSB cycles. Since the TSB can generate a request every 120nS it will consume on average half of the available QPRAM bandwidth. However because the incoming TSB cycles are processed asynchronously we must assume a worst case scenario in which every second TSB cycle “slips” 30nS, which will result in only one quarter of the QPRAM bandwidth remaining for other devices. This means in effect one SSI cycle every 240nS. This is still adequate to support both SSI output ports operating in indirect mode at 48kHz+15% and both SSI input ports operating at a

sample rate well above 48kHz.

There are four sources of QPRAM requests which are prioritised as follows (highest to lowest):

TSB
SSI receiver port A
SSI receiver port B
SSI transmitter

TSB requests are handled differently in that a pending TSB request prevents any other QPRAM request from being recognised in the 30nS preceding the TSB cycle. This ensures that TSB QPRAM cycles are never delayed by other requests, which would cause TSB data to be lost.

All three SSI requests undergo an extra level of pipelining in which arbitration is performed and a combined SSI request signal generated.

14.2.6.8 QPRAM address multiplexing

The QPRAM address multiplexor selects the appropriate address to be output to QPRAM according to the type of the current cycle. Addresses for the SSI receiver channels are pre-multiplexed and pipelined; this allows the final multiplexor stages to be implemented in one CLB level by reducing the number of inputs to each multiplexor.

14.2.6.9 QPRAM control interface

QPRAM address bus interface

All control and address outputs are pipelined using the IOB output registers to ensure that internal routing & propagation delays do not affect external timing. All control signals are asserted for the duration of the QPRAM cycle (60nS) with the exception of the write enable signal *QWR, which is asserted for 30nS in the middle of the cycle. This ensures that the setup and hold requirements of the QPRAM part are met on write cycles.

14.2.6.9.1 QPRAM Cycle Descriptions

TSB Slave:

A9-A8	current page (0..2)
A7-A2	slot number
A1-A0	byte within sample (0..2)

assert TSENI, *QCE, *QWR(30nS)

TSB Master:

A9-A8	current page (0..2)
A7-A2	slot number
A1-A0	byte within sample (0..2)

assert TCLKO, *QCE, *QRD

SSI RXA/B:

A9-A8	all ones
A7	port A => 0, port B => 1
A6-A3	RX queue pointer (0..15)
A2-A0	byte within sample period (0..7)

assert *RENBA/B, *QCE, *QWR(30nS)

SSI TXA/B Direct:

A9-A8	current page (0..2)
A7-A4	all ones
A3	port A => 0, port B => 1
A2-A0	byte within sample period (0..7)

assert TLDA/B, *QCE, *QRD

SSI TXA/B Indirect Address Fetch:

A9-A8	current page (0..2)
A7-A4	all ones
A3	port A => 0, port B => 1
A2-A0	byte within sample period (0..7)

assert NCLK, *QCE, *QRD

SSI TXA/B Indirect Data Transfer:

A9-A8	previous page (0..2)
A7-A0	tristate

assert TLDA/B, *QCE, *QRD, *NOE (enables indirect address onto A7-A0)

14.2.7 Additional References

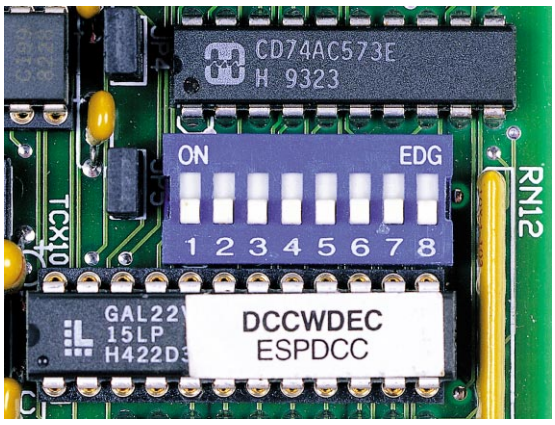
ADSP-21020 User's Manual (Analog Devices)

ADSP-21020KG-133 Data Sheet (Analog Devices)

XC3042-125 Data Sheet (Xilinx)

14.3 ESPDCC ID Switch Settings

Each DCC is addressable to the waveform bus by means of a physical dip switch on the upper right hand side of the card. See the photograph below to locate the address switch.



The addressing is binary, meaning that the switches represent binary values of zero and one, making the first decimal value zero. The MFX3Plus has only enough physical room for eight DCCs in the digital rack. Therefore, addresses 0-7 are all we need to concern ourselves with here. Binary 7 can be expressed in three digits, meaning that only switch numbers one two and three are used.

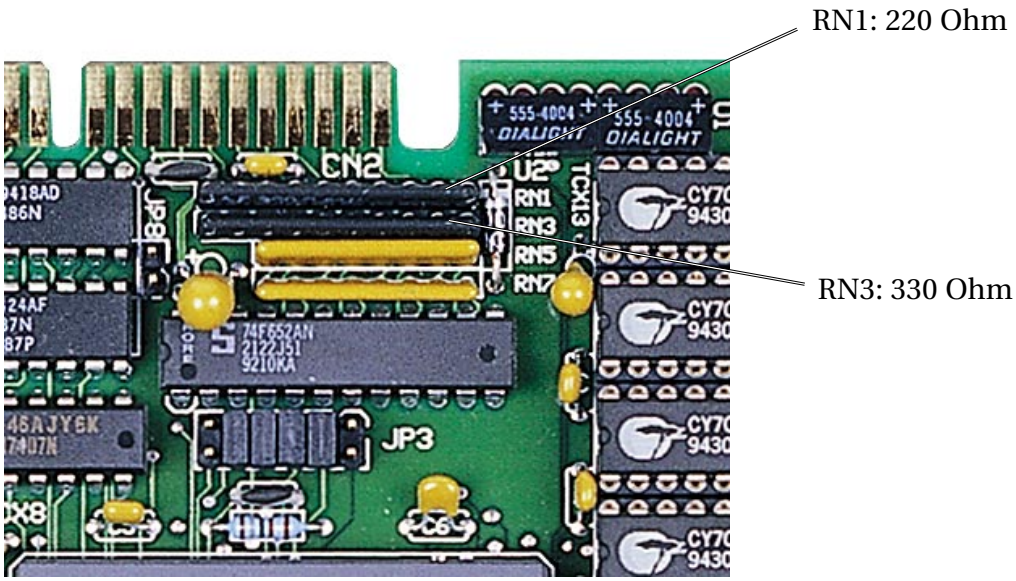
Set the switches on each DCC according to its location in the MFX Rack or Mini as per the table below. Take notice that the DCC that is addressed to zero must have two TSB Terminating resistor packs installed in locations RN1 and RN3.

14.3.1 DCC Addressing Table

Decimal Address	Binary Address	Switch 1	Switch 2	Switch 3	Rack Slot /Mini Slot
0	000	OFF	OFF	OFF	9 / 3
1	001	ON	OFF	OFF	8 / 2
2	010	OFF	ON	OFF	7
3	011	ON	ON	OFF	6
4	100	OFF	OFF	ON	5
5	101	ON	OFF	ON	4
6	110	OFF	ON	ON	3
7	111	ON	ON	ON	2

14.3.2 DCC Termination

The DCC at address 0 (located furthest from the Sync Card) should have termination resistors installed as follows:



14.4 ESPDCC Field Diagnostics

These diagnostics will check the features of the card and report any errors.

Multiple cards may be concurrently checked if S1 (DIP SWITCH) is set to a different address for each card. Cards are addressed as the binary code on S1 where switch 1 is the least significant bit. Further information on dccdiag is printed if invoked with:

```
dccdiag  -?
```

14.4.1 Diagnostic test procedure

1. Install the TSB cable and DIO cable to the card.
2. If the TSB cable is not connected to the SC, then JP7 must be installed.
3. Turn on system.
4. When at # prompt, run the DCC diagnostics by typing the following:

```
dccdiag    <return>.
```

5. Check 1st line of diagnostics:
6. " Wram size = ", is the correct size for the card eg. 6MB for DCC6 or 8MB for DCC8.
7. Check if any errors occur and note what they are, eg. Iram-wx: wa or Wram-wx: wa etc.
8. Use of further diagnostics and testing will be required if errors are found.

14.4.2 ESPDCC Diagnostic Program

DCCDIAG V2.01

Options:	-c=<num>	Only Test card <num> (default all cards)
	-e	no error abort
	-e=num>	error abort limit (default 1)
	-g	run JTAG bus banging test <forever>
	-m	boot DCC from IRAM (default WRAM)
	-j	include JTAG bus integrity tests
	-q {q}	quiet mode
	-r	repeat indefinitely
	-r=<num>	Repeat <num> times
	-s	load random seed from time of day
	-s=<num>	specify initial random seed <default 41>
	-v {v}	verbose mode
	-w	include WRAM tests
	-z {z}	Debug Mode

Test options <all tests if none specified>

-a	do JTAG test
-t	do interrupt tests
-i	do WX - IRAM test
-w	do WX - WRAM test
-x	do XILINX test
-j	do DCC - IRAM test
-f	do foreground WRAM test
-b	do background WRAM test
-d	do foreground write background read test
-p	do QRAM tests

Sample of the screen view after running DCCDIAG V2.01 with no errors:

```
WRAM test size = 6M or 8M
Testing Card <num>     (shows number of cards to be tested)
Test bus integrity via JTAG
Test DSP -> WX interrupt via JTAG
Test WX -> DSP interrupt via JTAG
Test IRAM - WX: WA
Test IRAM - WX: RN
Test WRAM - WX: WA
Load  XILINX
Test IRAM - DSP : FFFFFFFF/00000000
Test IRAM - DSP : 55555555/AAAAAAAA
Test IRAM - DSP : WA
Test IRAM - DSP : RN
Test IRAM - DSP : 55555555/AAAAAAAA & WX: WA
Test IRAM - DSP : 55555555/AAAAAAAA & WX: RN
Test IRAM - DSP : RN & WX: RN
Test WRAM - DSP : FOREGROUND: 5555/AAAA
Test WRAM - DSP : FOREGROUND: WA
Test WRAM - DSP : FOREGROUND: RN
Test WRAM - DSP : FOREGROUND: RN & WX: WA (SAME BANK)

Test WRAM - DSP : FOREGROUND: RN & WX: WA (SEPARATE BANKS)
Test WRAM - DSP : FGWRITE/BGREAD: RN
Test WRAM - DSP : FGWRITE/BGREAD: WA
Test WRAM - DSP : FGWRITE/BGREAD: WA & WX: WA (SAME BANK)
Test WRAM - DSP : FGWRITE/BGREAD: RN & WX: WA (SAME BANK)
Test WRAM - DSP : FGWRITE/BGREAD: WA & WX: WA (SEPERATE BANK)
Test WRAM - DSP : FGWRITE/BGREAD: RN & WX: WA (SEPERATE BANK)
Test WRAM - DSP : BACKGROUND: AAAA/5555
Test WRAM - DSP : BACKGROUND: 5555/AAAA & WX: WA (SAME BANK)
Test WRAM - DSP : BACKGROUND: 5555/AAAA & WX: WA (SEPERATE BANK)
Test QRAM - HIGH 24 BITS : 555555/AAAAAA
Test QRAM - HIGH 24 BITS : RN
Test QRAM - LOW 24 BITS : 555555/AAAAAA
Test QRAM - LOW 24 BITS : RN
```

14.4.3 DCC PLL Adjustment

1. Insert extender card into a vacant DCC slot.
2. Insert DCC card to be tested into extender card.
3. Turn on unit.
4. Set DVM to DC volts 20v range. Setup PLL as follows:
5. Measure the DC voltage between test points TP 9 & TP 10 (pins 8 and 7 of U26).
6. Adjust C13 (6-45pf variable capacitor) for a voltage of 1.8v to 2.3v DC (2 - 2.1v dc nom). This adjustment is critical. If when adjusting, the voltage is very unstable and hard to get in the 2-2.1v range, replace the cap. When adjusting the cap, the change in voltage should be smooth with no major changes in level.
7. Turn off unit.
8. Remove extender card and re-insert DCC card into unit.

14.4.4 DCC Led Indicators

The DCC Leds diplay the following signals:

RESET	Reset
LWIRQ	IRQ to WFM
MASKA	Accessing DCC WRAM
WACCL	WFM to DCC
DACC	DCC to DRAM
IRQ0	IRQ to DCC
MSTR	Card selected as AES input sync source
FLAG0	Debug - shows ‘in play’

14.4.5 DCC Debug Masks

Errors generated by the DCCs will produce a hexadecimal value identifying the card(s) which produced the problem. These errors are displayed at the top of the MFX screen or on the Blue <z> debug page.

To generate the mask value, each card is represented by a bit, with the resulting byte being derived by ‘OR ing’ all the DCC mask bits. The values are as follows:

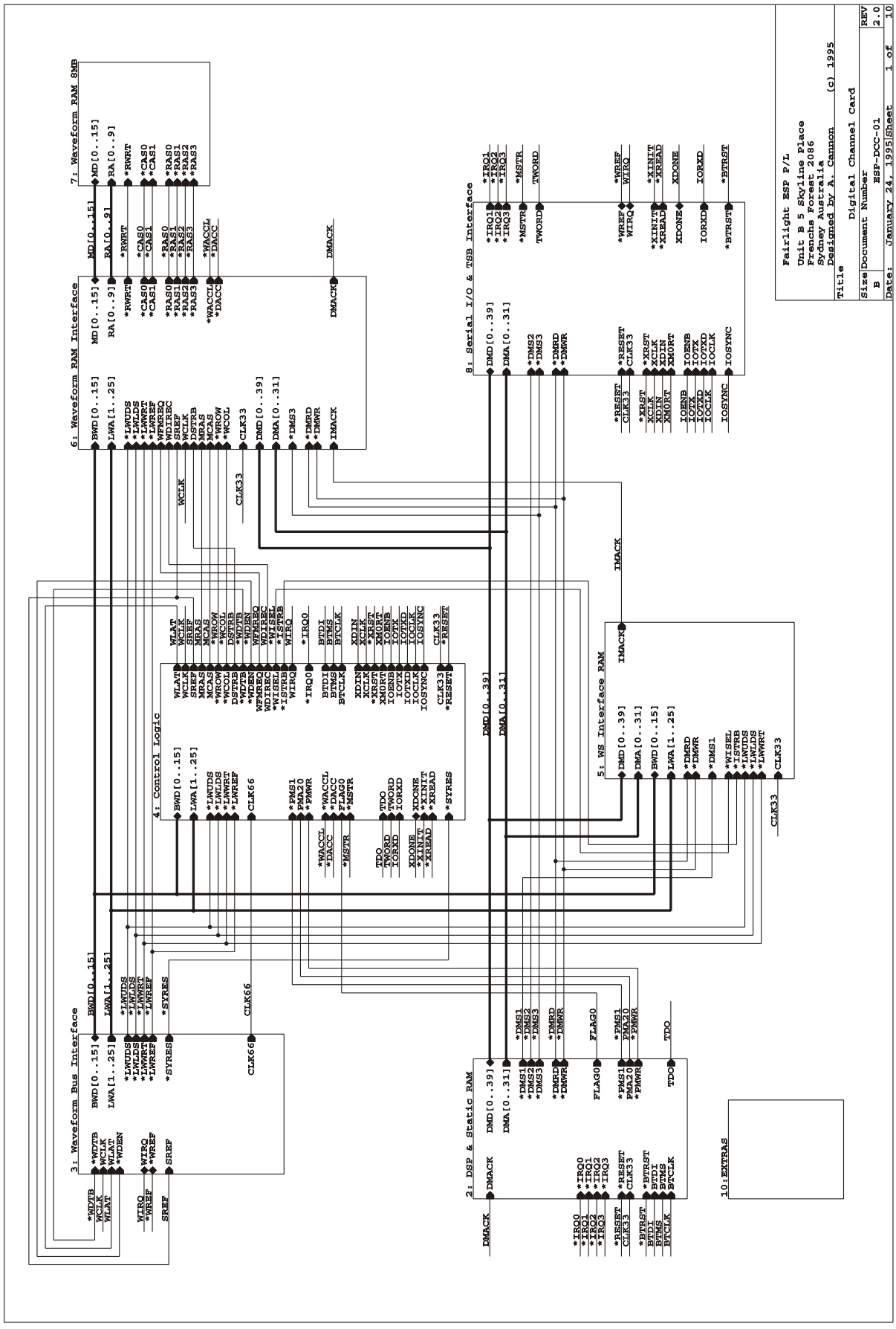
DCC	Mask	Hex
DCC 0	00000001	H01
DCC 1	00000010	H02
DCC 2	00000100	H04
DCC 3	00001000	H08
DCC 4	00010000	H10
DCC 5	00100000	H20
DCC 6	01000000	H40
DCC 7	10000000	H80

For example, if an error produces a mask value of H04, the 3rd DCC (DCC 2) reported the fault. If a mask value of H3f is reported, it came from all six DCCs of a 24 track MFX.

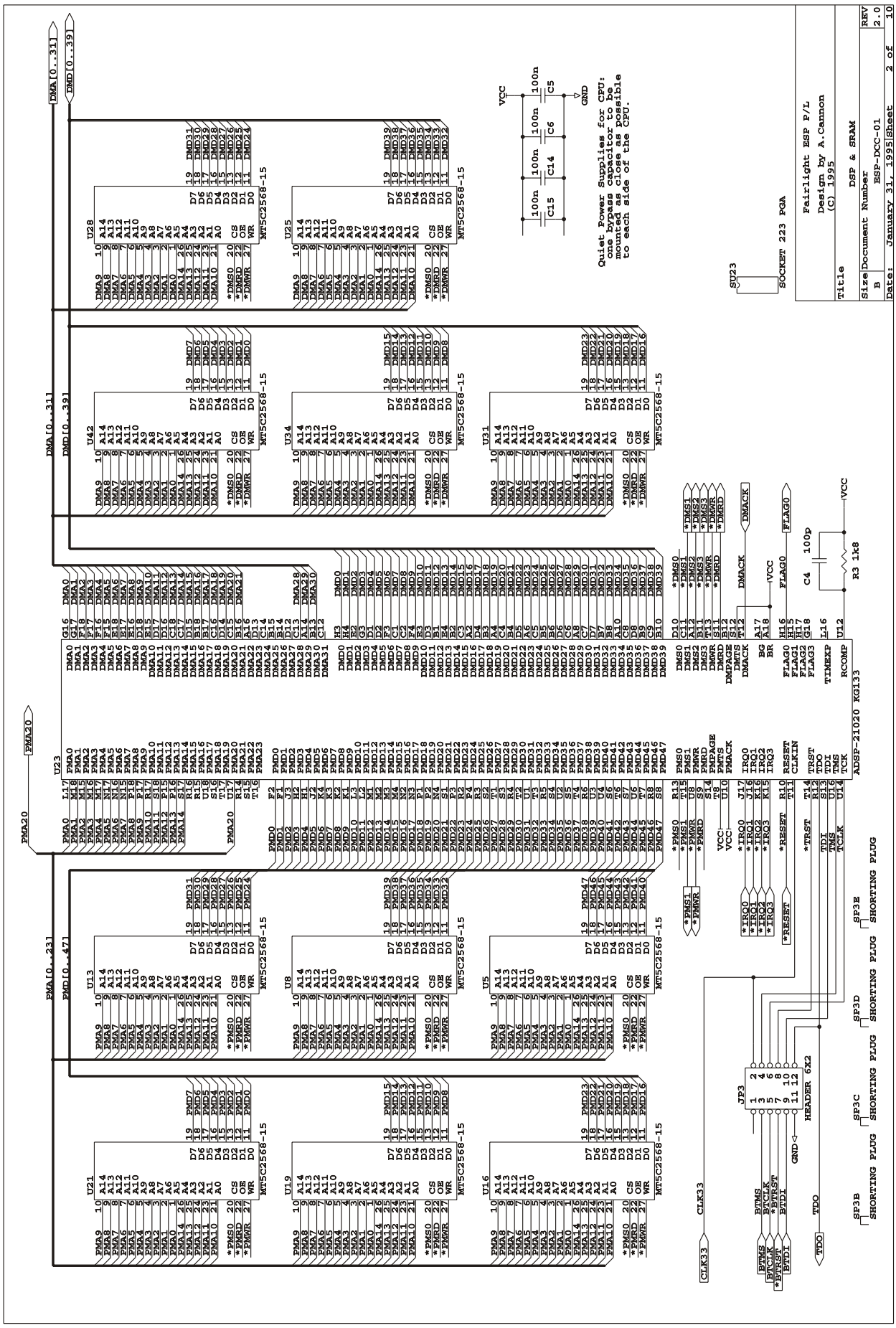
See section 14.3 for more details on DCC addressing.

14.5 ESPDCC Schematics

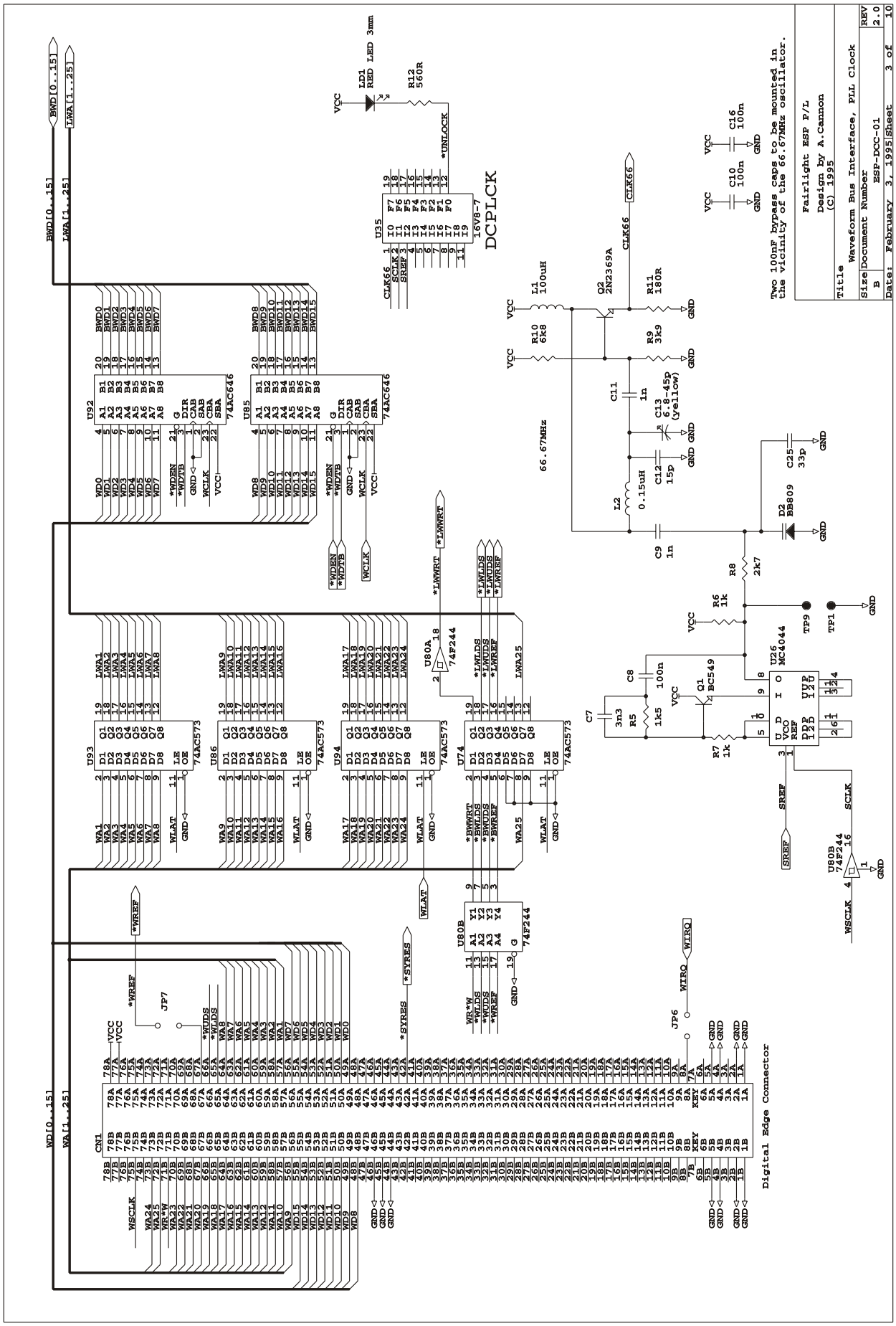
14.5.1 ESPDCC Interconnecting Diagram



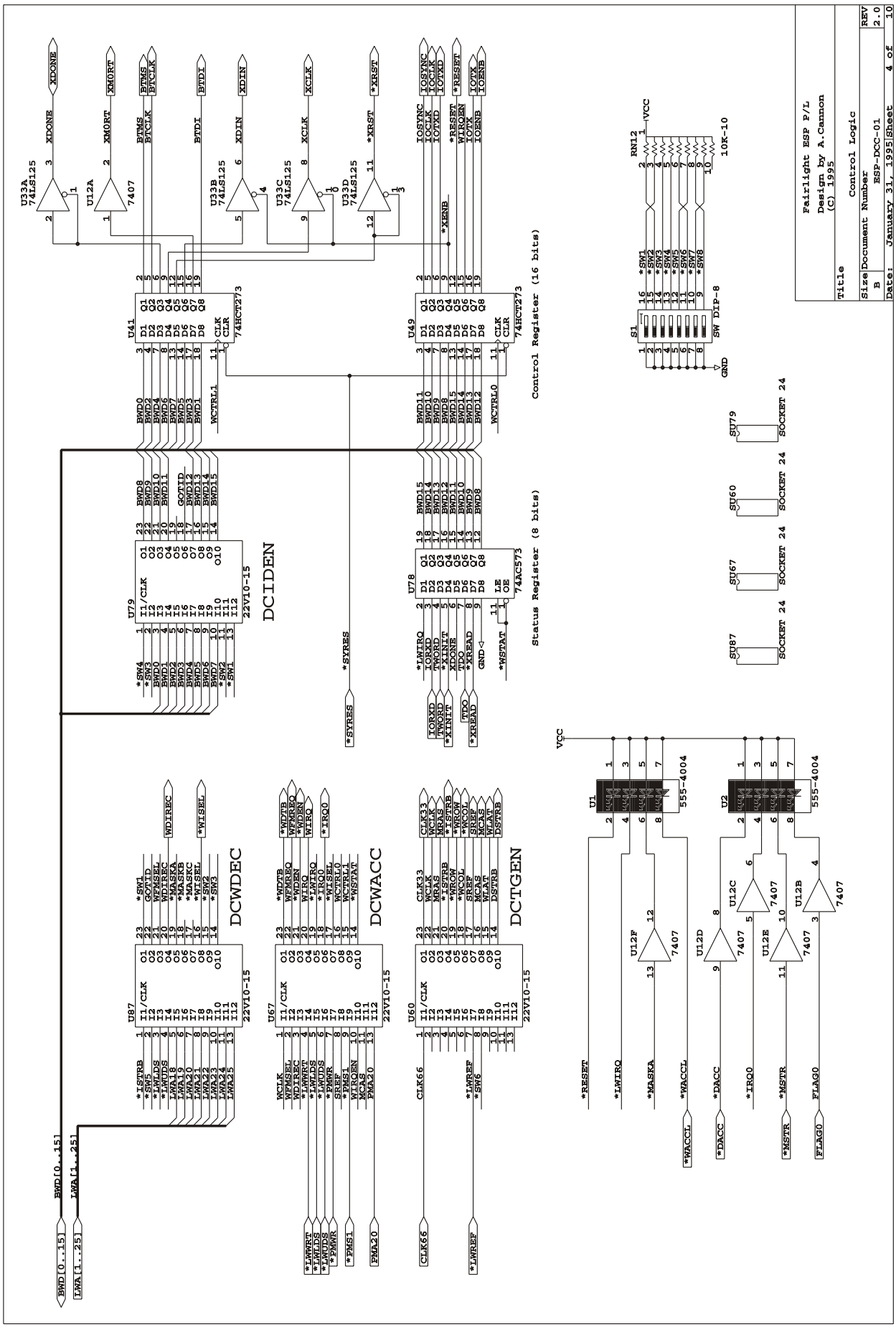
14.5.2 DSP AND SRAM



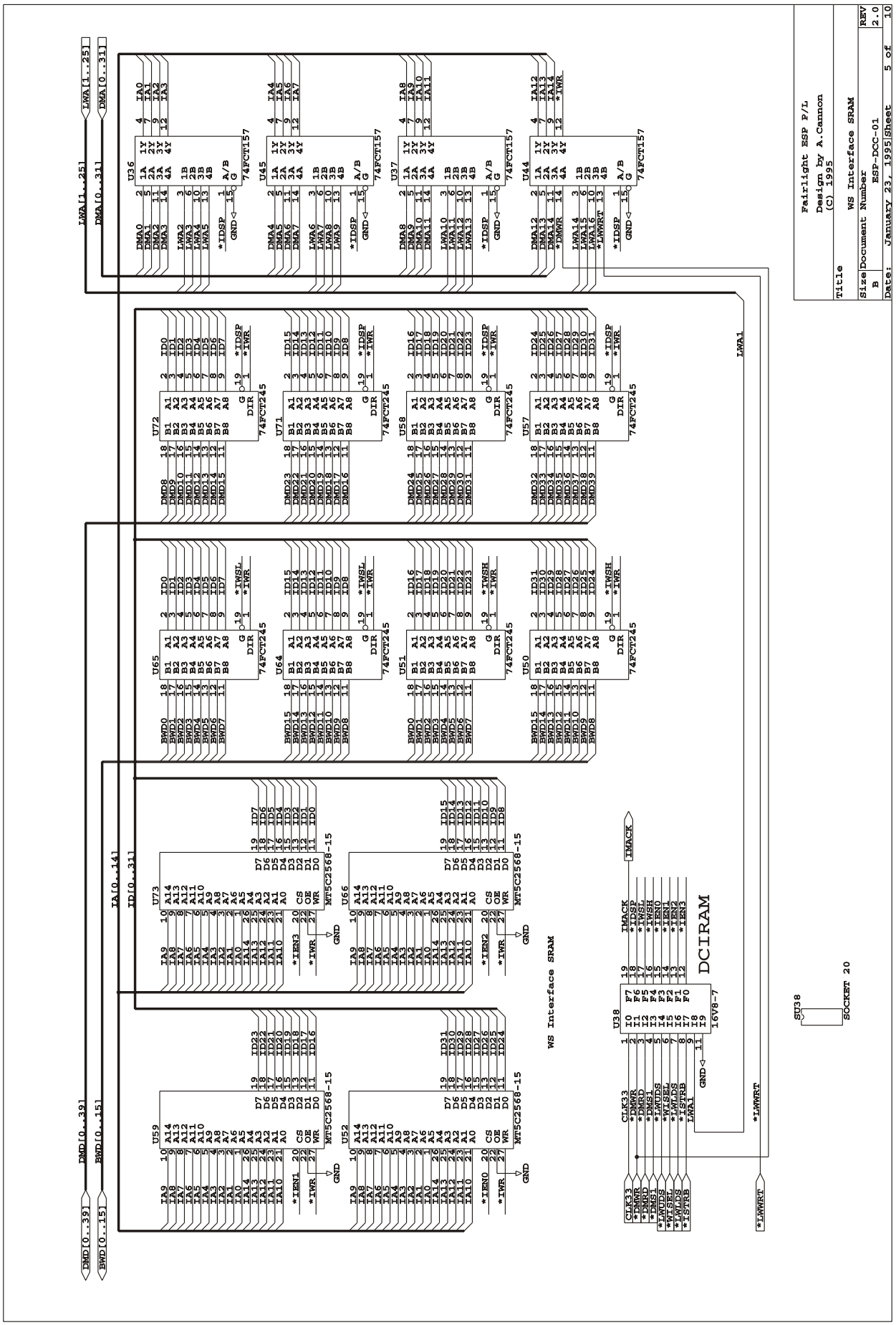
14.5.3 Waveform Bus Interface, PLL Clock



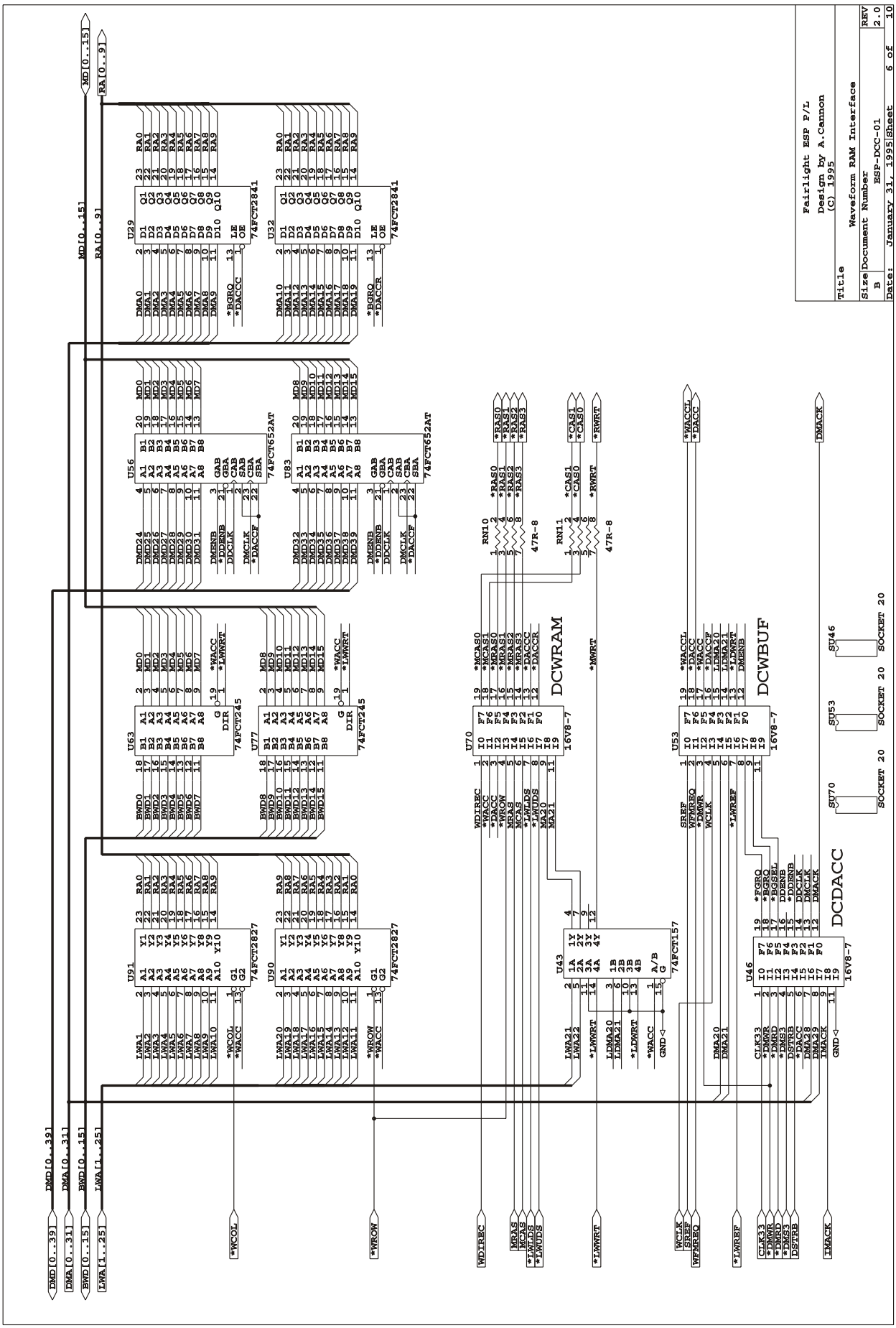
14.5.4 CONTROL LOGIC



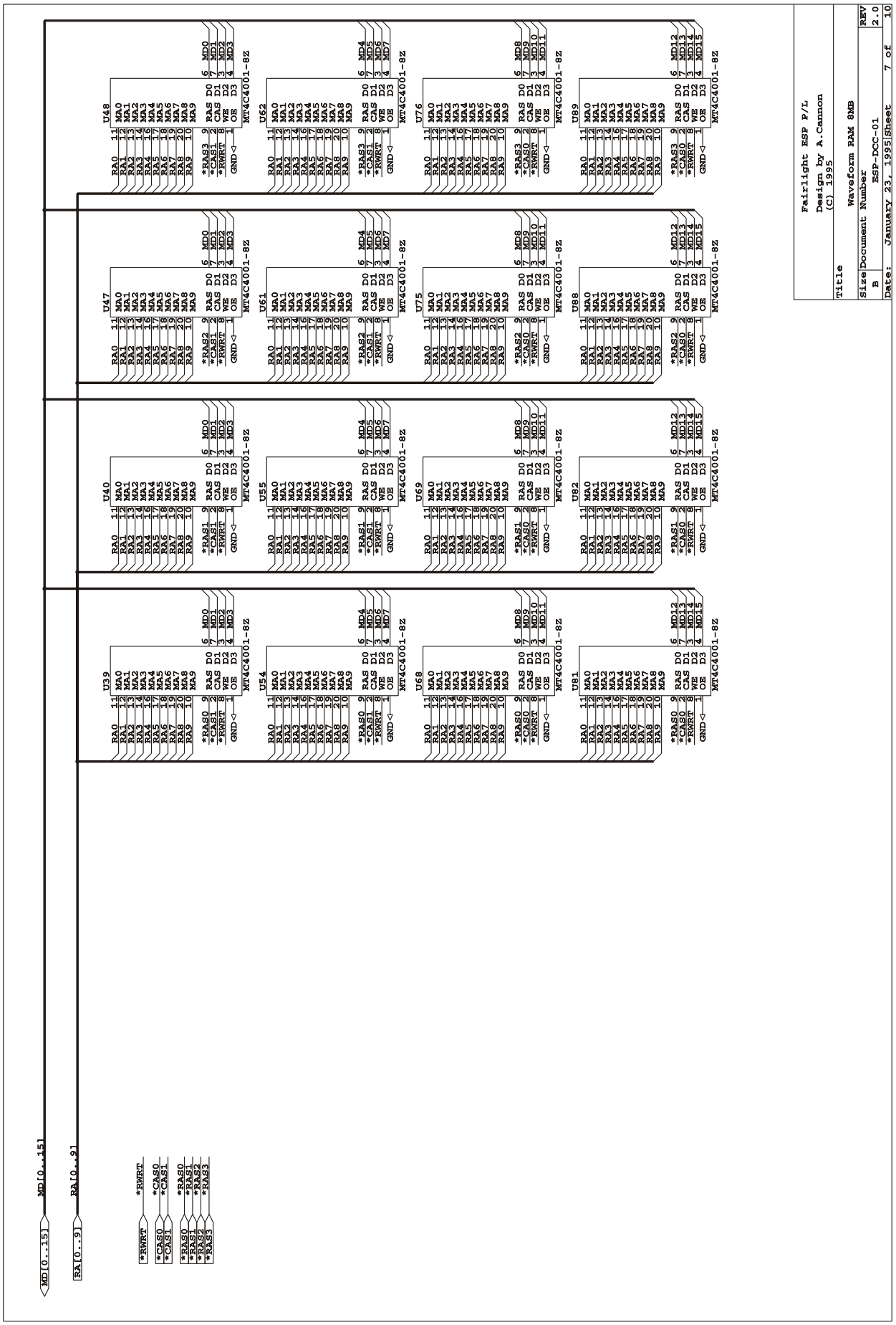
14.5.5 WS Interface SRAM



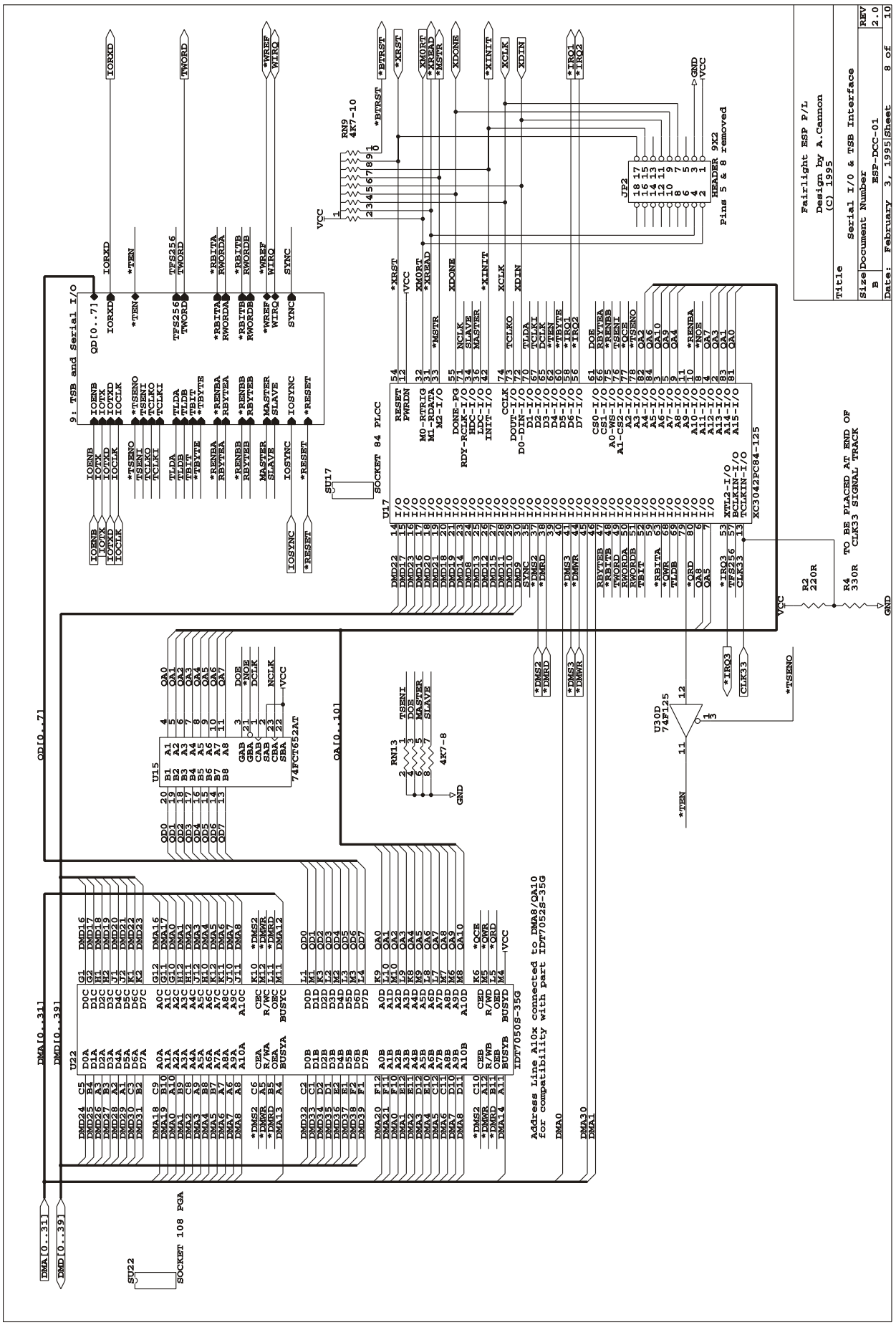
14.5.6 WAVEFORM RAM INTERFACE



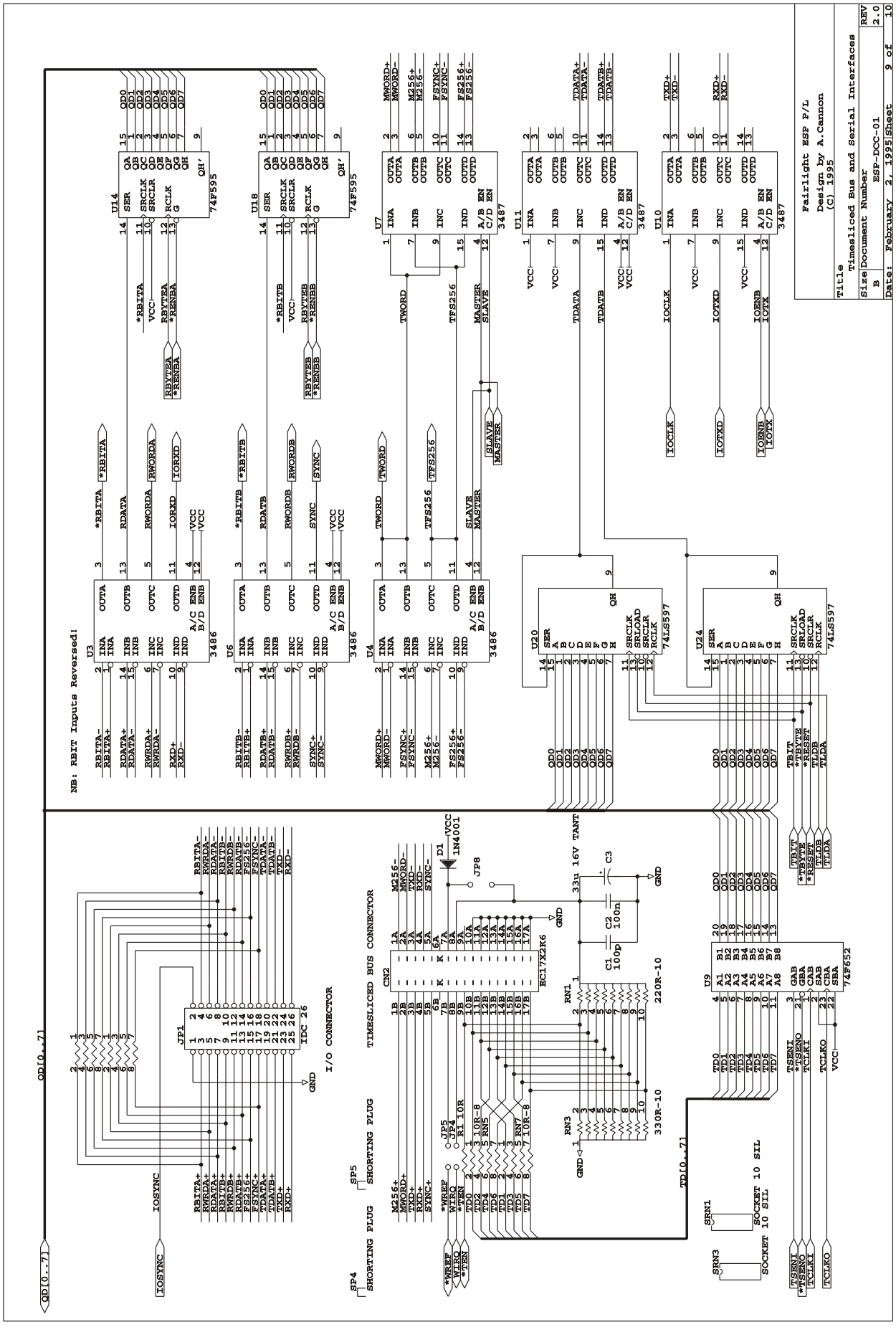
14.5.7 WAVEFORM RAM 8MB



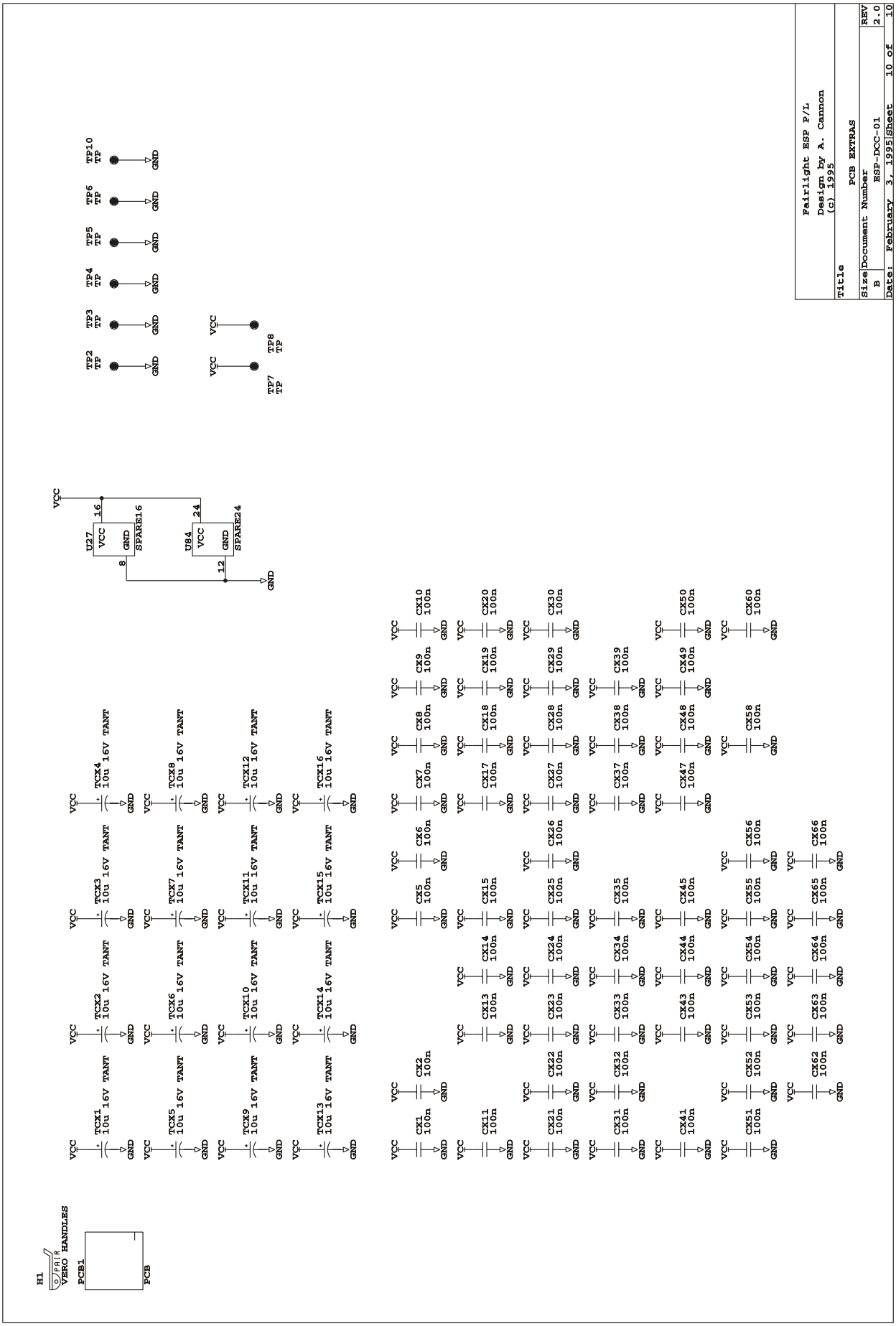
14.5.8 Serial I/O and TSB Interface



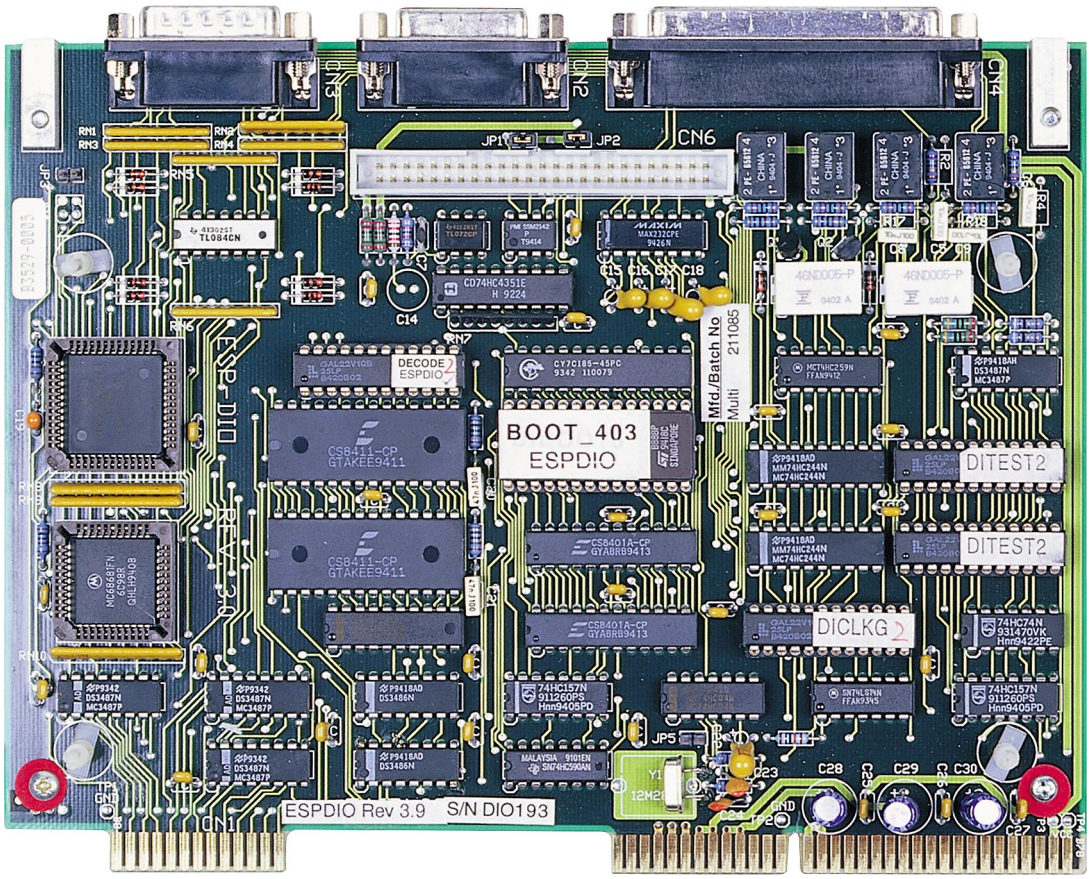
14.5.9 Timesliced Bus and Serial Interfaces



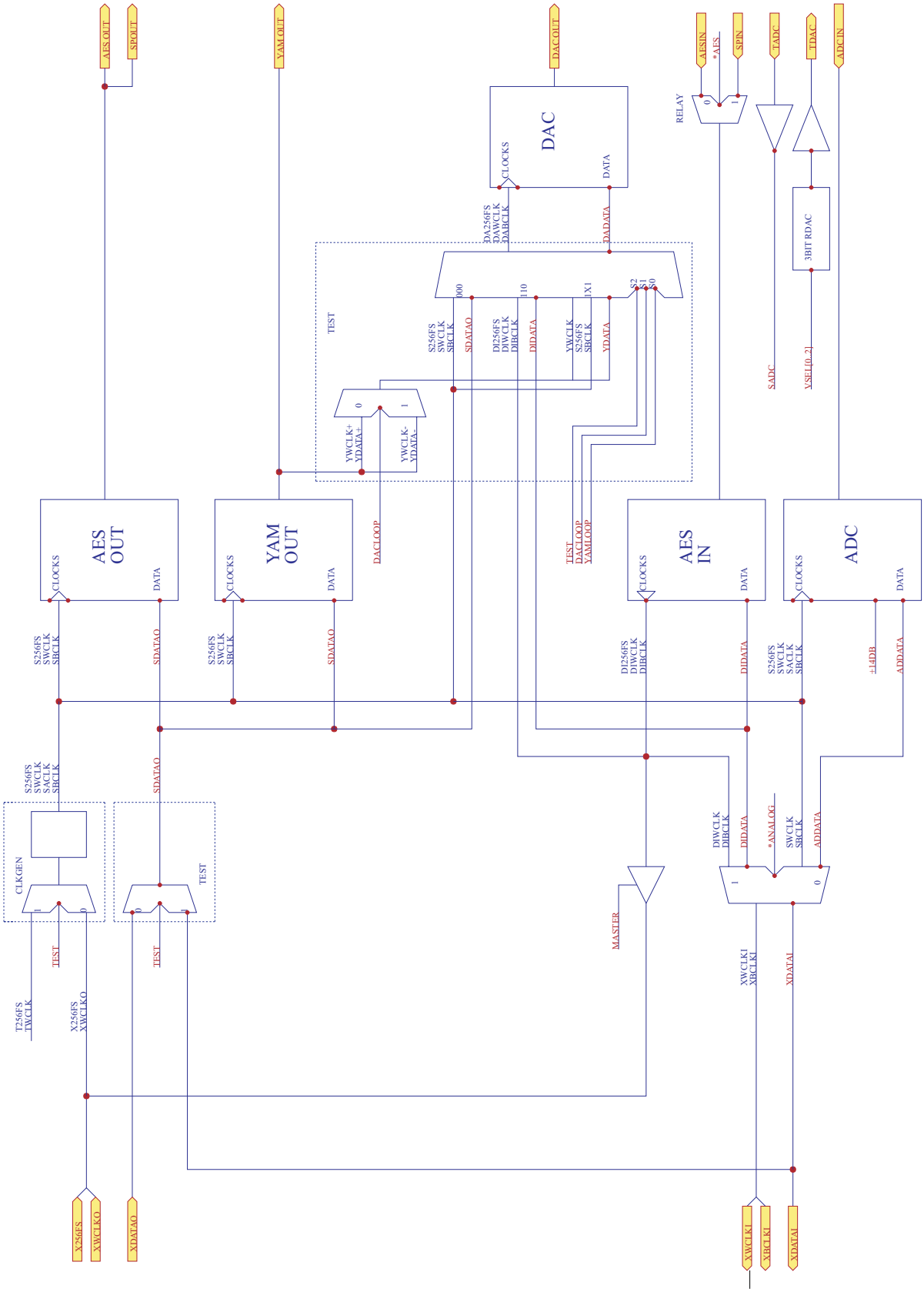
14.5.10 PCB EXTRAS



15.0 ESPDIO Digital I/O Card



15.1 ESPDIO Block Diagram



15.2 ESPDIO Circuit Description

15.2.1 CPU Operation

*PDRST U10/17(68HC11) Power down reset, approx 350mS low pulse. Test by shorting JP5. 6M144 U10/7 (68HC11) 6.144 MHz CPU crystal clock input E U10/5 (68HC11) 1.536 MHz (6M144 / 4) CPU clock. Always present when 68HC11 operational. AS U20/11(74HC373) 163nS high, 488nS low. Always present when 68HC11 operational.

The 68HC11 has a multiplexed address and data buss. When AS is high, D0-7 hold the lower address lines A0-7 which are latched on falling AS by U20 (74HC373). Write data from the CPU is valid at the rising edge of E, and remains valid while E is high. Read data is latched by the CPU on the falling edge of E.

15.2.2 Booting Procedure

1. Read reset vector from addresses $FFFE and $FFFF from eprom (*ROM asserted). The byte read from $FFFE should be $E0. The byte read from $FFFF will depend upon the eprom revision.

2. Read $0F from the eprom (at the reset vector). This is the first instruction (disable interrupts).

3. Read from *RAM.

   Read from *DIGIN0.

   Read from *DIGIN1.

   Read from *DIGOUT0.

   Read from *DIGOUT1.

   Read from *CTRL.

   Read from *ACIA.

   Read from *ROM.

4. Some initialisation occurs for approx 100uS which depends on the eprom revision. There will be activity on all DECODE pal outputs.

5. Once the initialisation is completed, *ROM and *ACIA signals will be strobing.

15.2.3 Communications to SC.

The SC controls the DIO via a multidrop RS422 interface. The DUART on the SC has serial port B dedicated to this purpose.

The transmit to the DIO is sent via the TSB cable to every DCC. The DCCs directly connect the transmit to the 26way connectors to their correcsponding DIO module. All DIO modules

receive the same data.

The receive lines are similarly bussed, however, only one DIO will transmit on this line at any one time. Pullups on the SC hold the line in the idle state (input to duart is high) when no card is transmitting.

As the transmit to the DCC is bussed, each DIO card has a TXEN transmit enable signal which is asserted only during its own transmission.

After the DCCs have been initialised in MDR, the DIO cards are initialised. During this sequence the third from top led on the DCC will light for 200mS on each DCC in succession. If the LED stays on for longer then the corresponding DIO is not responding correctly. During the period the LED is on, the corresponding IOSYNC line will be asserted on the 26way cable to the DIO.

15.2.4 DIO COMMANDS

The DIO cards can communicate to the SC via the DCCs and via a debugging serial port on the DIGITAL IO connector (pin 2 TX from DIO, pin 20 RX to DIO, pin 1 GND). Communications are monitored on both ports to allow in-system debugging. The protocol on both communication paths are identical, except for the RESET command which is always serviced from the debugging serial port. These ports operate at 19200 baud, 8 bits, 1 stop bit, no parity.

Commands are ascii characters, and the parameters are sent as ascii encoded hex. This allows debugging using only a serial communication program. The basic format of commands is:

<command character> <mask> <parameters> ...

The <command character> is one for the commands listed below. The <id> is a 2 ascii code byte mask of cards to execute the command. Each card is given its own identification during the RESET command which should have only one bit set. The DIO cards all listen to commands but only process them if the logical AND of the <mask> and their own identification is non-zero. All parameters are 2 ascii character encoded bytes. For some commands, ascii encoded data is returned - in this case only one card should be selected for the command to stop transmission contention.

The exception to the command format above is the RESET command which is of the format:

IOSYNC=HIGH <reset command> <id> {<reset command> echoed by DIO}

When the DIO receives the RESET command it is immediately processed and previous commands are aborted. The card which has its IOSYNC line asserted will set its identification to <id> and echo the RESET command character.

Like the RESET command, a STATUS command may be issued at any time. STATUS returns the following codes:

#	illegal command recevied
?	illegal parameter received
!	communications error
<command character>	last successfully executed command

Once one of the error conditions occur (#,!,?), the DIO will stop processing commands until a STATUS or RESET command. The STATUS command will echo the error code and resume processing commands. If a second STATUS command is issued, the status command itself will be echoed indicating the last successful command.

Command format

Key:

<mask>	card selection mask	(2 ascii digits)
<id>	card identification	(2 ascii digits)
	only one bit set in byte	
<addr>	16 bit address	(4 ascii digits)
<data>	8 bit data	(2 ascii digits)
<string>	$ terminated ascii string	
{...}	echoed data by DIO	
[...]	software equate names	

RESET

IOSYNC Z <id> {Z}

Abort any command processing. If IOSYNC is asserted to card, set card identification to <id> and echo Z. This command

must be issued before any other command.

STATUS

^ <id> {#,?,!,last successful command code}

Abort any command processing. Return the current status code. If a command is aborted, either # or ? will be returned to indicate where command was interrupted. Normally, this command is issued when it is thought that the DIO is not processing a command to check that the protocol is in sync. Only one card should be selected by <id>.

READ

R <id> <addr> {<data>}

Read <data> from address <addr>. Only one card should be selectedby <id>.

WRITE

W <mask> <addr> <data>

Write <data> to address <addr>

JUMP

J <mask> <addr>

Jump to address <addr> and start execution.

ANALOG INPUT LEVEL

L <mask> <input> <level>

Set analog input attenuator on <input> to <level>. <input> should be 0..3, and <level> is 00..FF in 0.5dB steps where C0 is 0dB gain.

INPUT SOURCE

I <mask> <port> <source>

Set input source on stereo pair <port> to <source>. <port> = 0

applies to inputs 0..1, and <port> = 1 applies to inputs 2..3.

The possible <source> values are:

00	analog input from A/D converter	[I_ADC]
01	AES digital input	[I_AES]
02	SPDIF digital input	[I_SPDIF]

Extra modes used for debugging:

03	AES input driven from internal DIO crystal	[I_XAES]
04	SPDIF input driven from internal DIO crystal	[I_XSPDIF]

OUTPUT SOURCE

O <mask> <output>

Set output source on card to <source>. Possible values for

<source> are:

00	data from ESP-DCC card to output	[O_DCC]
07	mute output	[O_MUTE]

Extra modes for debugging:

01	from A/D converter (analog loopback)	[O_ADC]
02	from digital in (digital loopback)	[O_DIGIN]
03	Yamaha Interface +ve (yamaha loopback)	[O_YAMP]
04	Yamaha Interface -ve (yamaha loopback)	[O_YAMN]

SYNC (clocking) SOURCE

S <mask> <source>

Set clocking sync source for card to <source>. Possible values

for <source> are:

00	from ESP-SYN card via ESP-DCC	[S_EXT]
01	from digital input port 0	[S_DIG0]
02	from digital input port 1	[S_DIG1]
	Extra debugging modes:	
03	from DIO crystal	[S_XTAL]
04	digital out from xtal,input from digital in port 0	[S_XDIG0]
05	digital out from xtal,input from digital in port 1	[S_XDIG1]

READ FROM EEPROM

N <id> <addr> {<data>}

Read <data> from DIO EEPROM offset address <addr>. Unlike writing to the EEPROM, this may be done as many times as you like.

READ FROM EEPROM

M <mask> <addr> <data>

Write <data> to EEPROM address offset <addr>. This should be used sparingly as there is a 10000 write cycle life of the EEPROM.

GET ROM IDENTIFICATION STRING

X <id> {<string>}

Sends DIO BOOT ROM identification string and copyright information as a $ terminated string.

ENABLE DEBUG PORT

+ <mask>

Enables debug printed during command processing to the debug port accessable to an external terminal or PC. As the output

data is buffered, characters can be delayed to the debug port. If the buffer is overrun, extra debug characters are lost.

DISABLE DEBUG PORT

- <mask>

Disable any debug output.

CALIBRATE ANALOG

~ <mask>

Reset and calibrate the A/D and D/A converters - this takes about 200mS to complete. This command should be issued on

initialisation and whenever the sample clocks are changed. The calibration resets the A/D and D/A processing and nulls

any DC offsets on the A/D converter.

NO OPERATION COMMAND

* <id> {*}

Echoes its own command code as a protocol confidence check.

DOWNLOAD

_ <mask> <addr> <count> <data> ... <checksum>

Down load data stream of length <count> starting at address <addr>. <count> is a 4 ascii 16 bit count of data bytes to

follow. <checksum> is the modulo 256 sum of the data bytes. If the <checksum> does not correspond the the DIO calculation,

the error code is set to ?.

15.3 ESPDIO DIAGNOSTICS

DIO.EXE Digital IO/Analog IO

Interface Software for PC.

15.3.1 INTRODUCTION

DIO.EXE is a program to communicate and control the ESP-DIO Digital IO Card and ESP-AIO Analog IO Card. This program communicates via COM1 serial port to a debugging serial port on the ESP-DIO.

Cable connections

IBM PC COM1	ESP-DIO CN4
(9 pin Dsub female)	(37 pin Dsub male)
2	2
3	20
5	1

15.3.2 COMMAND DESCRIPTION

. All parameters are in HEX

. <port> = 0 for first stereo pair, 1 for second stereo pair

*	test synchronisation of interface to PC
r <addr>	read from <addr>
w <addr> <data>	write <data> to <addr>
~	recalibrate ESP-AIO card (asserts CAL signal)
s <source>	select clocking source

<source>	clocking
0	ESP-SYN card
1	digital input 0
2	digital input 1
3	ESP-DIO internal crystal (48kHz)
4	digital input 0, digital out from internal crystal
5	digital input 1, digital out from internal crystal

i <port> <source> select source of input data

<source>	input source
0	analog
1	AES
2	SPDIF
3	AES, digital out is AES
4	SPDIF, digital out is SPDIF

o <source> select source of data for output (DAC)

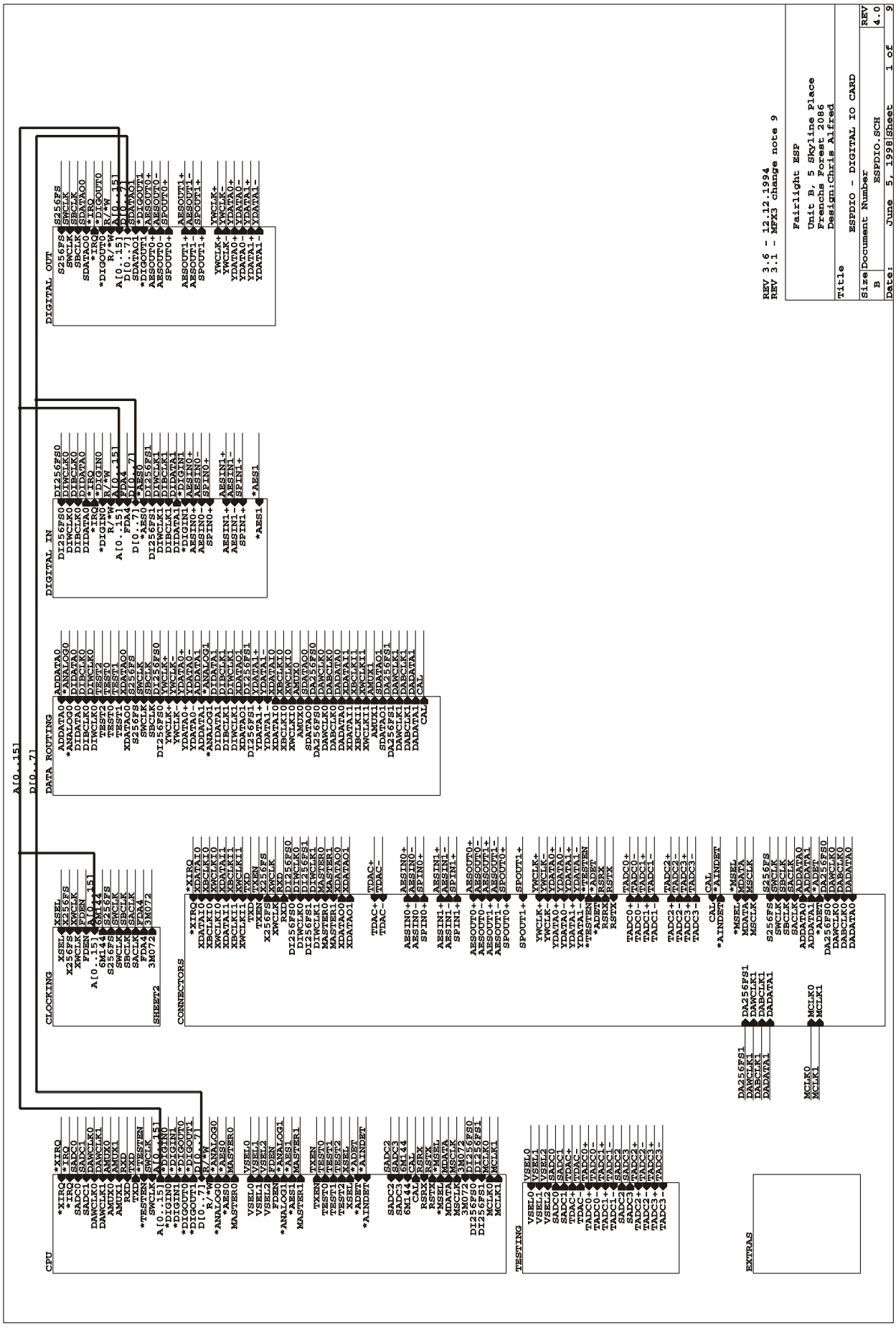
<source>	output source
0	ESP-DCC digital channel card
1	A/D converter (loops ADC to DAC)
2	Yamaha +ve
3	Yamaha -ve
7	Mute

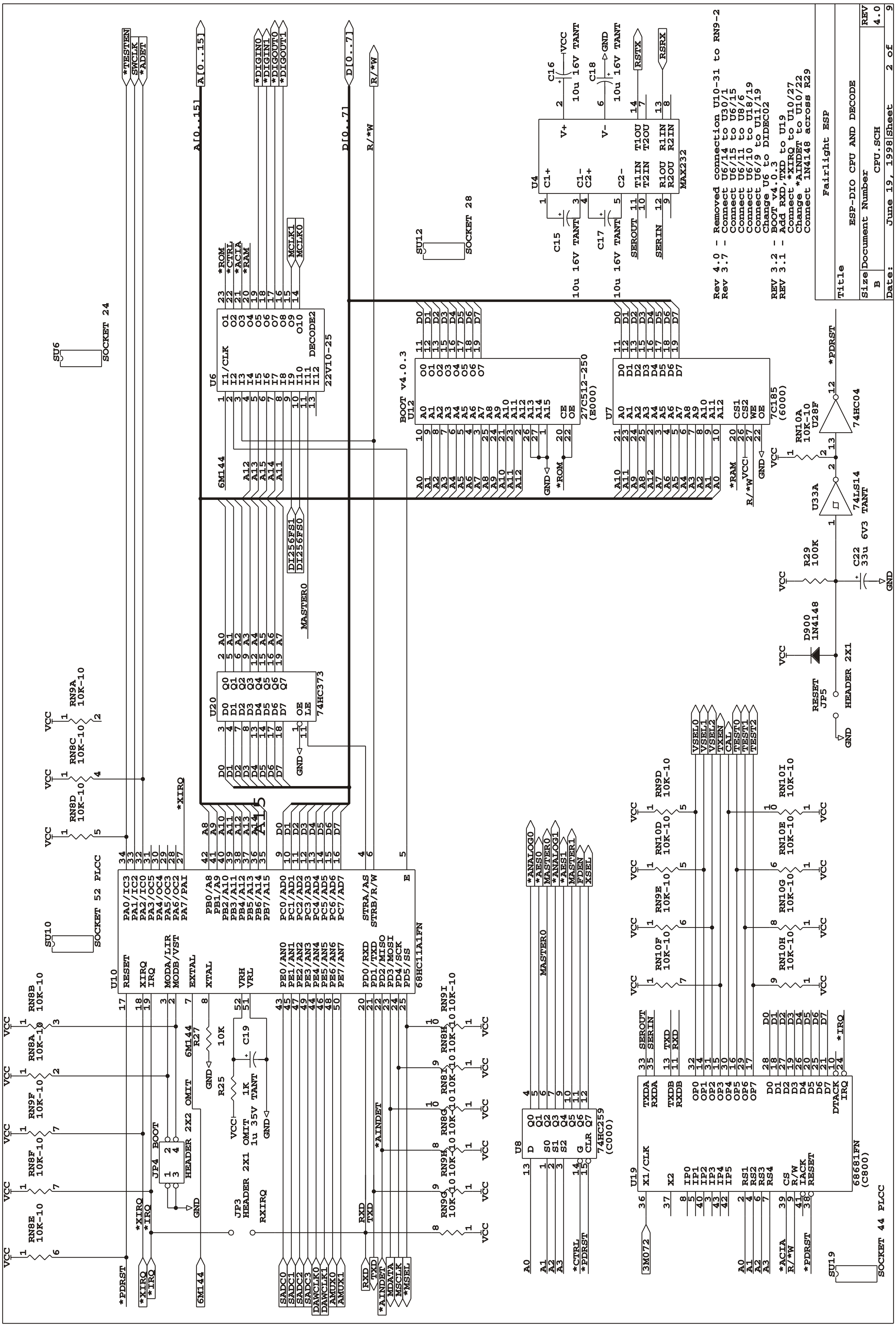
l <chan> <level>	Sets input attenuator on ESP-AIO card to <level> for channel <chan>. <level> is $00 to $FF, where 0 is mute and each step is 0.5dB to a maximum of +29.5dB gain. If <level> is $C0 the gain is 0dB.
x	send ROM identification string
d <addr> <count>	display <count> bytes starting at <addr>
f <addr> <count> <data>	fill memory for <count> bytes starting at <addr> with <data>
j <addr>	jump to address <addr> and execute
q	quit to DOS
h	print help listing
?<command>	print parameter information for command <command>

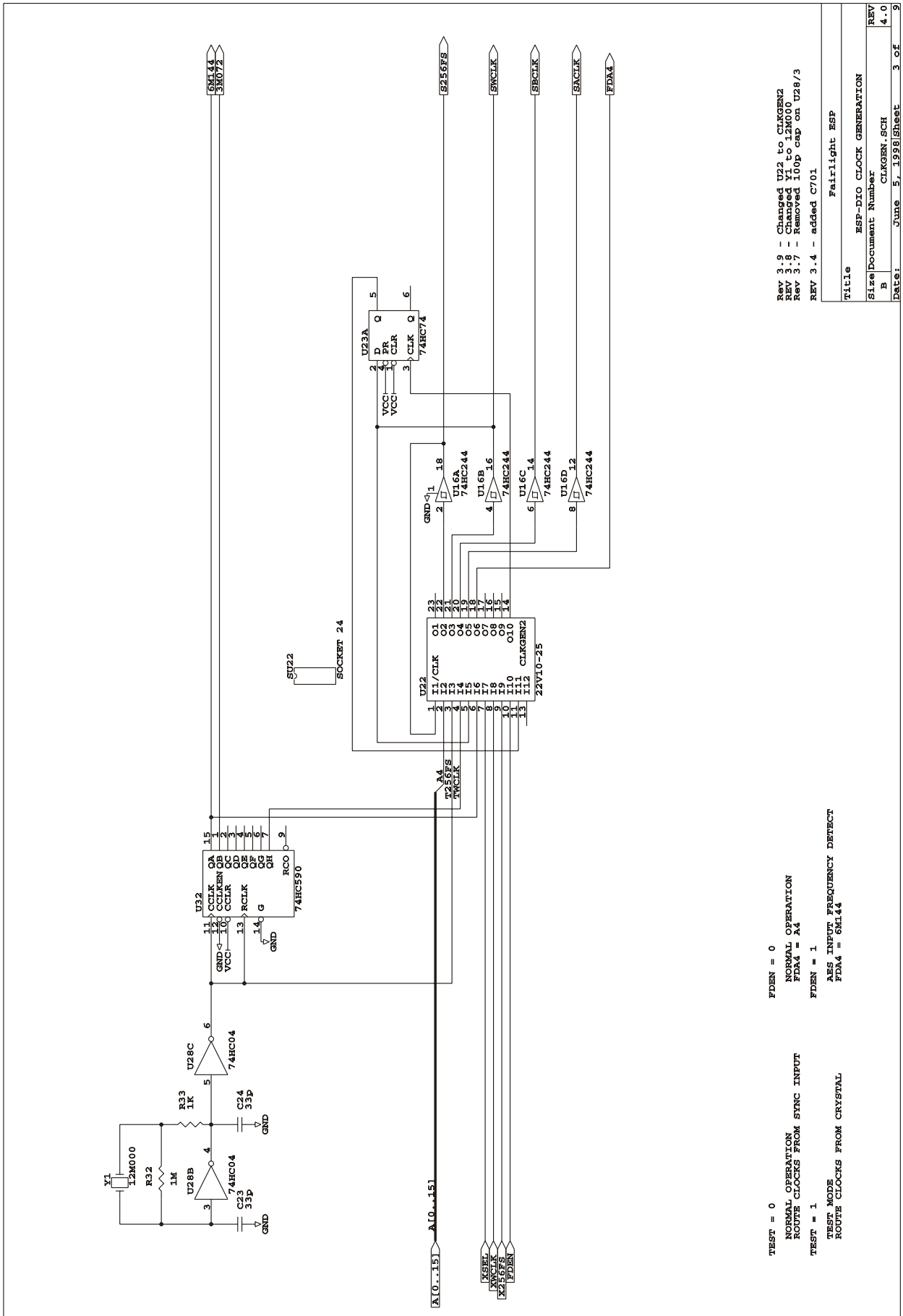
15.3.3 Additional Information

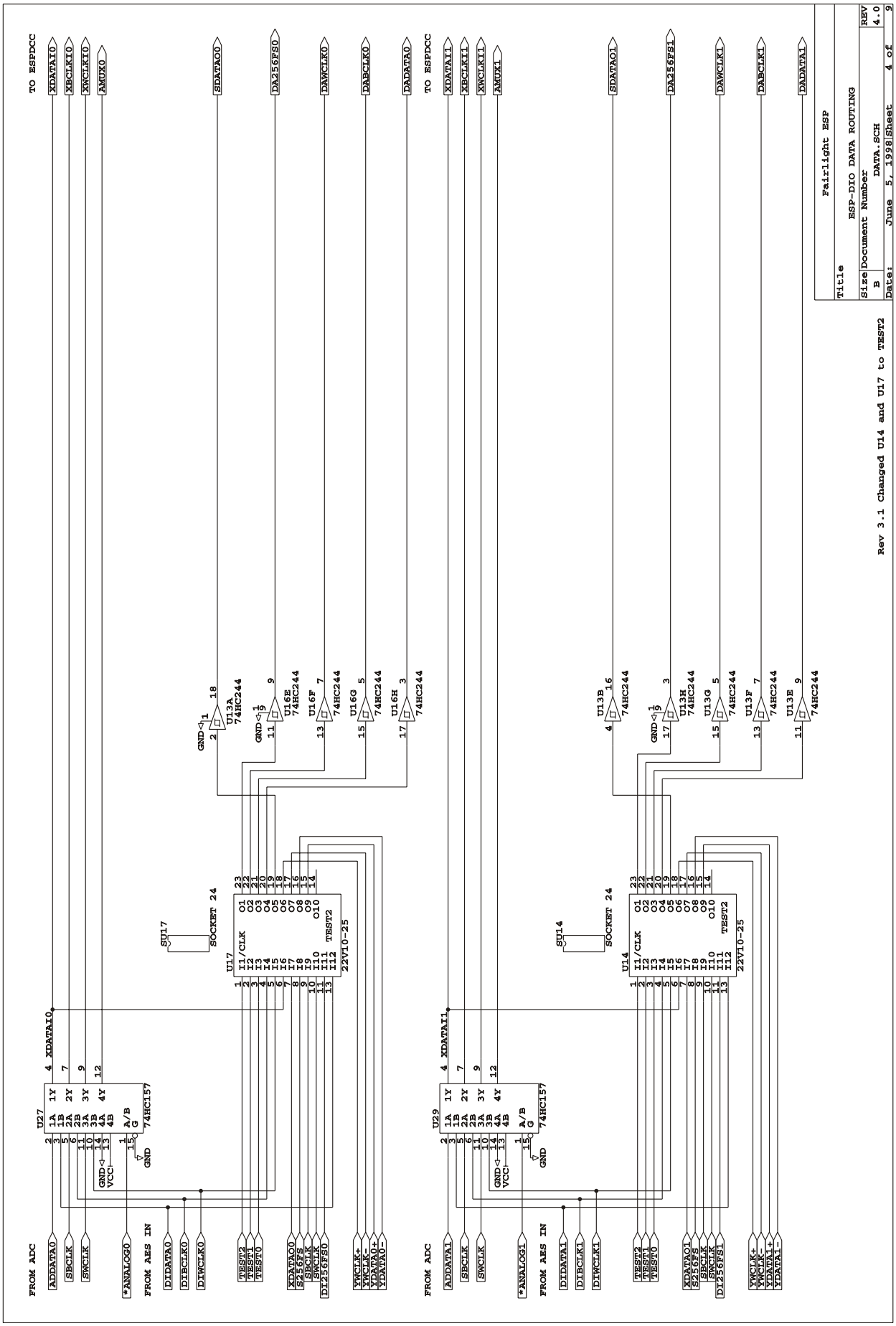
If pins 8 and 15 are shorted on CN3 of the ESP-DIO, then the card clocks from the internal ESP-DIO crystal (48kHz x 256) and loops analog input to analog output with 0dB gain.

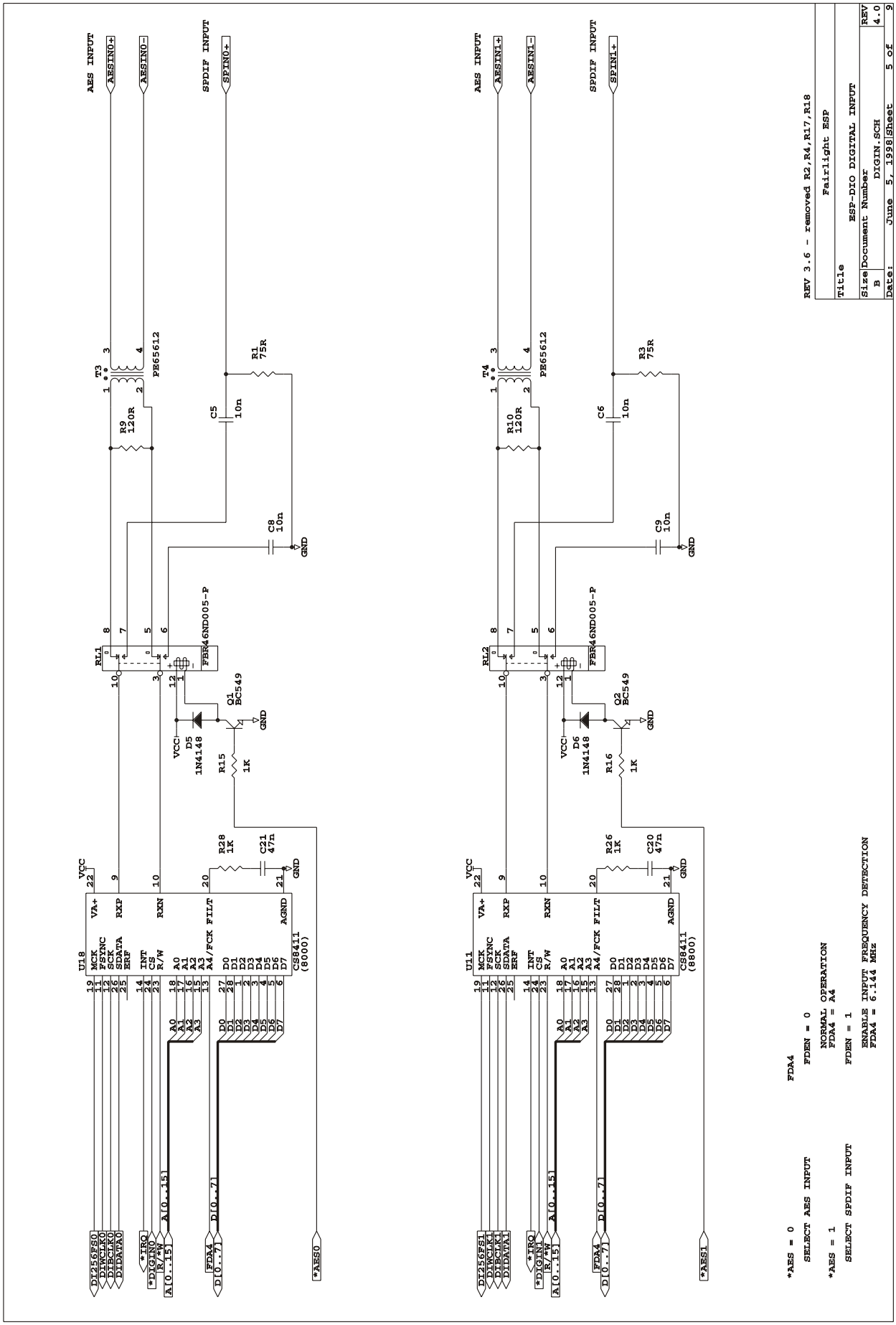
15.4 ESPDIO SCHEMATICS

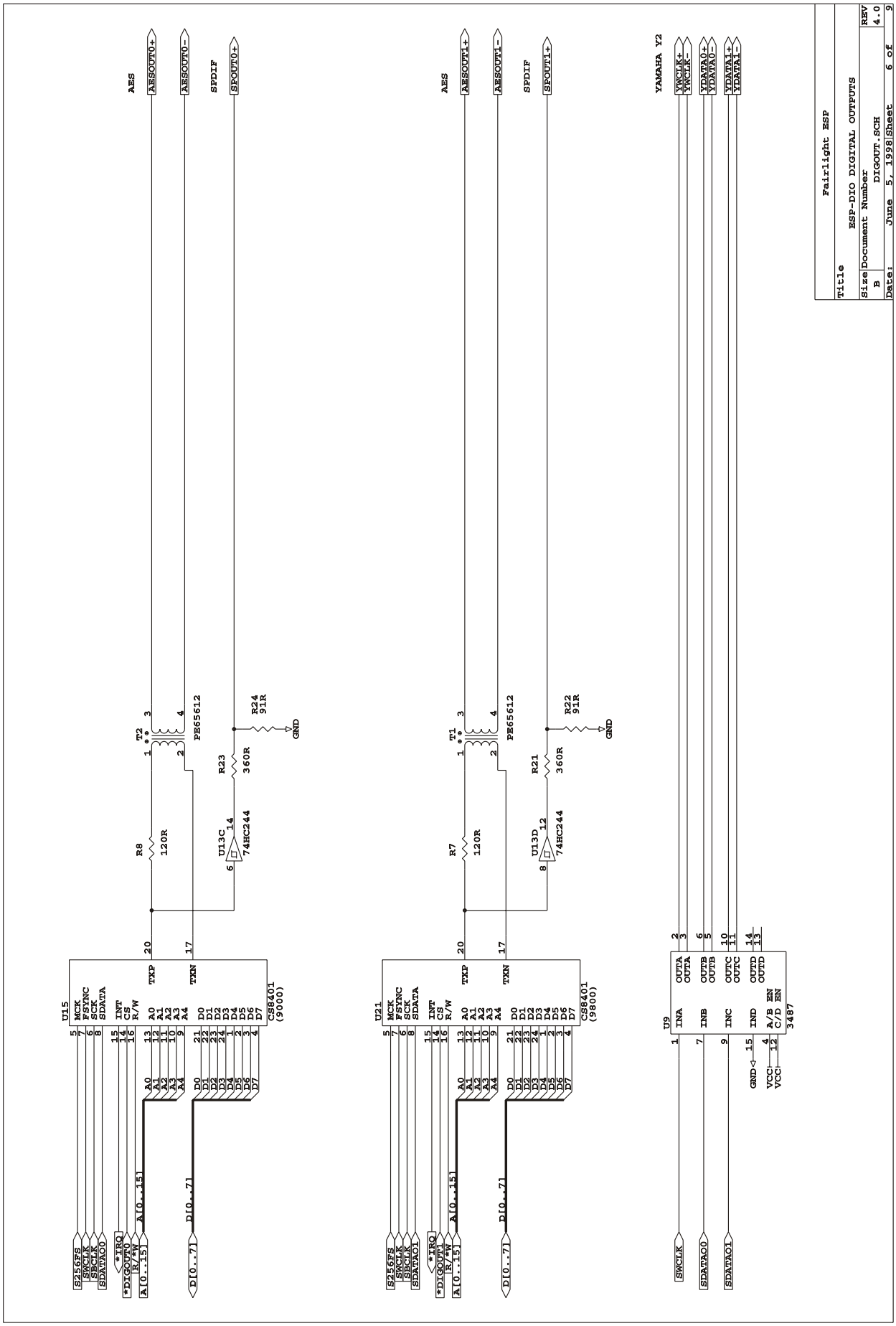


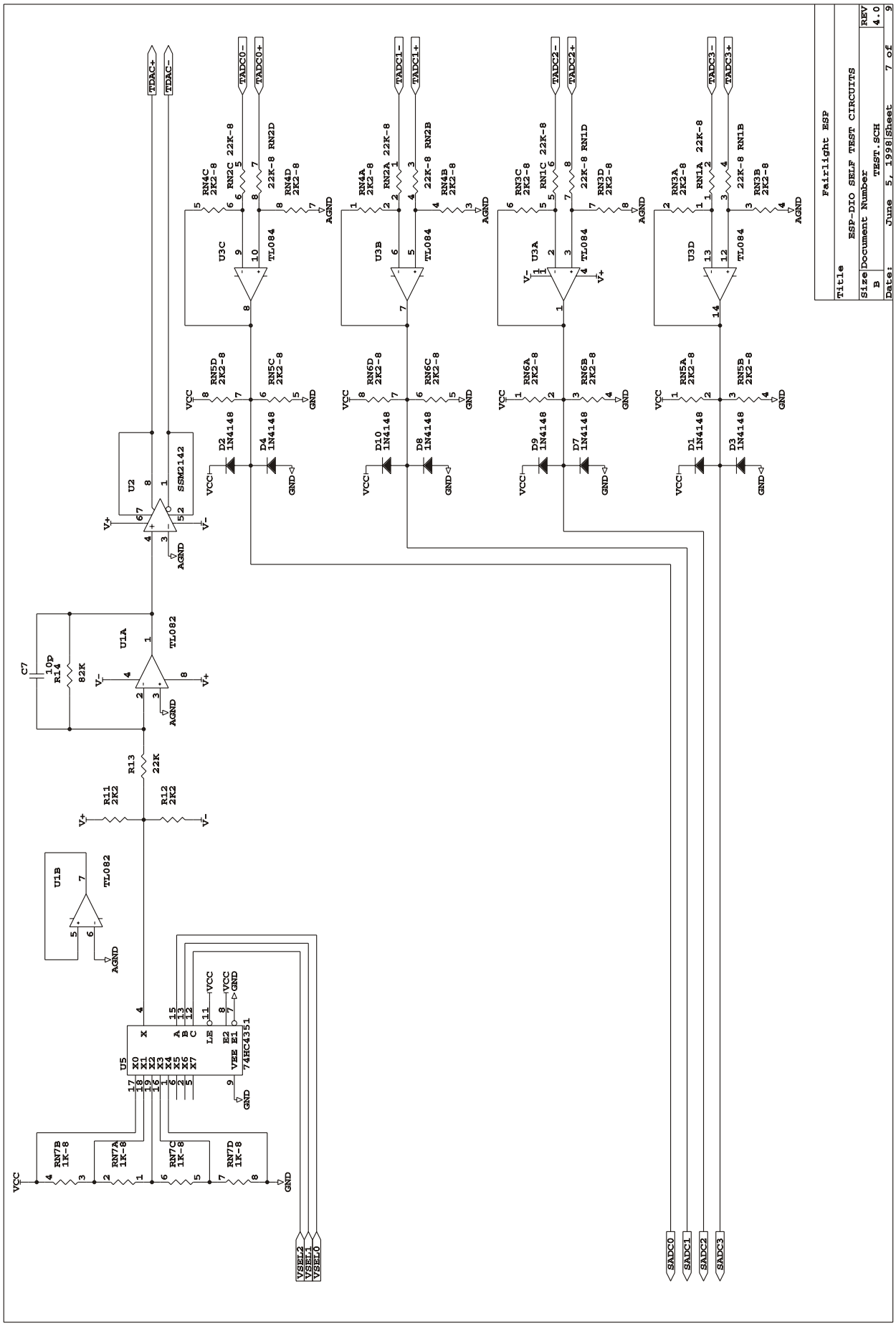

Fairlight ESP
ESP-DIO CPU AND DECODE
CPU.SCH
REV 4.0
June 19, 1998
Sheet 2 of 9


6M144
3M072
S256FS
SWCLK
SBCLK
SACLK
FDA4
U23A
74HC74
U16A
74HC244
U16B
74HC244
U16C
74HC244
U16D
74HC244
SU22
SOCKET 24
U22
22V10-25
CLKGEN2
U32
74HC590
U28C
74HC04
U28B
74HC04
R33
1K
C24
33p
R32
1M
C23
33p
Y1
12M000
GND
VCC
A[0..15]
XSEL
XWCLK
X256FS
FDEN
Rev 3.9 - Changed U22 to CLKGEN2
REV 3.8 - Changed Y1 to 12M000
Rev 3.7 - Removed 100p cap on U28/3
REV 3.4 - added C701
Fairlight ESP
Title
ESP-DIO CLOCK GENERATION
Size B
Document Number
CLKGEN.SCH
REV 4.0
Date: June 5, 1998 Sheet 3 of 9
TEST = 0
NORMAL OPERATION
ROUTE CLOCKS FROM SYNC INPUT
TEST = 1
TEST MODE
ROUTE CLOCKS FROM CRYSTAL
FDEN = 0
NORMAL OPERATION
FDA4 = A4
FDEN = 1
ABS INPUT FREQUENCY DETECT
FDA4 = 6M144


TO ESPDCC
XDATAI0
XBCLKI0
XWCLKI0
AMUX0
SDATAO0
DA256FS0
DAWCLK0
DABCLK0
DADATA0
FROM ADC
ADDATA0
SBCLK
SWCLK
*ANALOG0
FROM AES IN
DIDATA0
DIBCLK0
DIWCLK0
U27
74HC157
U17
22V10-25
SOCKET 24
U13A
U16E
U16F
U16G
U16H
74HC244
TEST2
TEST1
TEST0
XDATAO0
S256FS
SBCLK
SWCLK
DI256FS0
YWCLK+
YWCLK-
YDATA0+
YDATA0-
TO ESPDCC
XDATAI1
XBCLKI1
XWCLKI1
AMUX1
SDATAO1
DA256FS1
DAWCLK1
DABCLK1
DADATA1
FROM ADC
ADDATA1
SBCLK
SWCLK
*ANALOG1
FROM AES IN
DIDATA1
DIBCLK1
DIWCLK1
U29
74HC157
U14
22V10-25
SOCKET 24
U13B
U13H
U13G
U13F
U13E
74HC244
TEST2
TEST1
TEST0
XDATAO1
S256FS
SBCLK
SWCLK
DI256FS1
YWCLK+
YWCLK-
YDATA1+
YDATA1-
Fairlight ESP
Title
ESP-DIO DATA ROUTING
Size
B
Document Number
DATA.SCH
REV
4.0
Date:
June 5, 1998
Sheet
4 of 9
Rev 3.1 Changed U14 and U17 to TEST2


AES INPUT
AESIN0+
AESIN0-
SPDIF INPUT
SPIN0+
T3
PE65612
R9 120R
R1 75R
C5 10n
C8 10n
GND
RL1
FBR46ND005-P
Q1 BC549
VCC
D5 1N4148
R15 1K
R28 1K
C21 47n
U10
CS8411 (8000)
VA+
RXP
RXN
FILT
AGND
MCK
FSYNC
SCK
SDATA
ERF
INT
CS
R/W
A4/FCK
D0
D1
D2
D3
D4
D5
D6
D7
A0
A1
A2
A3
DI256FS0
DIWCLK0
DIBCLK0
DIDATA0
*IRQ
*DIGIN0
R/*W
A[0..15]
FDA4
D[0..7]
*AES0
AES INPUT
AESIN1+
AESIN1-
SPDIF INPUT
SPIN1+
T4
PE65612
R10 120R
R3 75R
C6 10n
C9 10n
RL2
FBR46ND005-P
Q2 BC549
D6 1N4148
R16 1K
R26 1K
C20 47n
U11
DI256FS1
DIWCLK1
DIBCLK1
DIDATA1
*DIGIN1
*AES1
REV 3.6 - removed R2,R4,R17,R18
Fairlight ESP
Title
ESP-DIO DIGITAL INPUT
Size
B
Document Number
DIGIN.SCH
REV
4.0
Date:
June 5, 1998
Sheet
5 of 9
*AES = 0
SELECT AES INPUT
*AES = 1
SELECT SPDIF INPUT
FDA4
FDEN = 0
NORMAL OPERATION
FDA4 = A4
FDEN = 1
ENABLE INPUT FREQUENCY DETECTION
FDA4 = 6.144 MHz


Fairlight ESP
Title
ESP-DIO DIGITAL OUTPUTS
Size B
Document Number DIGOUT.SCH
REV 4.0
Date: June 5, 1998 Sheet 6 of 9
AES
AESOUT0+
AESOUT0-
SPDIF
SPOUT0+
T2
PE65612
R8 120R
R23 360R
R24 91R
GND
U13C 74HC244
U15 CS8401 (9000)
MCK FSYNC SCK SDATA INT CS R/W TXP TXN A0 A1 A2 A3 A4 D0 D1 D2 D3 D4 D5 D6 D7
S256FS SWCLK SBCLK SDATAO0 *IRQ *DIGOUT0 R/*W A10..15 D10..71
AES
AESOUT1+
AESOUT1-
SPDIF
SPOUT1+
T1
PE65612
R7 120R
R21 360R
R22 91R
GND
U13D 74HC244
U21 CS8401 (9800)
S256FS SWCLK SBCLK SDATAO1 *IRQ *DIGOUT1 R/*W A10..15 D10..71
YAMAHA Y2
YWCLK+
YWCLK-
YDATA0+
YDATA0-
YDATA1+
YDATA1-
U9 3487
INA INB INC IND OUTA OUTB OUTC OUTD A/B EN C/D EN
GND VCC VCC
SWCLK SDATAO0 SDATAO1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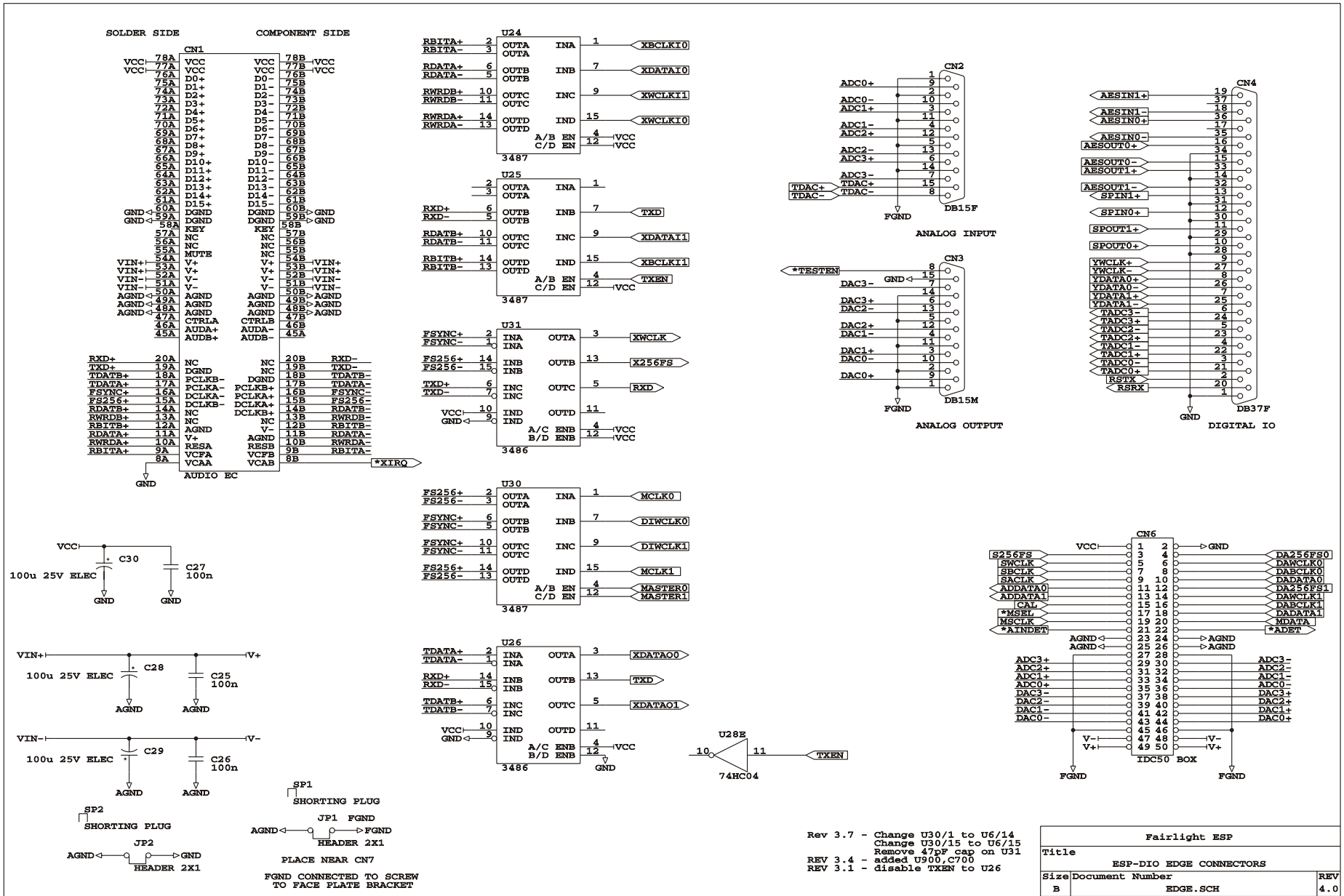
Title
ESP-DIO SELF TEST CIRCUITS
Size
B
Document Number
TEST.SCH
REV
4.0
Date:
June 5, 1998
Sheet
7 of 9
TDAC+
TDAC-
TADC0-
TADC0+
TADC1-
TADC1+
TADC2-
TADC2+
TADC3-
TADC3+
U2
SSM2142
U1A
TL082
U1B
TL082
U3C
U3B
U3A
U3D
TL084
C7
10p
R14
82K
R13
22K
R11
2K2
R12
2K2
RN4C 2K2-8
RN2C 22K-8
RN2D 22K-8
RN4D 2K2-8
RN4A 2K2-8
RN2A 22K-8
RN2B 22K-8
RN4B 2K2-8
RN3C 2K2-8
RN1C 22K-8
RN1D 22K-8
RN3D 2K2-8
RN3A 2K2-8
RN1A 22K-8
RN1B 22K-8
RN3B 2K2-8
RN5D 2K2-8
RN5C 2K2-8
RN6D 2K2-8
RN6C 2K2-8
RN6A 2K2-8
RN6B 2K2-8
RN5A 2K2-8
RN5B 2K2-8
D2 1N4148
D4 1N4148
D10 1N4148
D8 1N4148
D9 1N4148
D7 1N4148
D1 1N4148
D3 1N4148
U5
74HC4351
RN7B 1K-8
RN7A 1K-8
RN7C 1K-8
RN7D 1K-8
VSEL2
VSEL1
VSEL0
SADC0
SADC1
SADC2
SADC3
VCC
GND
AGND
V+
V-


SOLDER SIDE
COMPONENT SIDE
CN1
AUDIO EC
U24
U25
U31
U30
U26
U28E
74HC04
3487
3486
CN2
DB15F
ANALOG INPUT
CN3
DB15M
ANALOG OUTPUT
CN4
DB37F
DIGITAL IO
CN6
IDC50 BOX
C30
C27
C28
C25
C29
C26
SP1
SHORTING PLUG
SP2
SHORTING PLUG
JP1
HEADER 2X1
JP2
HEADER 2X1
PLACE NEAR CN7
FGND CONNECTED TO SCREW
TO FACE PLATE BRACKET
Rev 3.7 - Change U30/1 to U6/14
Change U30/15 to U6/15
Remove 47pF cap on U31
REV 3.4 - added U900,C700
REV 3.1 - disable TXEN to U26
Fairlight ESP
Title
ESP-DIO EDGE CONNECTORS
Size B
Document Number EDGE.SCH
REV 4.0
Date: June 5, 1998
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Fairlight ESP
Title
ESP-DIO EXTRAS
Size
B
Document Number
EXTRAS.SCH
REV
4.0
Date: June 5, 1998
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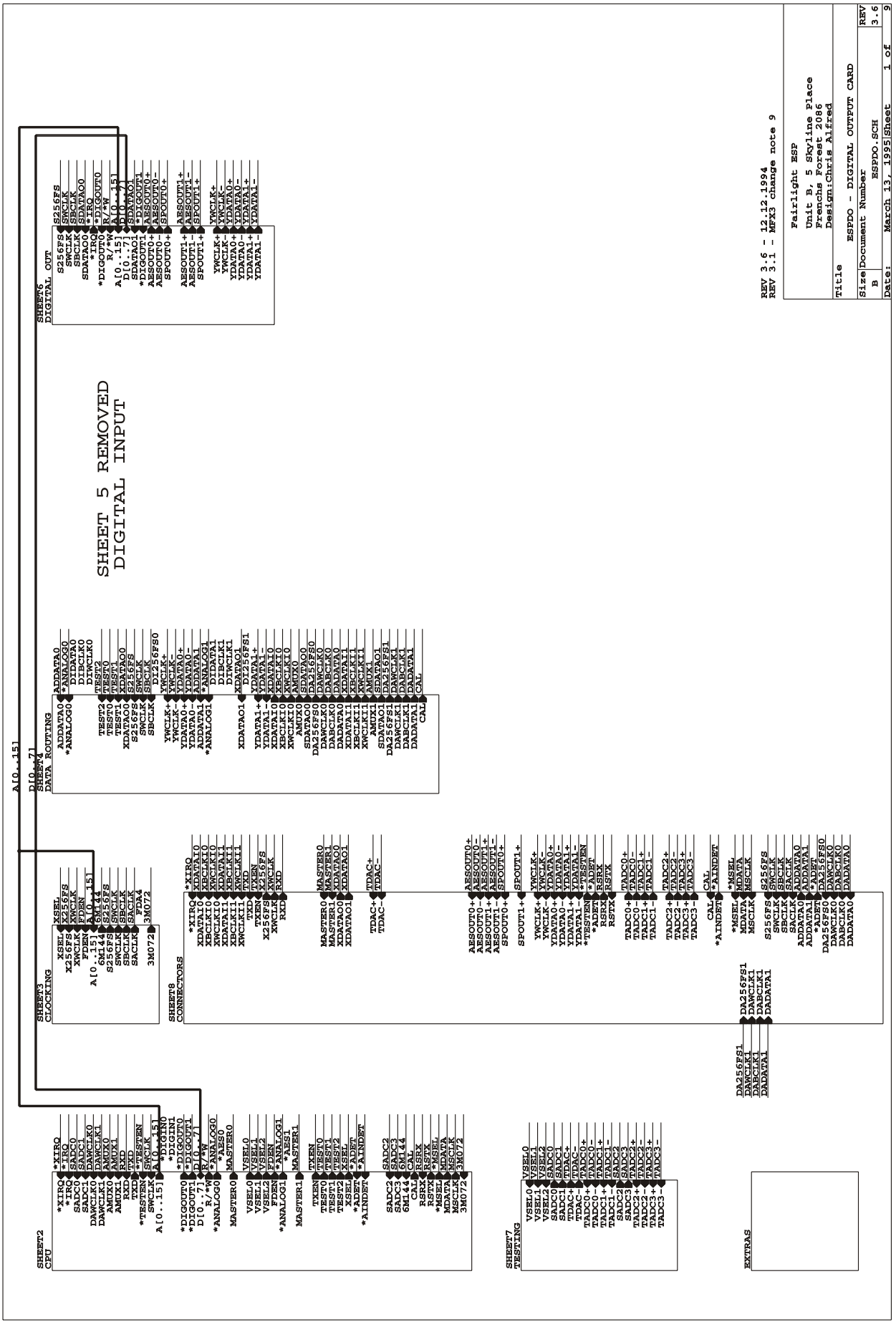
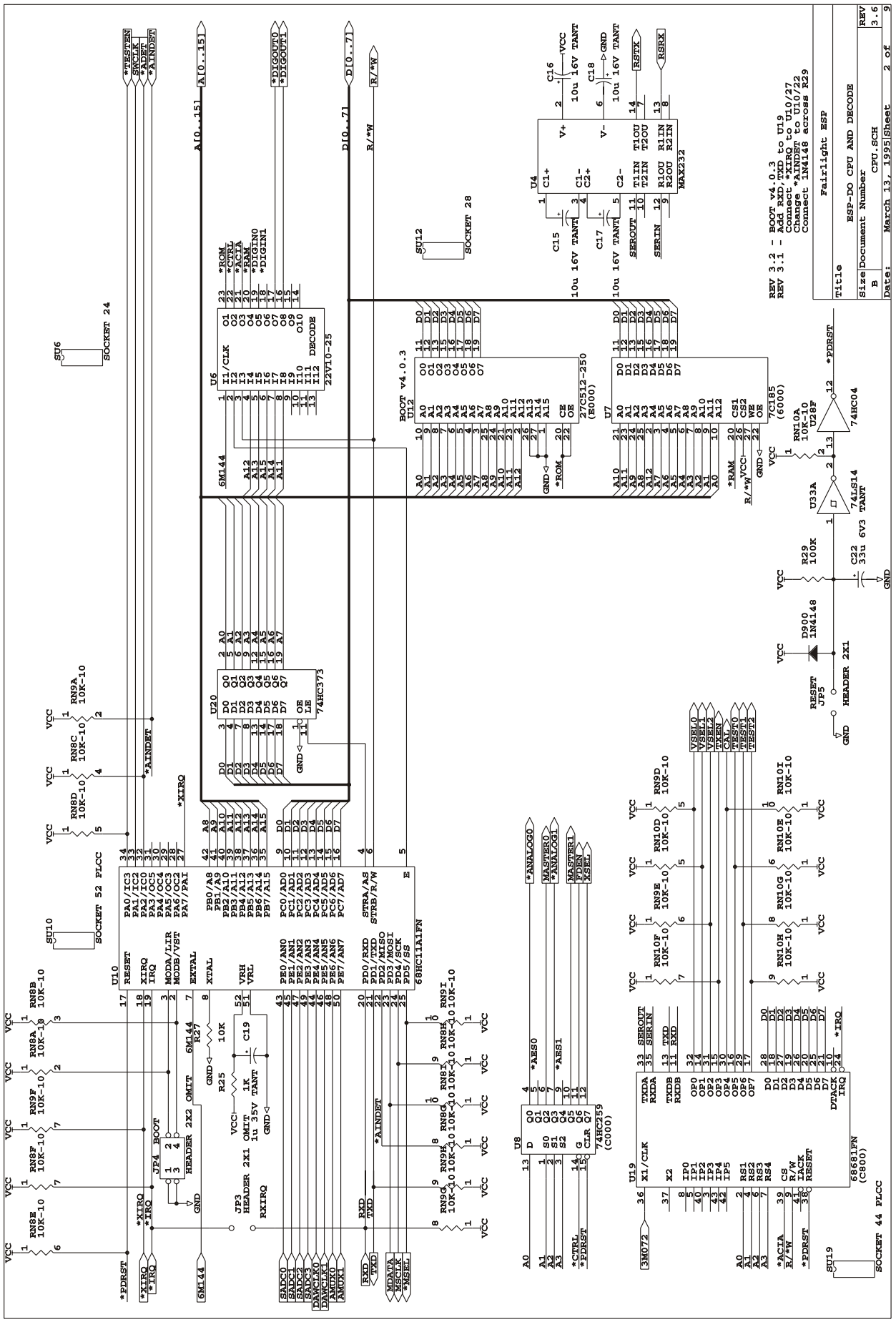
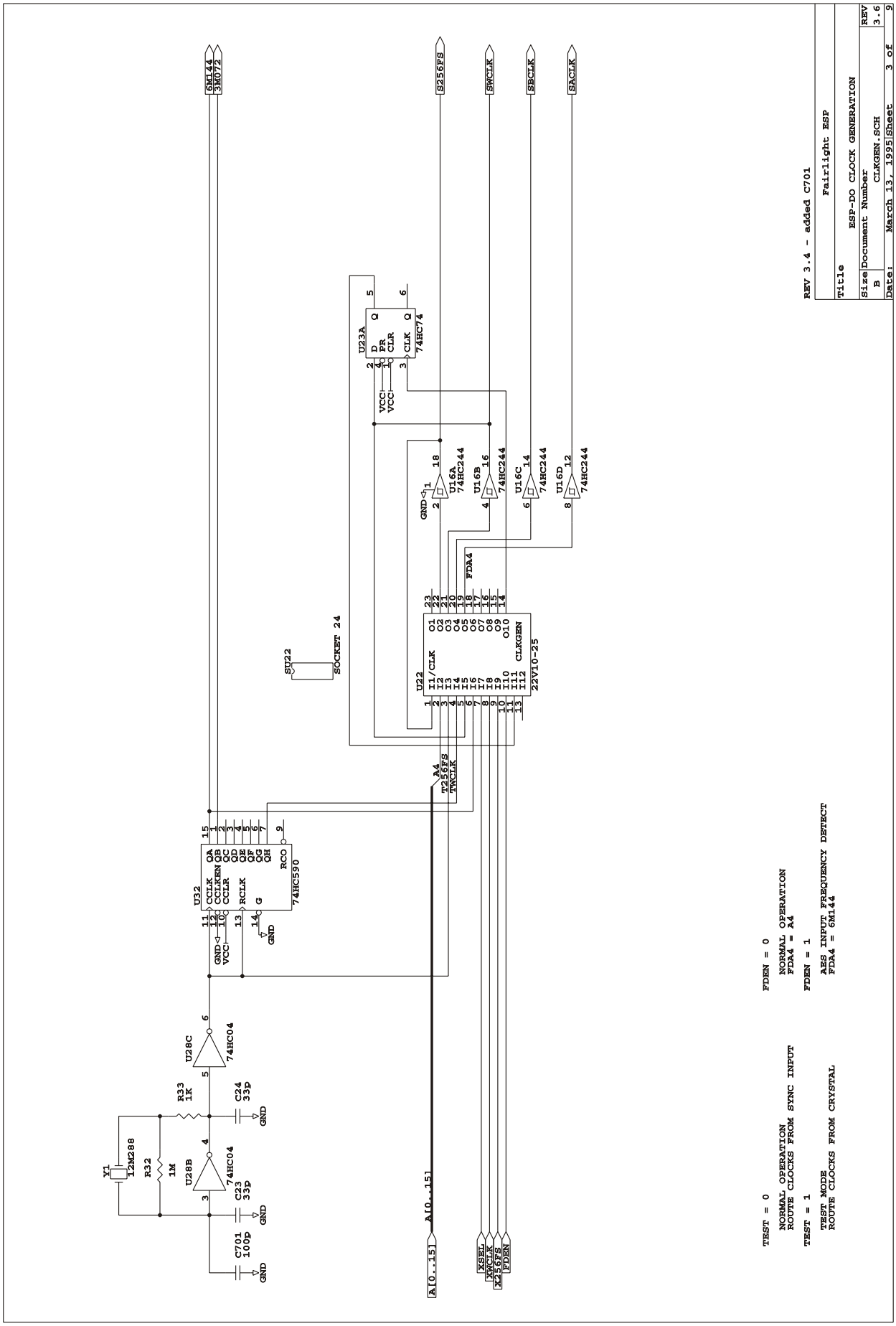
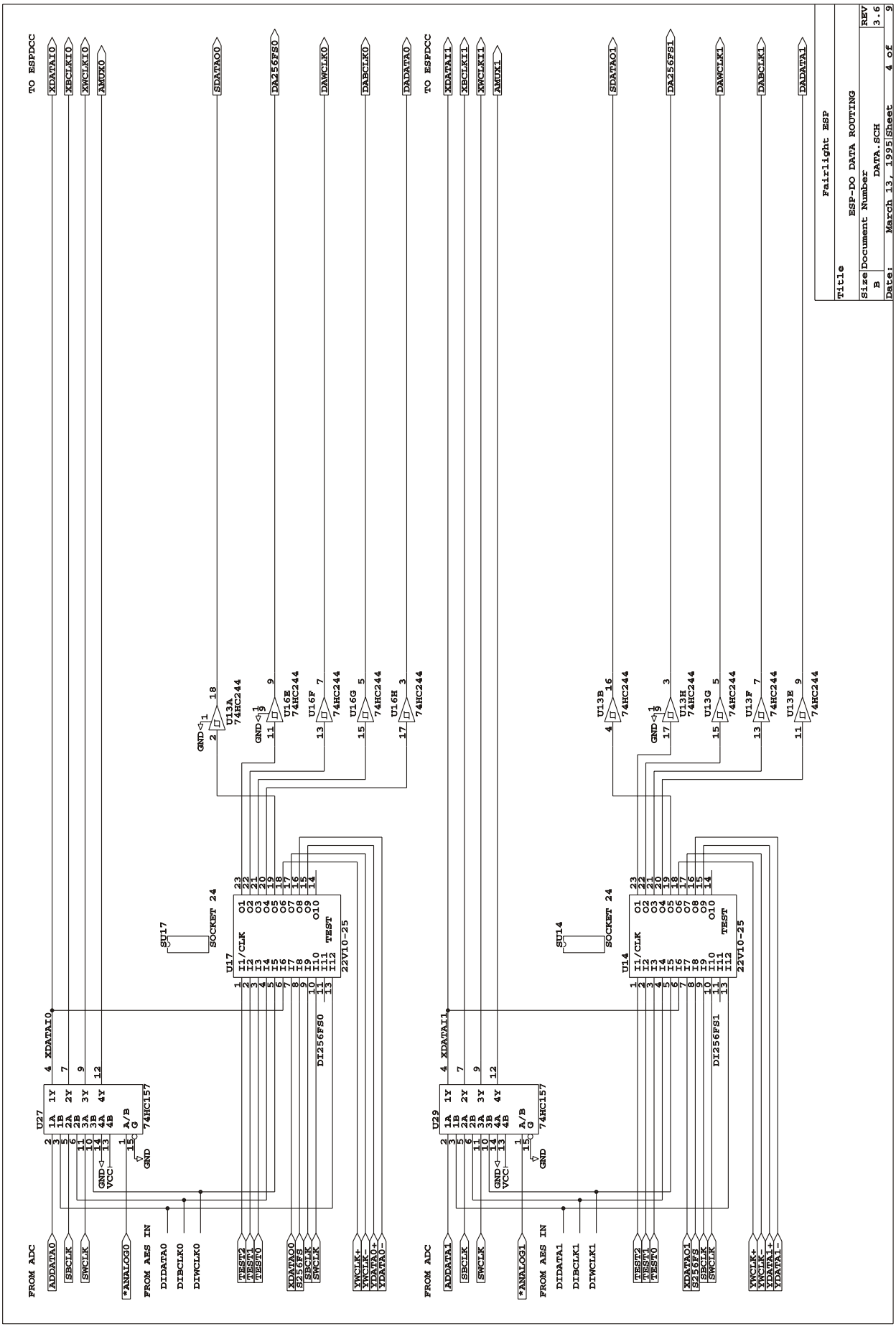
PCB1
PCB
PCB2
GND PLANE
H1
LCBSM-6-01
H2
LCBSM-6-01
H3
LCBSM-6-01
H4
LCBSM-6-01
H5
M3x8
H6
M3x8
H7
M3x8
H8
M3x8
H9
M3 FIBRE
H10
M3 FIBRE
H11
M3 FIBRE
H12
M3 FIBRE
H13
M3 FIBRE
H14
M3 FIBRE
C901 100n
C902 100n
C903 100n
C904 100n
C905 100n
C906 100n
C907 100n
C908 100n
C909 100n
C910 100n
C911 100n
C912 100n
C913 100n
C914 100n
C915 100n
C916 100n
C917 100n
C918 100n
C919 100n
C920 100n
C921 100n
C922 100n
VCC
GND

15.5 ESPDO SCHEMATICS

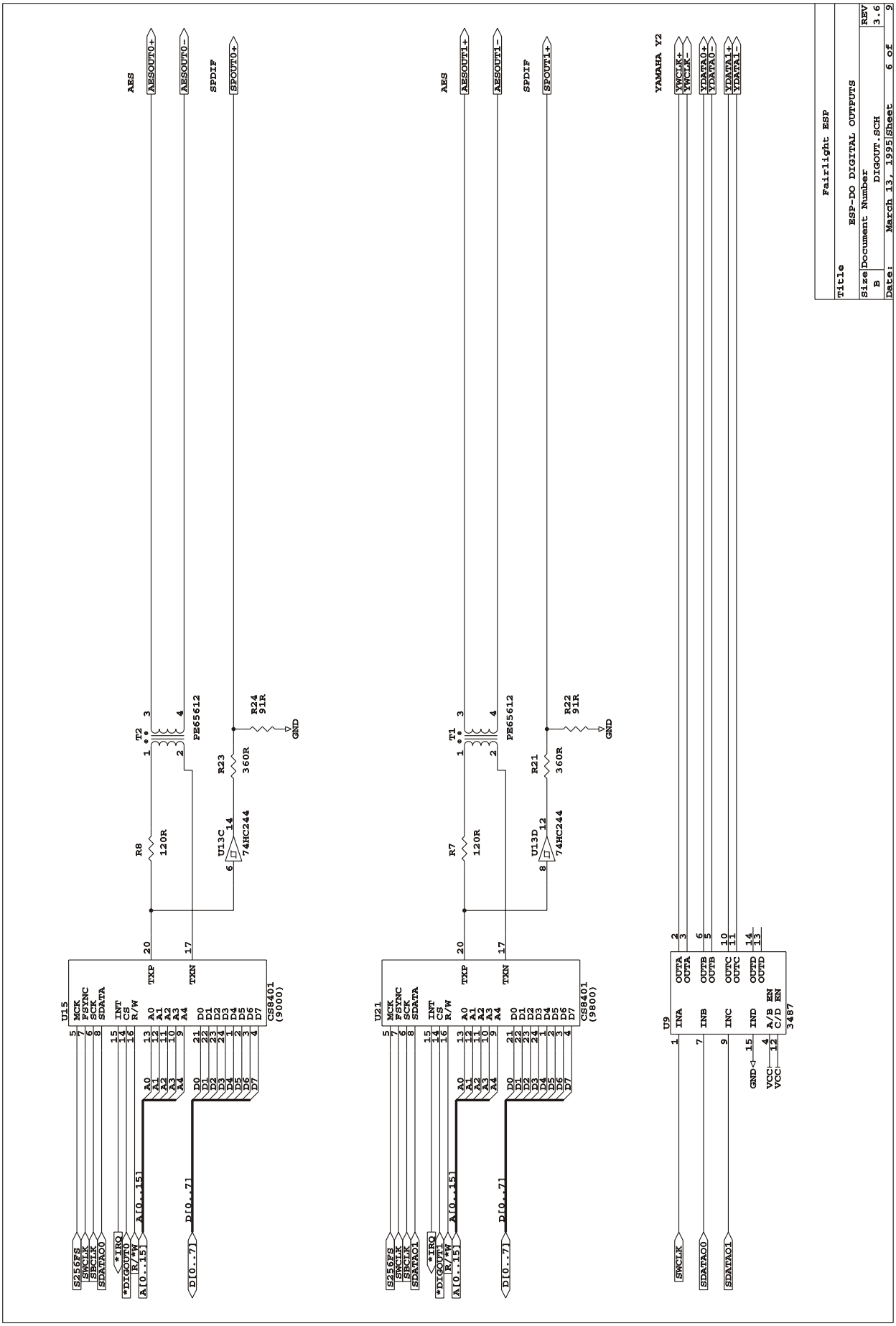


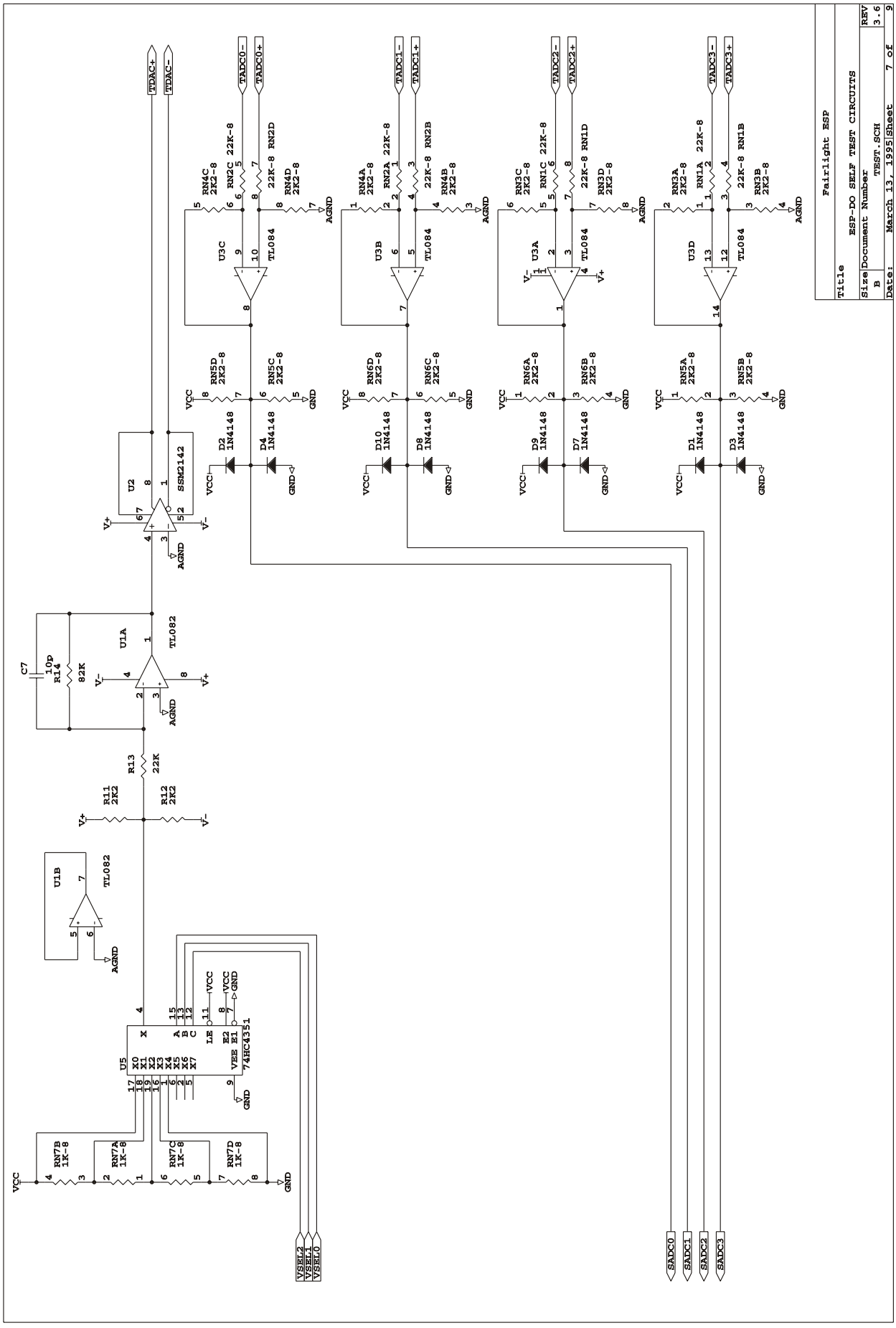

Fairlight ESP
Title
ESP-DO CPU AND DECODE
Size B
Document Number
CPU.SCH
REV
Date: March 13, 1995
Sheet 2 of 9
REV 3.2 - BOOT v4.0.3
REV 3.1 - Add RXD, TXD to U19
Connect *XIRQ to U10/27
Change *AINDET to U10/22
Connect 1N4148 across R29
SOCKET 52 PLCC
SOCKET 44 PLCC
SOCKET 24
SOCKET 28
BOOT v4.0.3
27C512-250 (E000)
74HC373
74HC259 (C000)
74HC04
74LS14
MAX232
68681FN (C800)
68HC11A1FN
22V10-25
7C185 (6000)
HEADER 2X1
HEADER 2X2
A[0..15]
D[0..7]
*XIRQ
*AINDET
*PDRST
*ROM
*CTRL
*ACIA
*RAM
*DIGIN0
*DIGIN1
*DIGOUT0
*DIGOUT1
*TESTEN
SWCLK
*ADET
*AINDET
R/*W
*RAM
*ROM
*PDRST
RSTX
RSRX
RSTK
VCC
GND

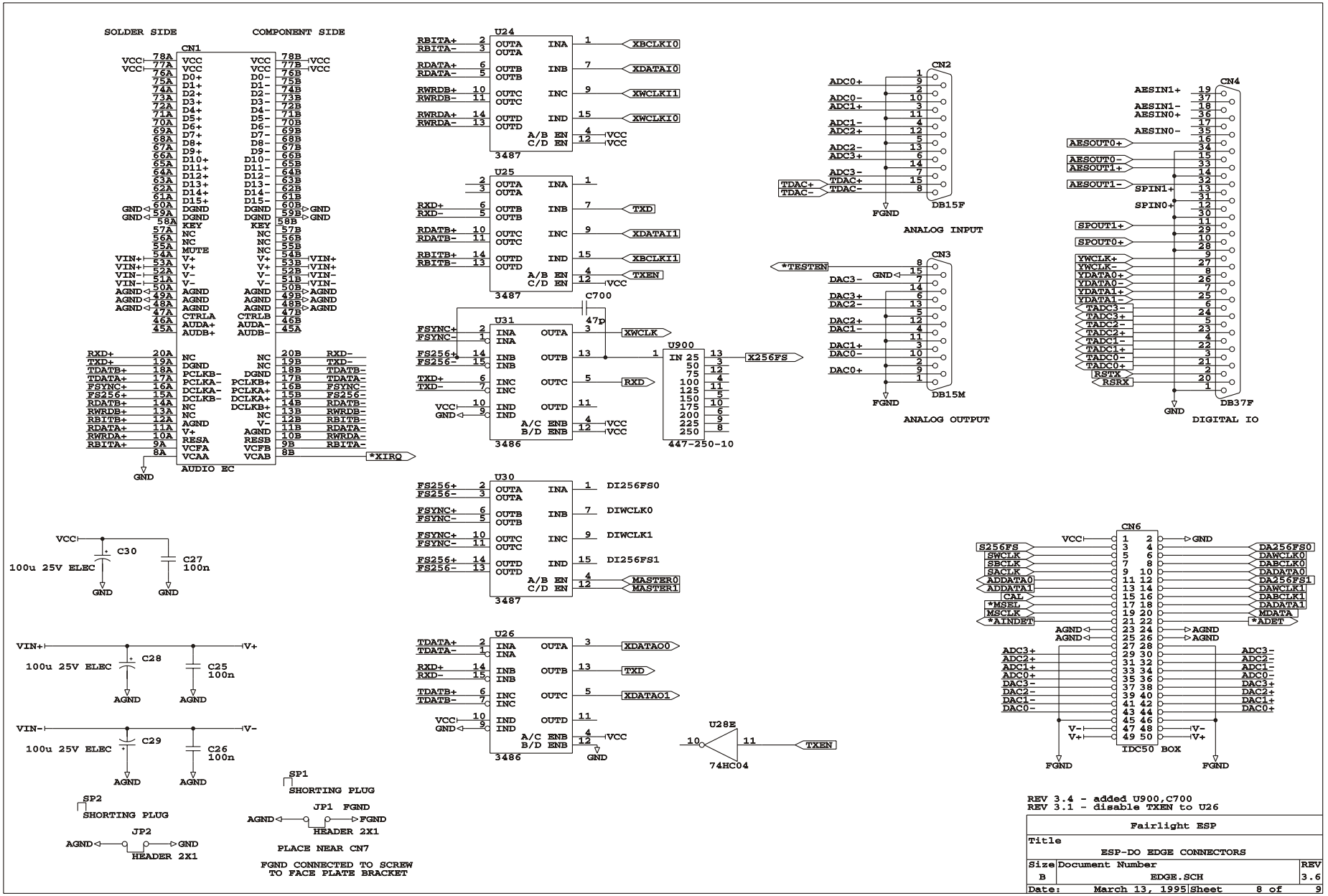

6M144
3M072
S256FS
SWCLK
SBCLK
SACLK
U23A
74HC74
U16A
74HC244
U16B
74HC244
U16C
74HC244
U16D
74HC244
SU22
SOCKET 24
U22
22V10-25
CLKGEN
FDA4
A4
TS256FS
TSWCLK
U32
74HC590
U28C
74HC04
U28B
74HC04
R33
1K
R32
1M
C24
33p
C23
33p
C701
100p
Y1
12M288
GND
VCC
A[0..15]
XSEL
XWCLK
X256FS
FDEN
REV 3.4 - added C701
Fairlight ESP
ESP-DO CLOCK GENERATION
Document Number
CLKGEN.SCH
March 13, 1995
Sheet 3 of 9
REV 3.6
TEST = 0
NORMAL OPERATION
ROUTE CLOCKS FROM SYNC INPUT
TEST = 1
TEST MODE
ROUTE CLOCKS FROM CRYSTAL
FDEN = 0
NORMAL OPERATION
FDA4 = A4
FDEN = 1
AES INPUT FREQUENCY DETECT
FDA4 = 6M144

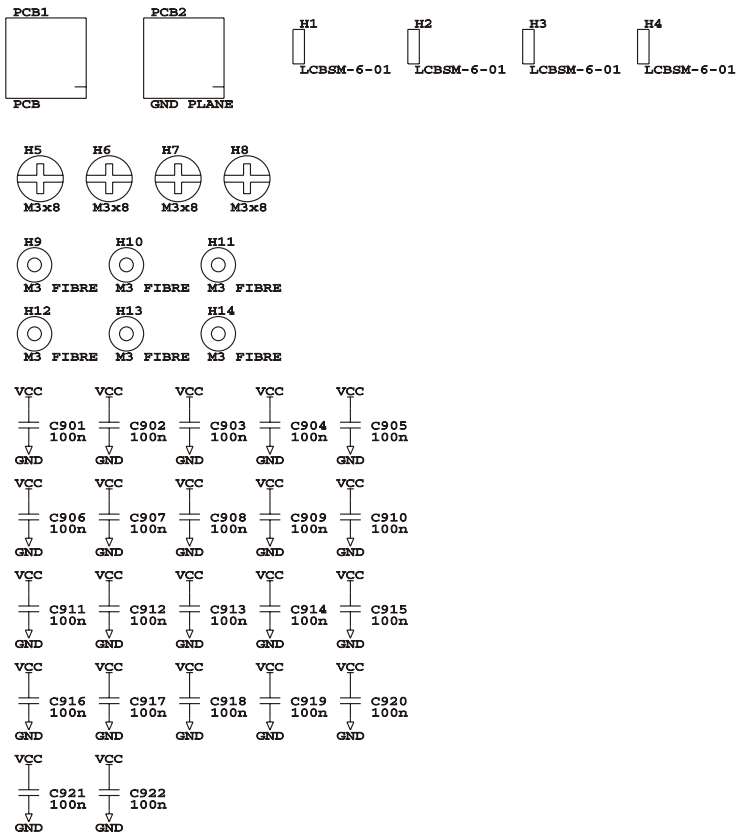

TO ESPDCC
XDATAI0
XBCLKI0
XWCLKI0
AMUXO
SDATAO0
DA256FS0
DAWCLK0
DABCLK0
DADATA0
TO ESPDCC
XDATAI1
XBCLKI1
XWCLKI1
AMUX1
SDATAO1
DA256FS1
DAWCLK1
DABCLK1
DADATA1
Fairlight ESP
Title
ESP-DO DATA ROUTING
Size
B
Document Number
DATA.SCH
REV
3.6
Date: March 13, 1995
Sheet 4 of 9
FROM ADC
ADDATA0
SBCLK
SWCLK
*ANALOG0
FROM AES IN
DIDATA0
DIBCLK0
DIWCLK0
U27
74HC157
SU17
SOCKET 24
U17
22V10-25
TEST
DI256FS0
XDATAO0
A256FS
SBCLK
SWCLK
YWCLK+
YWCLK-
YDATA0+
YDATA0-
U13A
74HC244
U16E
74HC244
U16F
74HC244
U16G
74HC244
U16H
74HC244
FROM ADC
ADDATA1
SBCLK
SWCLK
*ANALOG1
FROM AES IN
DIDATA1
DIBCLK1
DIWCLK1
U29
74HC157
SU14
SOCKET 24
U14
22V10-25
TEST
DI256FS1
XDATAO1
A256FS
SBCLK
SWCLK
YWCLK+
YWCLK-
YDATA1+
YDATA1-
U13B
74HC244
U13H
74HC244
U13G
74HC244
U13F
74HC244
U13E
74HC244

Sheet 5 Removed


Fairlight ESP
Title
ESP-DO DIGITAL OUTPUTS
Size
B
Document Number
DIGOUT.SCH
REV
3.6
Date:
March 13, 1995
Sheet
6 of
9
AES
AESOUT0+
AESOUT0-
SPDIF
SPOUT0+
AESOUT1+
AESOUT1-
SPOUT1+
YAMAHA Y2
YWCLK+
YWCLK-
YDATA0+
YDATA0-
YDATA1+
YDATA1-
T2
T1
PE65612
R8
R7
120R
R23
R21
360R
R24
R22
91R
GND
U13C
U13D
74HC244
U15
U21
CS8401
(9000)
(9800)
MCK
FSYNC
SCK
SDATA
INT
CS
R/W
A0
A1
A2
A3
A4
D0
D1
D2
D3
D4
D5
D6
D7
TXP
TXN
A[0..15]
D[0..7]
S256FS
SWCLK
SBCLK
SDATA0
SDATA1
*IRQ
*DIGOUT0
*DIGOUT1
R/*W
U9
INA
INB
INC
IND
OUTA
OUTB
OUTC
OUTD
A/B
C/D
EN
GND
VCC
3487

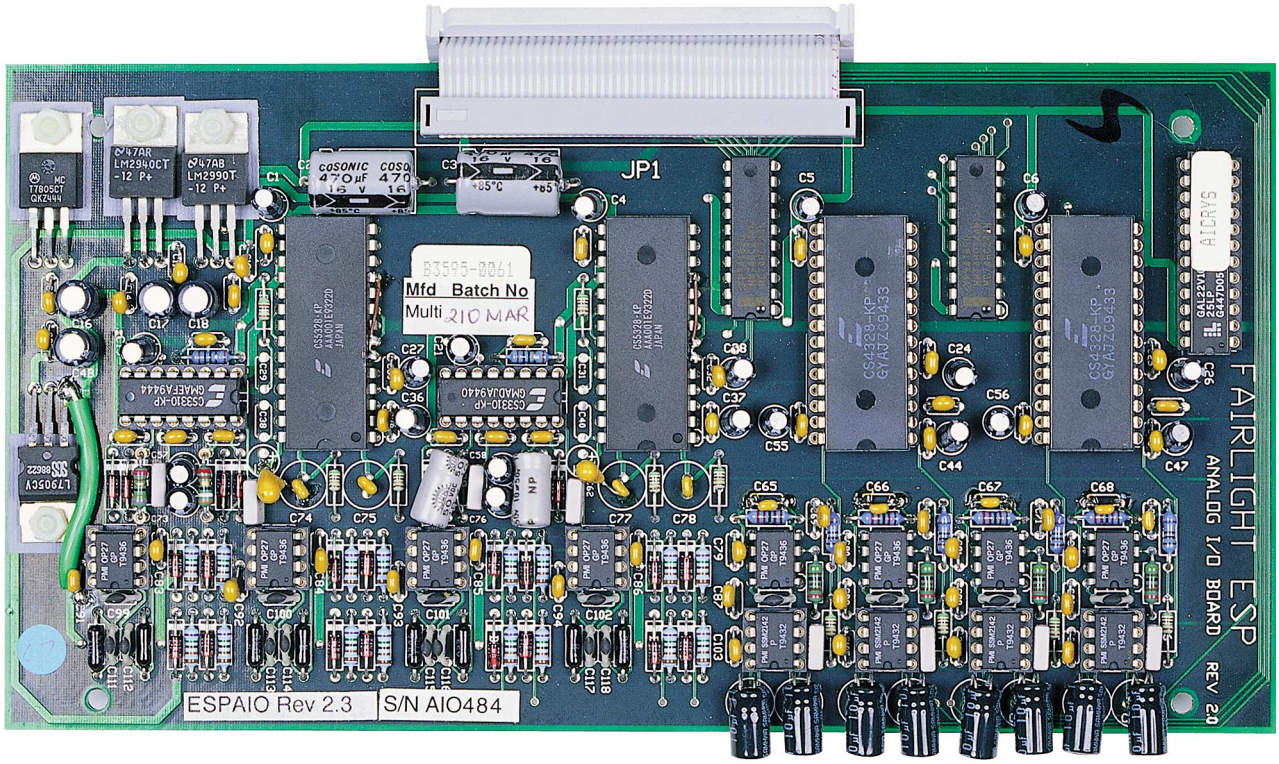

Fairlight ESP
Title
ESP-DO SELF TEST CIRCUITS
Size B
Document Number
TEST.SCH
REV 3.6
Date: March 13, 1995
Sheet 7 of 9
TDAC+
TDAC-
TADC0-
TADC0+
TADC1-
TADC1+
TADC2-
TADC2+
TADC3-
TADC3+
U2
SSM2142
U1A
TL082
U1B
TL082
U3C
U3B
U3A
U3D
TL084
U5
74HC4351
C7
10p
R14
82K
R13
22K
R11
2K2
R12
2K2
RN4C 2K2-8
RN2C 22K-8
RN4D 2K2-8
RN4A 2K2-8
RN2A 22K-8
RN4B 2K2-8
RN3C 2K2-8
RN1C 22K-8
RN3D 2K2-8
RN3A 2K2-8
RN1A 22K-8
RN3B 2K2-8
RN5D 2K2-8
RN5C 2K2-8
RN6D 2K2-8
RN6C 2K2-8
RN6A 2K2-8
RN6B 2K2-8
RN5A 2K2-8
RN5B 2K2-8
RN7B 1K-8
RN7A 1K-8
RN7C 1K-8
RN7D 1K-8
D2 1N4148
D4 1N4148
D10 1N4148
D8 1N4148
D9 1N4148
D7 1N4148
D1 1N4148
D3 1N4148
VCC
GND
AGND
V+
V-
VSEL2
VSEL1
VSEL0
SADC0
SADC1
SADC2
SADC3


SOLDER SIDE
COMPONENT SIDE
CN1
AUDIO EC
U24
U25
U31
U30
U26
U900
X256FS
447-250-10
C700
47p
XWCLK
XBCLKI0
XDATAI0
XWCLKI1
XWCLKI0
TXD
XDATAI1
XBCLKI1
TXEN
RXD
MASTER0
MASTER1
DI256FS0
DIWCLK0
DIWCLK1
DI256FS1
XDATAO0
XDATAO1
3487
3486
CN2
DB15F
ANALOG INPUT
CN3
DB15M
ANALOG OUTPUT
CN4
DB37F
DIGITAL IO
CN6
IDC50 BOX
U28E
74HC04
C30
100u 25V ELEC
C27
100n
C28
C25
C29
C26
SP1
SHORTING PLUG
SP2
SHORTING PLUG
JP1 FGND
HEADER 2X1
JP2
HEADER 2X1
PLACE NEAR CN7
FGND CONNECTED TO SCREW
TO FACE PLATE BRACKET
REV 3.4 - added U900,C700
REV 3.1 - disable TXEN to U26
Fairlight ESP
Title
ESP-DO EDGE CONNECTORS
Size B
Document Number EDGE.SCH
REV 3.6
Date: March 13, 1995 Sheet 8 of 9

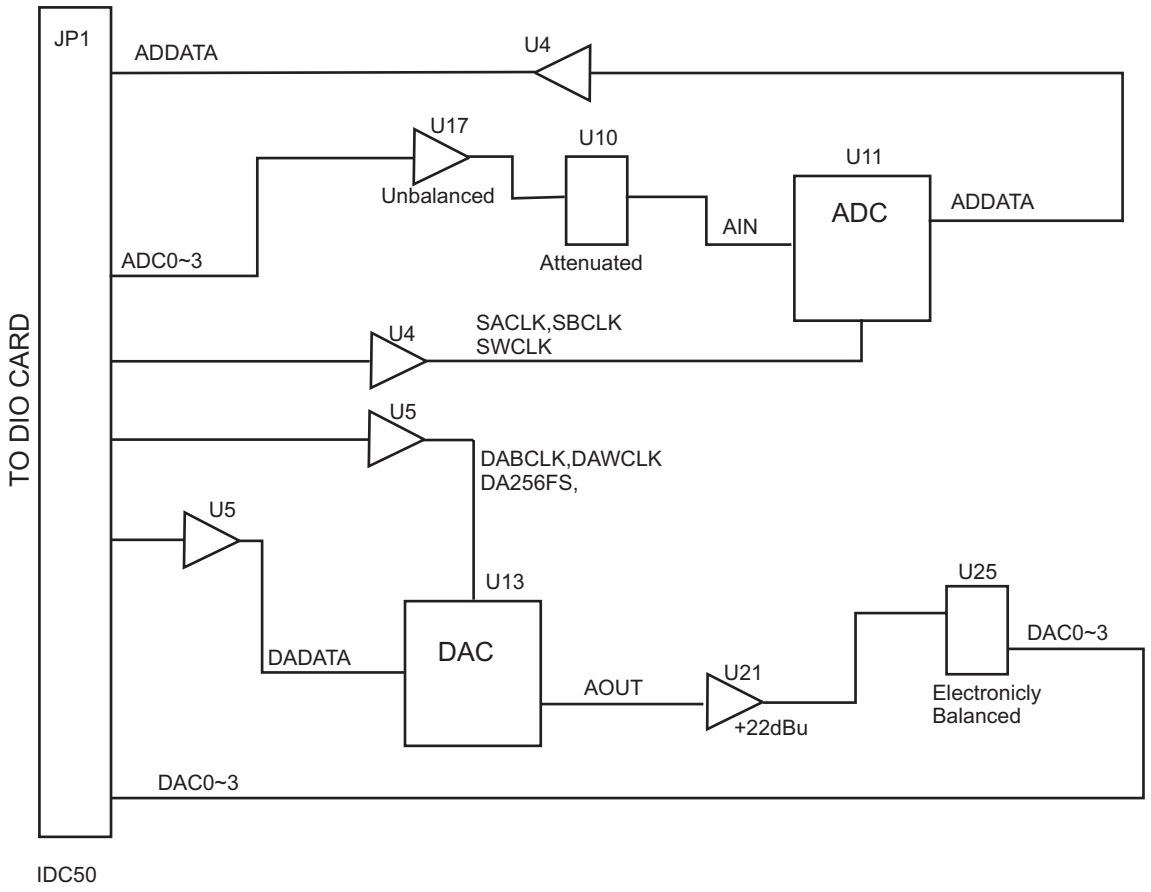


Fairlight ESP		
Title: ESP-DO EXTRAS		
Size: B	Document Number: EXTRAS.SCH	REV: 3.6
Date: March 13, 1995	Sheet 9 of 9	

16.0 ESPAIO Analog I/O Card



16.1 ESPAIO Block Diagram



16.2 ESPAIO Circuit Description

16.2.1. Introduction

The AIO card provides 4 channels of analog input and 4 channels of analog output. Each input channel has digitally controlled attenuators allowing gain to +30dB and attenuation to -96dB and mute.

The peak levels allowed on the card are +22dBu based on +4dBu nominal level and 18dB headroom.

16.2.2. Power Supply

The +/-15V analog supply from the Analog Mother Board is regulated to +/-12V by U1 and U2 for driving the input and output stage op-amps. The +/-12V supply is further regulated to +/-5V to supply the other analog devices.

16.2.3. Anlog Input stage

As each input channel in identical, channel 0 will be used as an example.

The balanced input (ADC0+, ADC0-)is unbalanced by U17 (AD797 or OP27) and attenuated by 14.3dB (+22dBu peak input attenuated to +7.7dBu). This signal is then fed into U10 (CS3310) digitally controlled attenuator and finally filtered by R10 (51R) and C64 (10nF) to become AIN0. Diodes D7,D8 (1N4148) protect the inputs of the A/D converter.

The CS3310 digital attenuators are controlled by serial lines driven by the 68HC11 CPU on the DIO. *MSEL is asserted when the CPU writes to the chips, and the MSCLK and MSDATA are to clock and serial data respectively. MDATA is received by U10 which takes is data and feeds extra data out MSDATA0 which is passed to U10. This allows one serial data stram to control both attenuators.

16.2.4. A/D Conversion

CS5328 18bit stereo 64 times oversampling delta-sigma converters are used for input conversion. The output of these converters is in three wire serial format where SWCLK is the sample rate word clock (high = LEFT sample, low = RIGHT sample), SBCLK is the 64Fs bit clock, and ADDATA0..1 is the serial audio data. SACLK is a 256Fs clock synchronous to SWCLK used to internally clock the A/D conversion process.

The LCAL signal is used to recalibrate the inputs to the chip to remove DC offsets and reset the chip. This signal is asserted by the DIO CPU upon power-on and whenever the samplerate or sync source changes in the disk recorder. LCAL is synchronised to SWCLK by U6 (CRYSTAL pal) as required by the A/D converters.

16.2.5. D/A Conversion

CS4328 18bit stereo 16 times oversampling delta-sigma converters are used for output conversion. The input to these converters is in three wire format where DAWCLK0..1 is the sample rate word clock, DABCLK0..1 is the 64 Fs bit clock, and DADATA0..1 is the serial output data. DA256FS0..1 is used to clock the internal conversion process.

16.2.6. Analog Output Stage

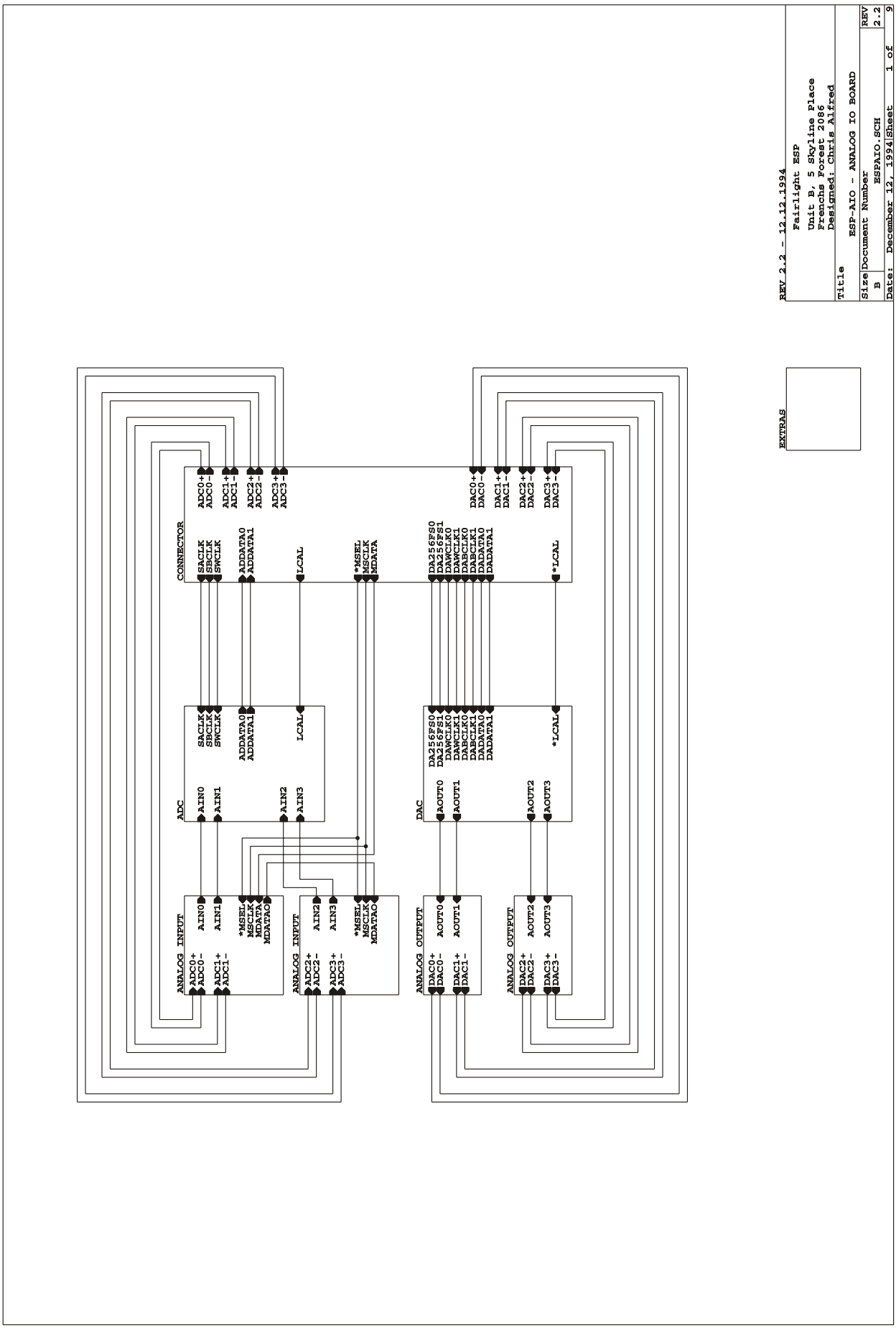
As all output channels are identical, channel 0 will be used as an example.

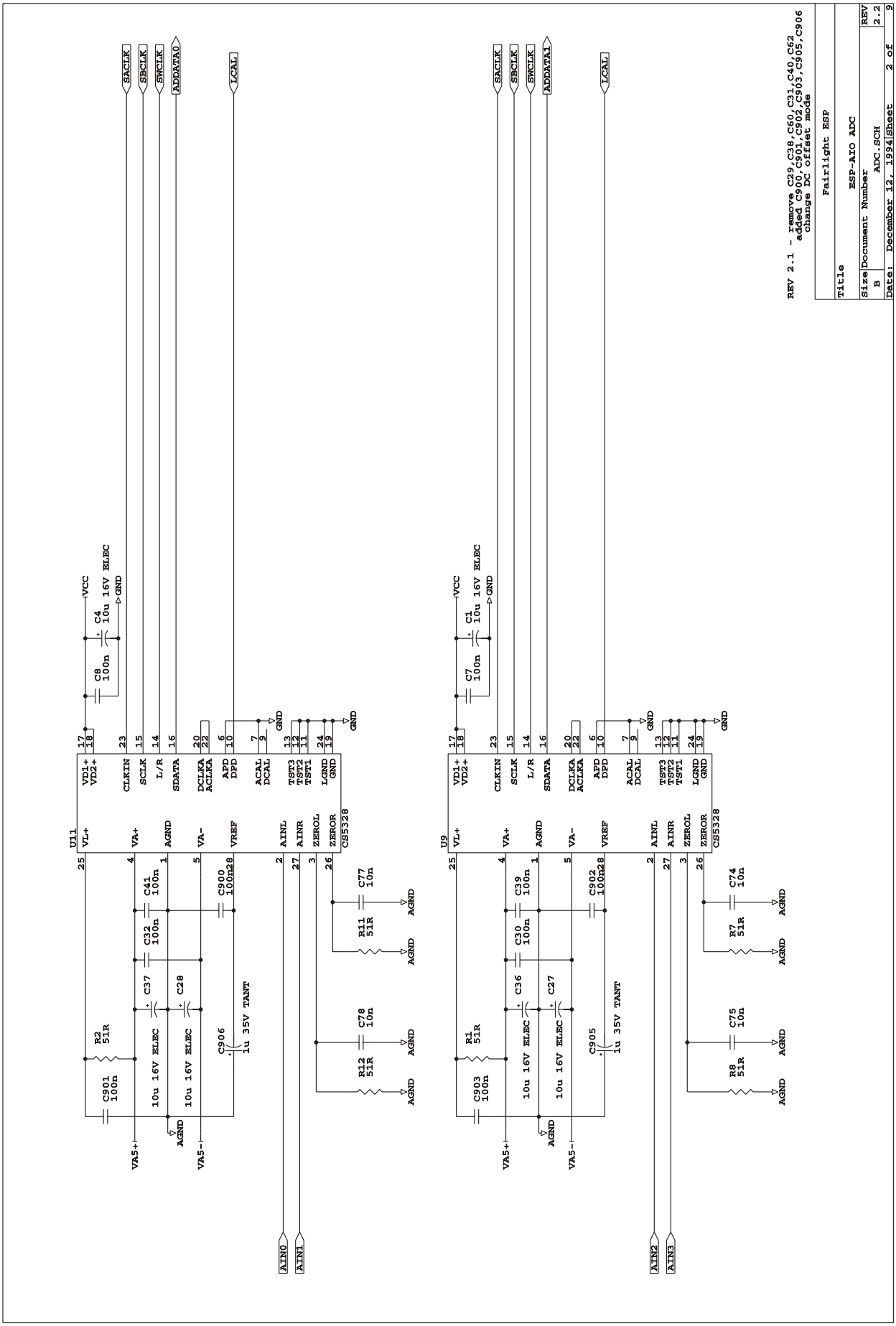
The analog output from the D/A converter AOUT0 is gained by U21 (AD797 or OP27) for a peak output of +22dBu. U25 (SSM2142) electronically balances the output. If one side of the output is shorted to GND, the other side will gain by +6dB to compensate. The bipolar capacitors protect the output against large DC offsets (e.g. phantom power).

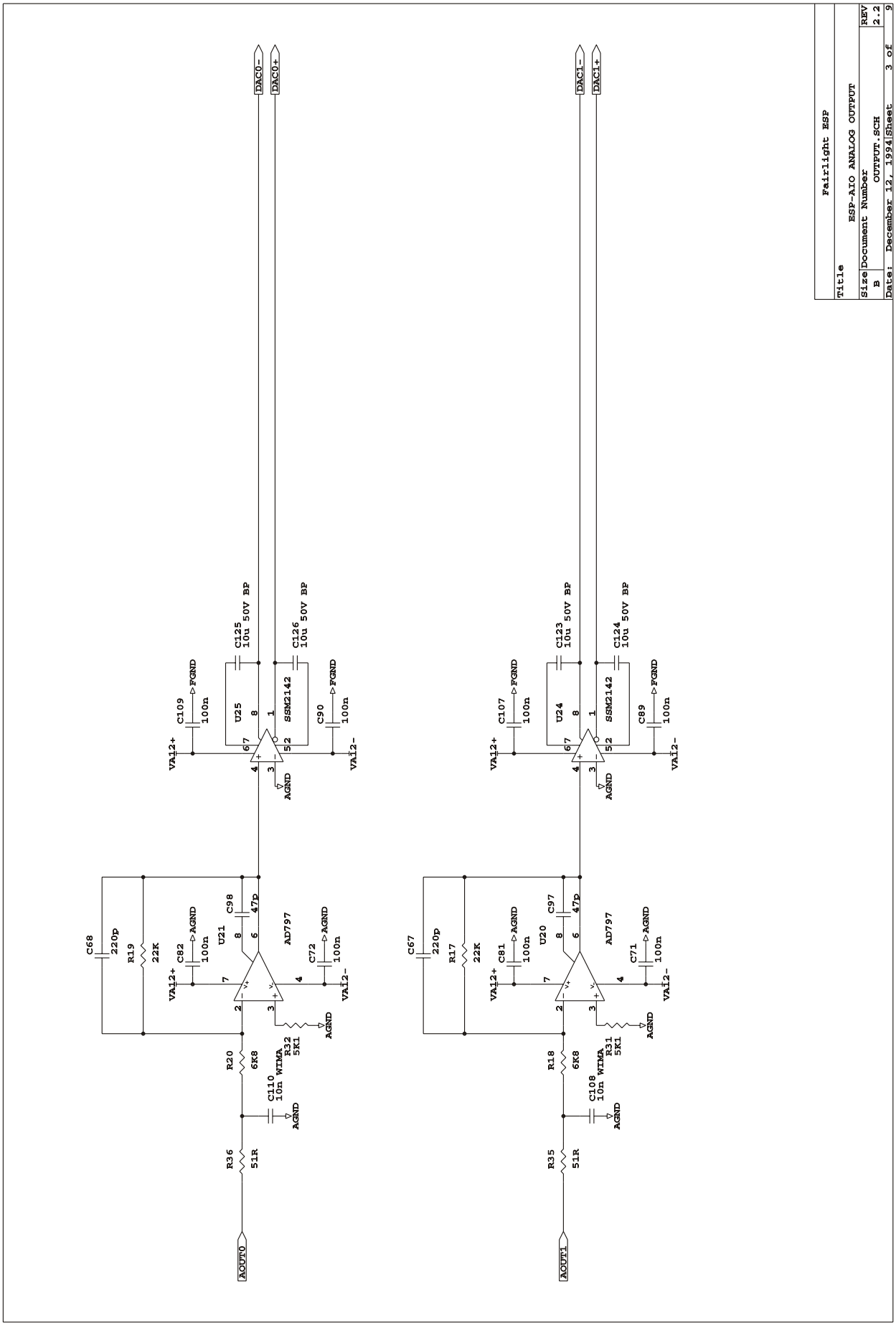
16.2.7. Testing information

If pins 8 and 15 of CN3 on the DIO are shorted, then the analog input is routed to the analog output with the digital attenuator set to 0dB gain.

16.3 ESPAIO SCHEMATICS




REV 2.1 - remove C29,C38,C60,C31,C40,C62
added C900,C901,C902,C903,C905,C906
change DC offset mode
Fairlight ESP
Title
ESP-AIO ADC
Size
B
Document Number
ADC.SCH
REV
2.2
Date: December 12, 1994
Sheet
2 of
9
U11
CS5328
U9
CS5328
SACLK
SBCLK
SWCLK
ADDATA0
ADDATA1
LCAL
VCC
GND
AGND
VA5+
VA5-
AIN0
AIN1
AIN2
AIN3
C8 100n
C4 10u 16V ELEC
C7 100n
C1 10u 16V ELEC
C901 100n
C41 100n
C32 100n
C37 10u 16V ELEC
C28 10u 16V ELEC
C906 1u 35V TANT
C900 100n28
C903 100n
C39 100n
C30 100n
C36 10u 16V ELEC
C27 10u 16V ELEC
C905 1u 35V TANT
C902 100n28
R2 51R
R11 51R
R12 51R
C77 10n
C78 10n
R1 51R
R7 51R
R8 51R
C74 10n
C75 10n
VD1+
VD2+
VL+
VA+
VA-
AGND
VREF
CLKIN
SCLK
L/R
SDATA
DCLKA
ACLKA
APD
DPD
ACAL
DCAL
TSP3
TSP2
TSP1
LGND
GND
AINL
AINR
ZEROL
ZEROR


Fairlight ESP
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ESP-AIO ANALOG OUTPUT
Size
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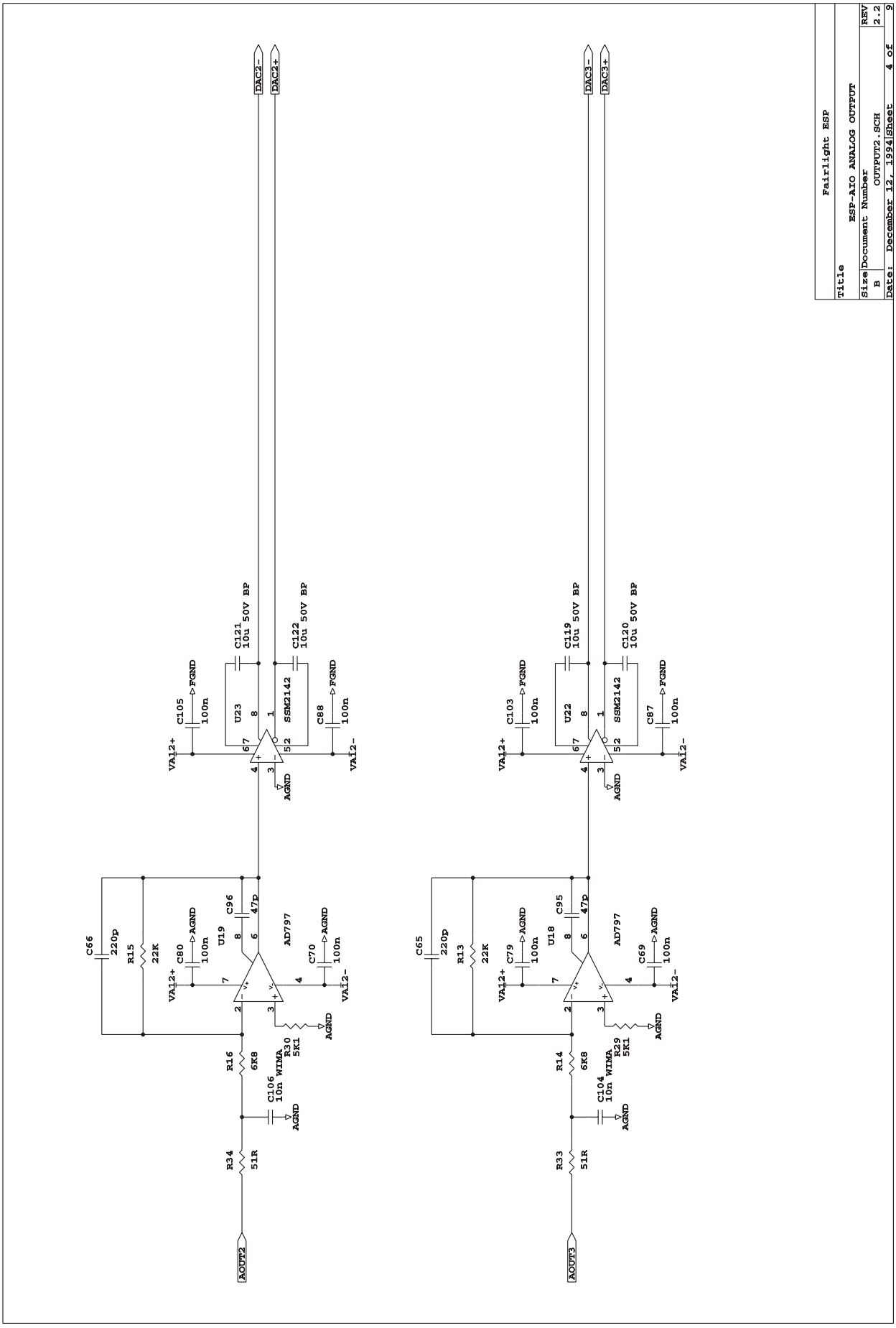
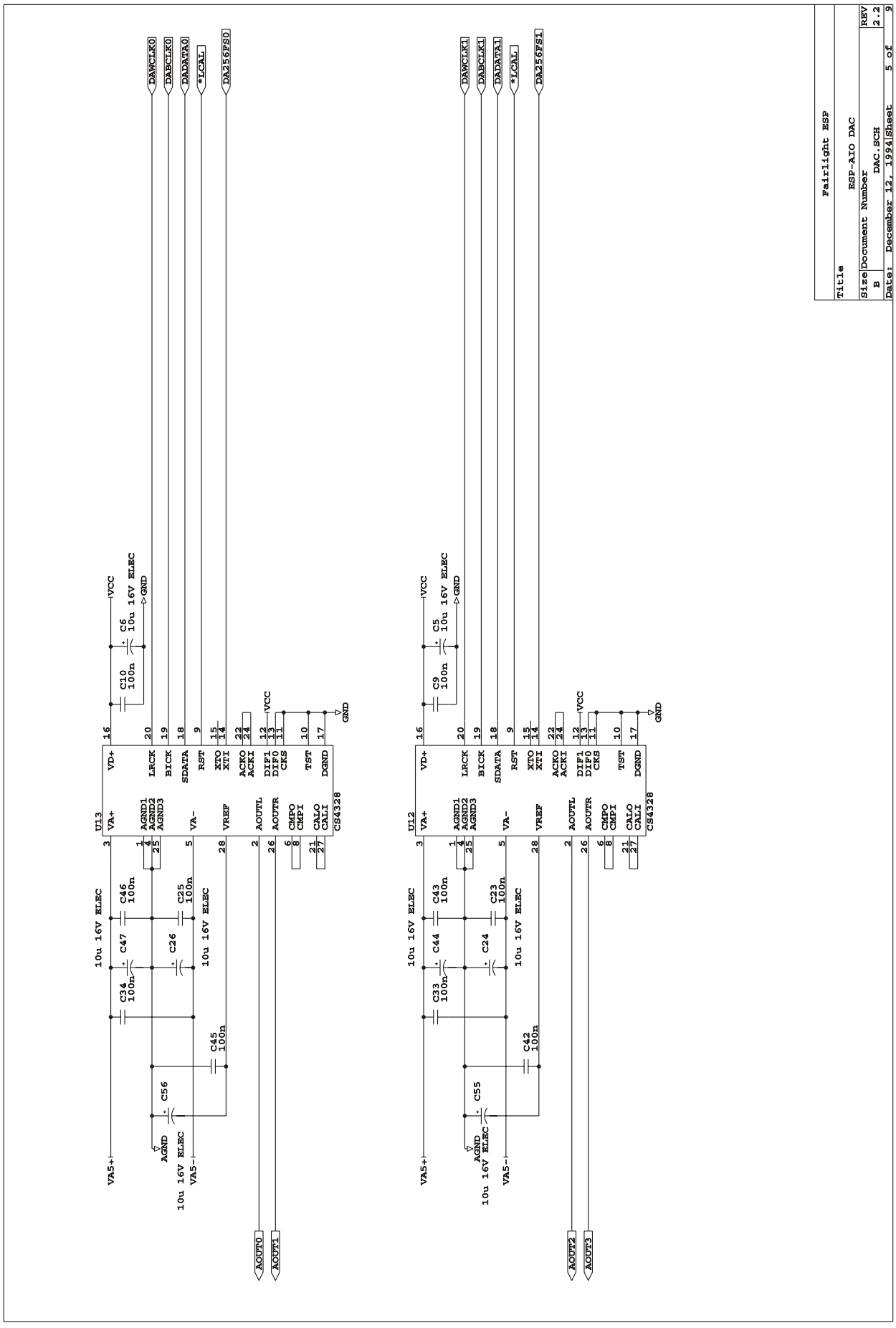
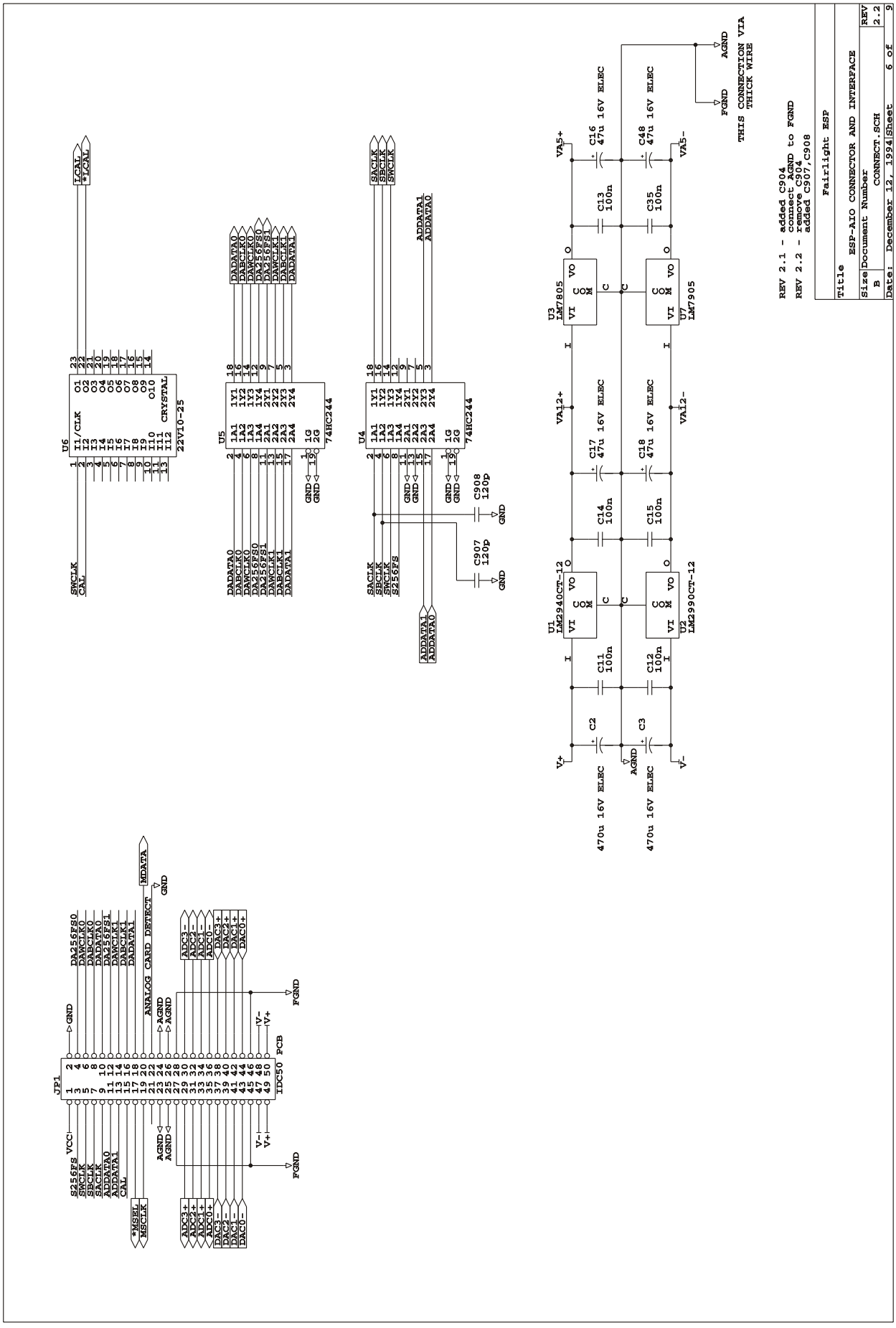
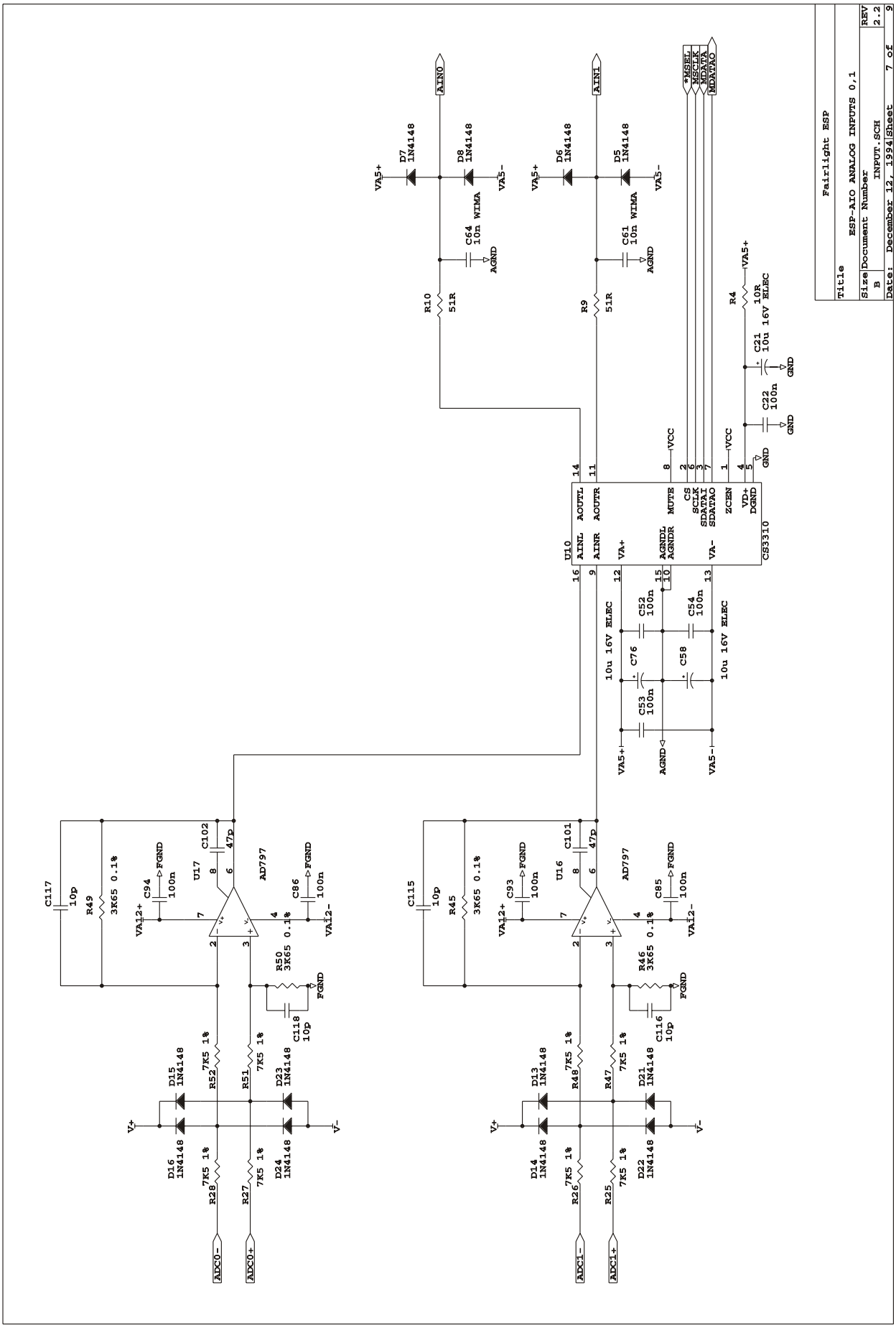
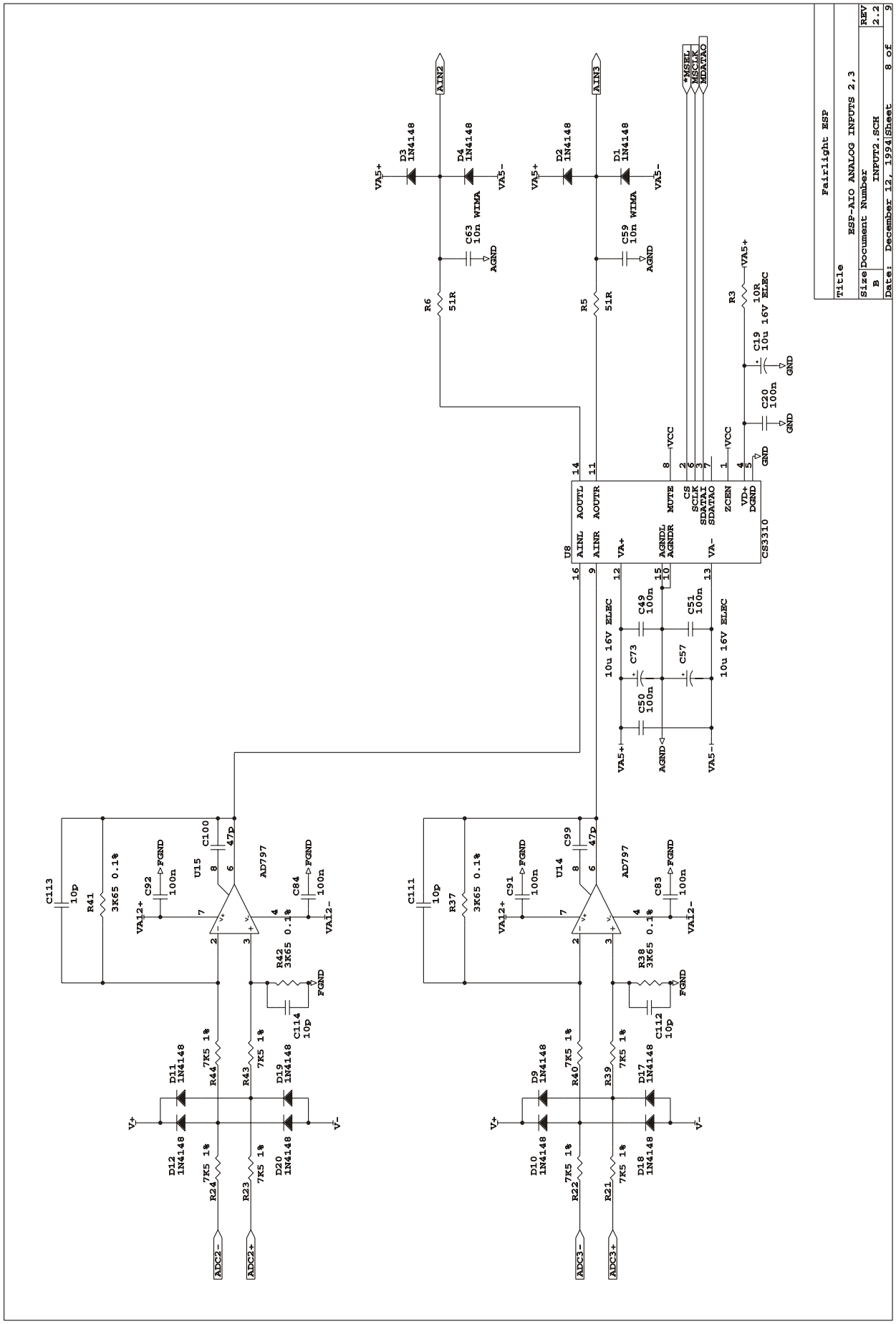
Document Number
OUTPUT.SCH
REV
2.2
Date: December 12, 1994
Sheet
3 of
9
DAC0-
DAC0+
DAC1-
DAC1+
U25
SSM2142
U24
SSM2142
U21
AD797
U20
AD797
C125
10u 50V BP
C126
10u 50V BP
C123
10u 50V BP
C124
10u 50V BP
C109
100n
C90
100n
C107
100n
C89
100n
C68
220p
R19
22K
C82
100n
C98
47p
C72
100n
R20
6K8
C110
10n WIMA
R32
5K1
R36
51R
AOUT0
C67
220p
R17
22K
C81
100n
C97
47p
C71
100n
R18
6K8
C108
10n WIMA
R31
5K1
R35
51R
AOUT1
VA12+
VA12-
AGND
FGND


Fairlight ESP
Title
ESP-AIO ANALOG OUTPUT
Size Document Number REV
B OUTPUT2.SCH 2.2
Date: December 12, 1994 Sheet 4 of 9
DAC2-
DAC2+
DAC3-
DAC3+
C121 10u 50V BP
C122 10u 50V BP
C119 10u 50V BP
C120 10u 50V BP
U23 SSM2142
U22 SSM2142
C105 100n FGND
C88 100n FGND
C103 100n FGND
C87 100n FGND
VA12+
VA12-
AGND
C66 220p
R15 22K
C65 220p
R13 22K
C96 47p
C95 47p
U19 AD797
U18 AD797
C80 100n AGND
C70 100n AGND
C79 100n AGND
C69 100n AGND
R16 6K8
R14 6K8
C106 10n WIMA
C104 10n WIMA
R30 5K1
R29 5K1
R34 51R
R33 51R
AOUT2
AOUT3

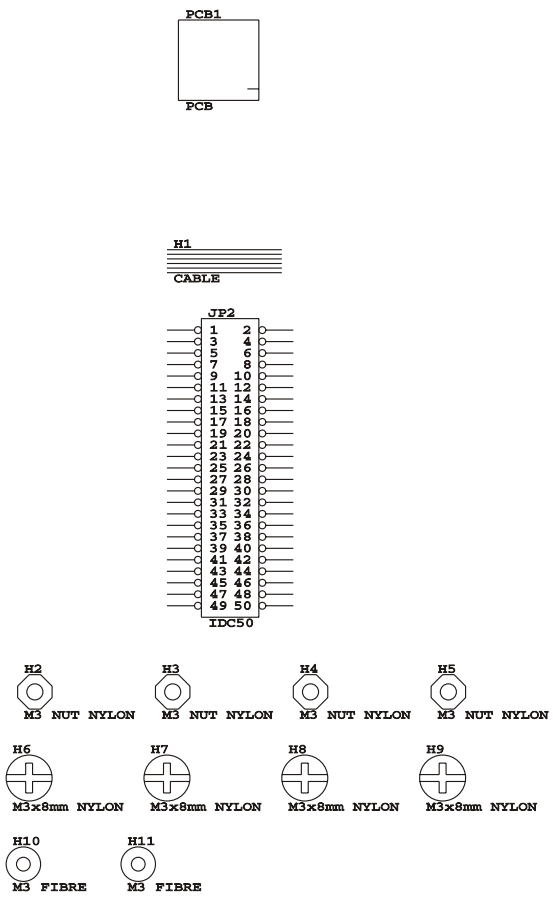

Fairlight ESP
Title
ESP-AIO DAC
Size B
Document Number
DAC.SCH
REV 2.2
Date: December 12, 1994 Sheet 5 of 9
U13
U12
CS4328
VD+
VA+
VA-
VREF
AGND1
AGND2
AGND3
LRCK
BICK
SDATA
RST
XTO
XTI
ACKO
ACKI
DIF1
DIF0
CKS
CMPO
CMPI
CALO
CALI
TST
DGND
AOUTL
AOUTR
VCC
GND
AGND
DAWCLK0
DABCLK0
DADATA0
*LCAL
DA256FS0
DAWCLK1
DABCLK1
DADATA1
DA256FS1
AOUT0
AOUT1
AOUT2
AOUT3
VA5+
VA5-
C5
C6
C9
C10
C23
C24
C25
C26
C33
C34
C42
C43
C44
C45
C46
C47
C55
C56
10u 16V ELEC
100n


REV 2.1 - added C904
connect AGND to FGND
REV 2.2 - remove C904
added C907,C908
THIS CONNECTION VIA THICK WIRE
Fairlight ESP
ESP-AIO CONNECTOR AND INTERFACE
Size B
Document Number CONNECT.SCH
REV 2.2
Date: December 12, 1994 Sheet 6 of 9
U6 22V10-25 CRYSTAL
U5 74HC244
U4 74HC244
U3 LM7805
U7 LM7905
U1 LM2940CT-12
U2 LM2990CT-12
JP1 IDC50 PCB
ANALOG CARD DETECT
C908 120p
C907 120p
C2 470u 16V ELEC
C3 470u 16V ELEC
C11 100n
C12 100n
C13 100n
C14 100n
C15 100n
C16 47u 16V ELEC
C17 47u 16V ELEC
C18 47u 16V ELEC
C35 100n
C48 47u 16V ELEC
VA5+
VA5-
VA12+
VA12-
V+
V-
AGND
FGND
GND
MDATA
SA256FS
SACLK
SBCLK
SWCLK
ADDATA0
ADDATA1
CAL
*MSEL
MSCLK
DA256FS0
DA256FS1
DACLK0
DACLK1
DADATA0
DADATA1
ADC3+
ADC2+
ADC1+
ADC0+
ADC3-
ADC2-
ADC1-
ADC0-
DAC3+
DAC2+
DAC1+
DAC0+
DAC3-
DAC2-
DAC1-
DAC0-

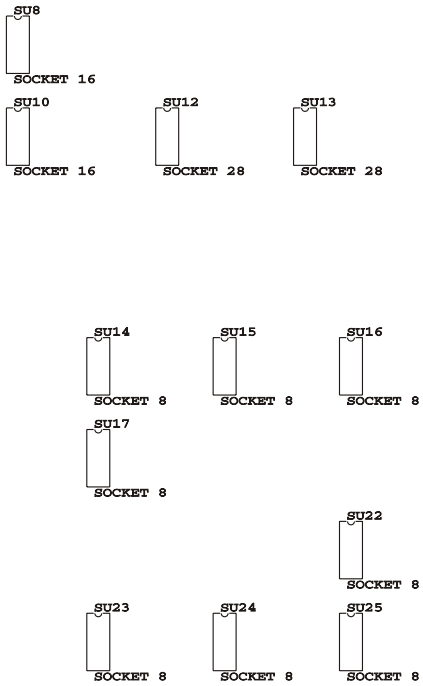

Fairlight ESP
Title
ESP-AIO ANALOG INPUTS 0,1
Size Document Number REV
B INPUT.SCH 2.2
Date: December 12, 1994 Sheet 7 of 9
AIN0
AIN1
*MSEL
MSCLK
MSDATA
MDATAO
D7 1N4148
D8 1N4148
D6 1N4148
D5 1N4148
VA5+
VA5-
C64 10n WIMA
C61 10n WIMA
AGND
R10 51R
R9 51R
R4 10R ELEC
C21 10u 16V
C22 100n
GND
U10
CS3310
AINL
AINR
VA+
AGNDL
AGNDR
VA-
AOUTL
AOUTR
MUTE
CS
SCLK
SDATAI
SDATAO
ZCEN
VD+
DGND
VCC
C52 100n
C54 100n
C76
C58
C53 100n
10u 16V ELEC
VA12+
VA12-
FGND
C117 10p
R49 3K65 0.1%
C115 10p
R45 3K65 0.1%
C94 100n
C93 100n
C102 47p
C101 47p
U17
U16
AD797
C86 100n
C85 100n
R50 3K65 0.1%
R46 3K65 0.1%
C118 10p
C116 10p
D15 1N4148
D23 1N4148
D13 1N4148
D21 1N4148
D16 1N4148
D24 1N4148
D14 1N4148
D22 1N4148
R52 7K5 1%
R51 7K5 1%
R48 7K5 1%
R47 7K5 1%
R28 7K5 1%
R27 7K5 1%
R26 7K5 1%
R25 7K5 1%
V+
V-
ADC0-
ADC0+
ADC1-
ADC1+


Fairlight ESP
Title
ESP-AIO ANALOG INPUTS 2,3
Size B
Document Number
INPUT2.SCH
REV 2.2
Date: December 12, 1994 Sheet 8 of 9
AIN2
AIN3
*MSEL
MSCLK
MDATAO
VA5+
VA5-
D3 1N4148
D4 1N4148
D2 1N4148
D1 1N4148
C63 10n WIMA
C59 10n WIMA
AGND
R6 51R
R5 51R
R3 10R 16V ELEC
C19 10u 16V ELEC
C20 100n
GND
VCC
U8
CS3310
AOUTL
AOUTR
AINL
AINR
VA+
VA-
AGNDL
AGNDR
MUTE
CS
SCLK
SDATAI
SDATAO
ZCEN
VD+
DGND
C49 100n
C51 100n
C73 10u 16V ELEC
C57 10u 16V ELEC
C50 100n
VA12+
VA12-
FGND
C92 100n
C91 100n
C84 100n
C83 100n
U15
U14
AD797
C100 47p
C99 47p
C113 10p
C111 10p
R41 3K65 0.1%
R37 3K65 0.1%
R42 3K65 0.1%
R38 3K65 0.1%
C114 10p
C112 10p
D11 1N4148
D9 1N4148
D19 1N4148
D17 1N4148
D12 1N4148
D10 1N4148
D20 1N4148
D18 1N4148
R44 7K5 1%
R40 7K5 1%
R43 7K5 1%
R39 7K5 1%
R24 7K5 1%
R22 7K5 1%
R23 7K5 1%
R21 7K5 1%
V+
V-
ADC2-
ADC2+
ADC3-
ADC3+

ADDITIONAL HARDWARE



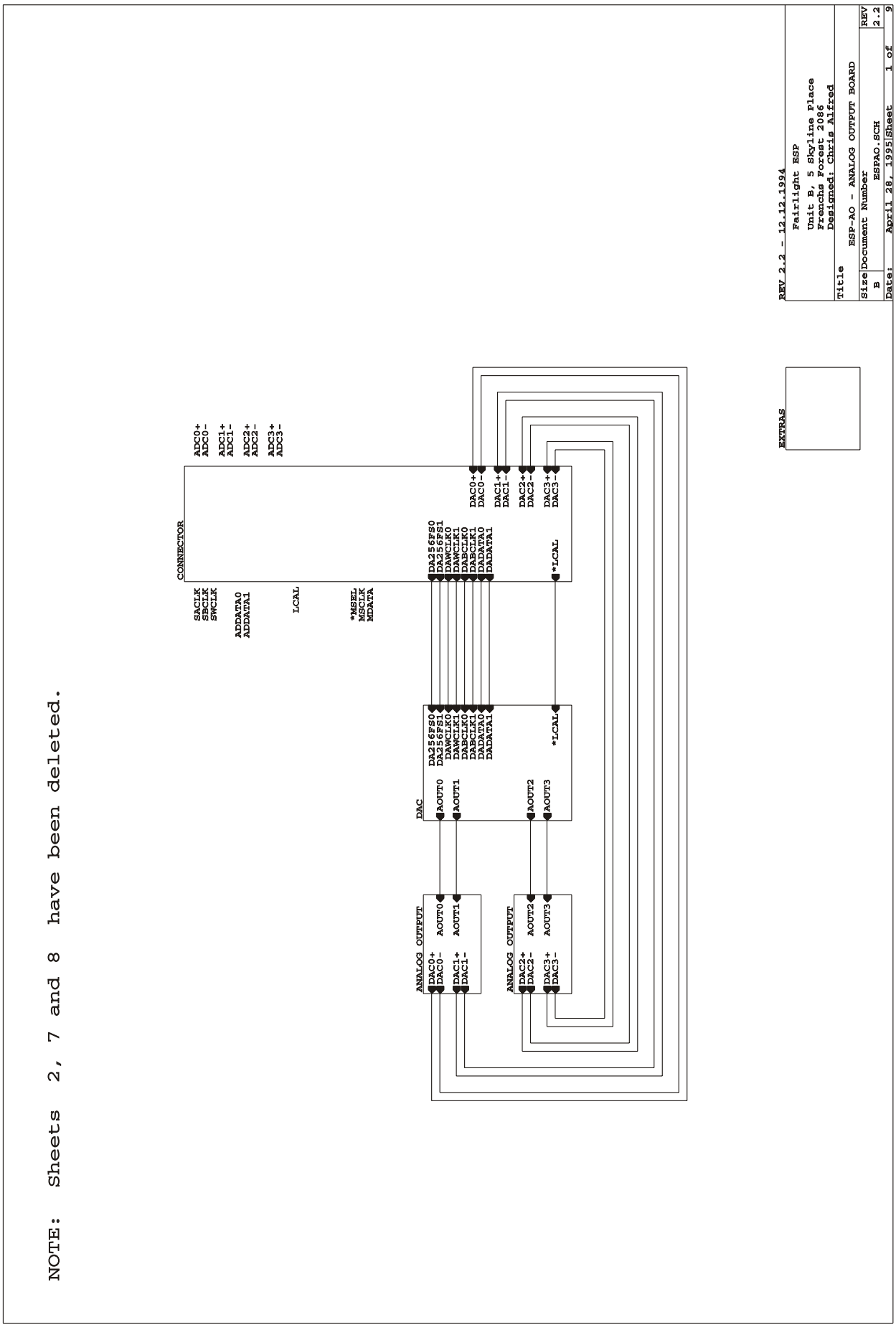
SOCKETS



REV 2.2 - remove U9,U11 sockets

Fairlight ESP		
Title: ESP-AIO SCHEMATIC EXTRAS		
Size: B	Document Number: EXTRAS.SCH	REV: 2.2
Date: December 12, 1994	Sheet 9 of 9	

16.4 ESPAO SCHEMATICS



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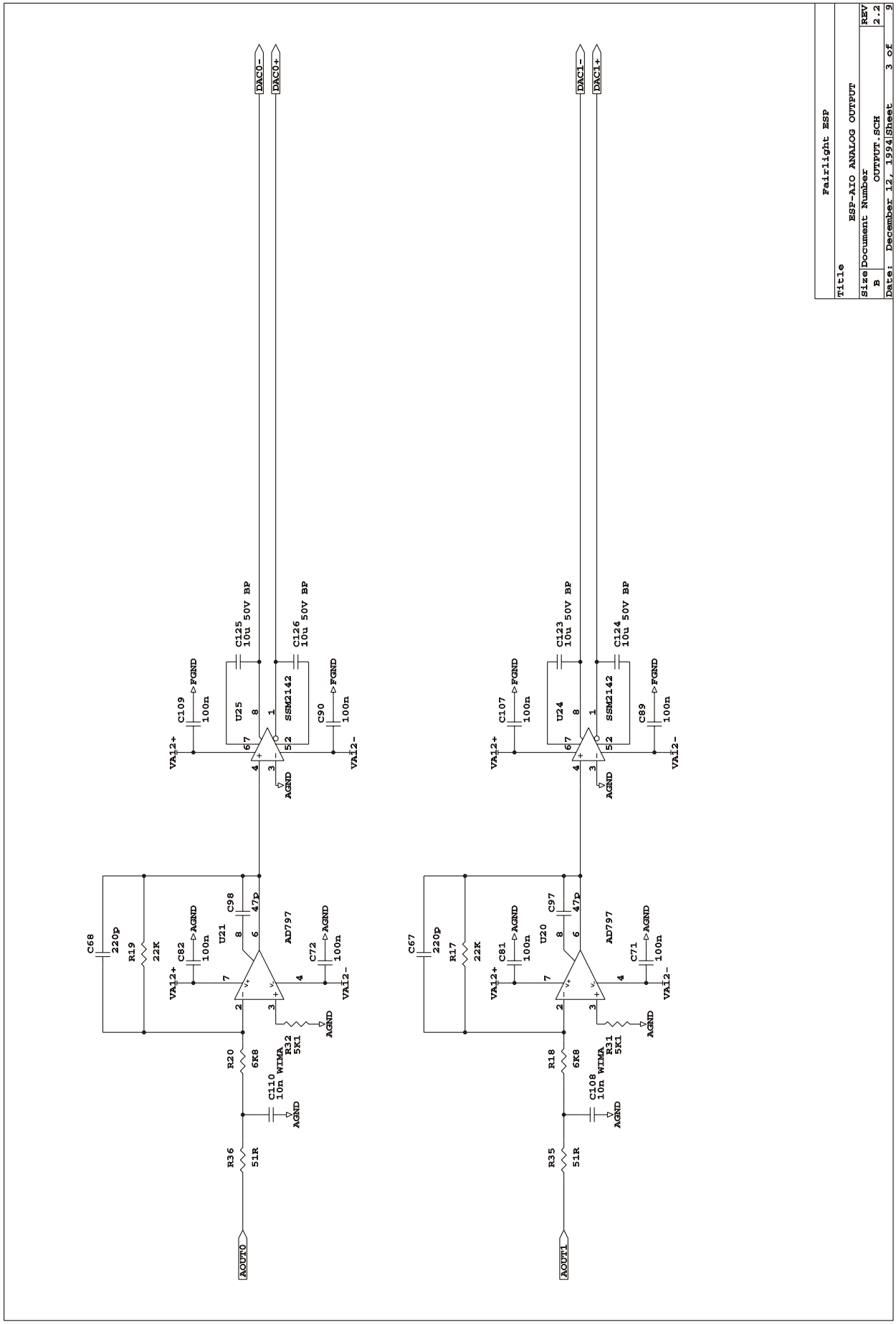
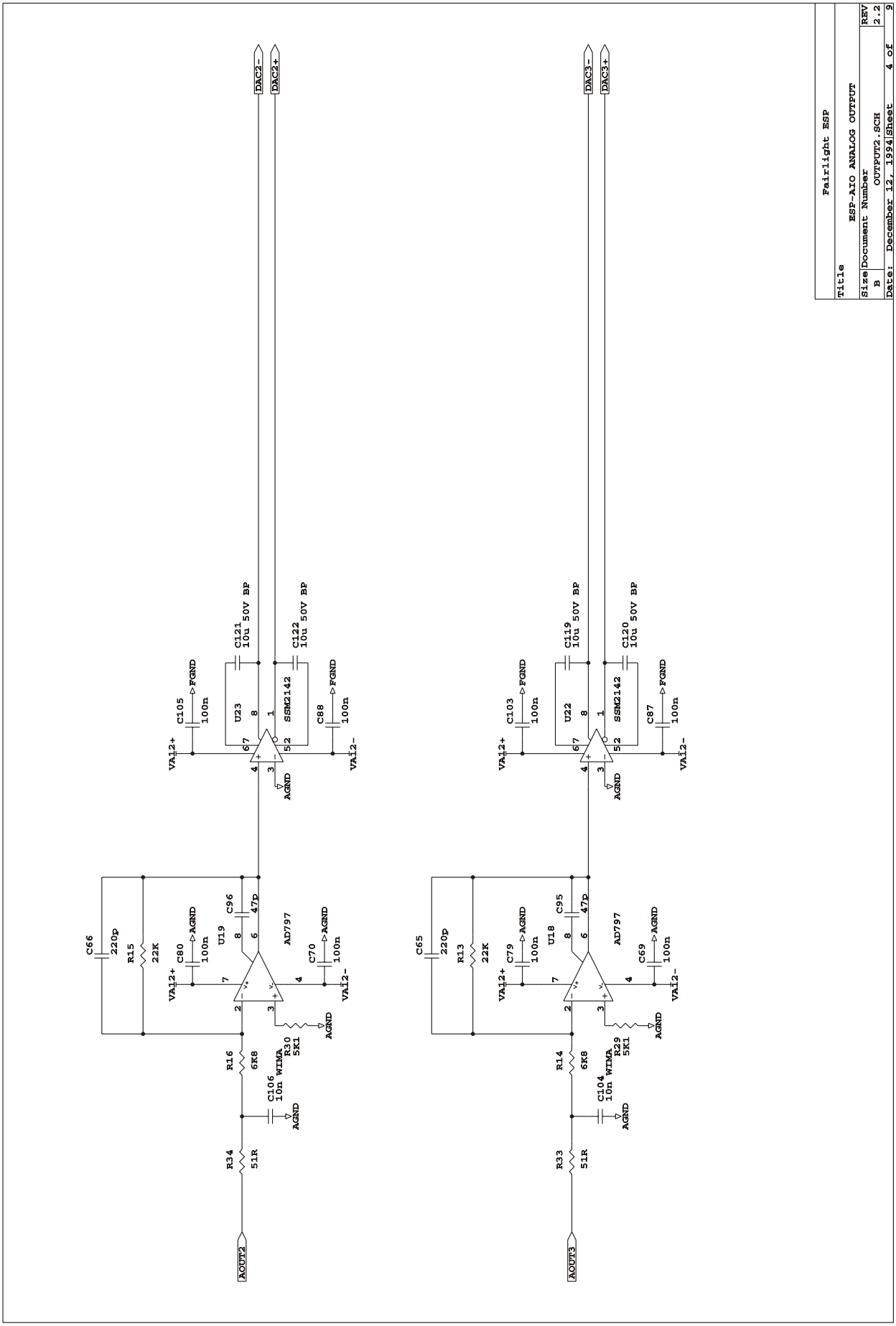
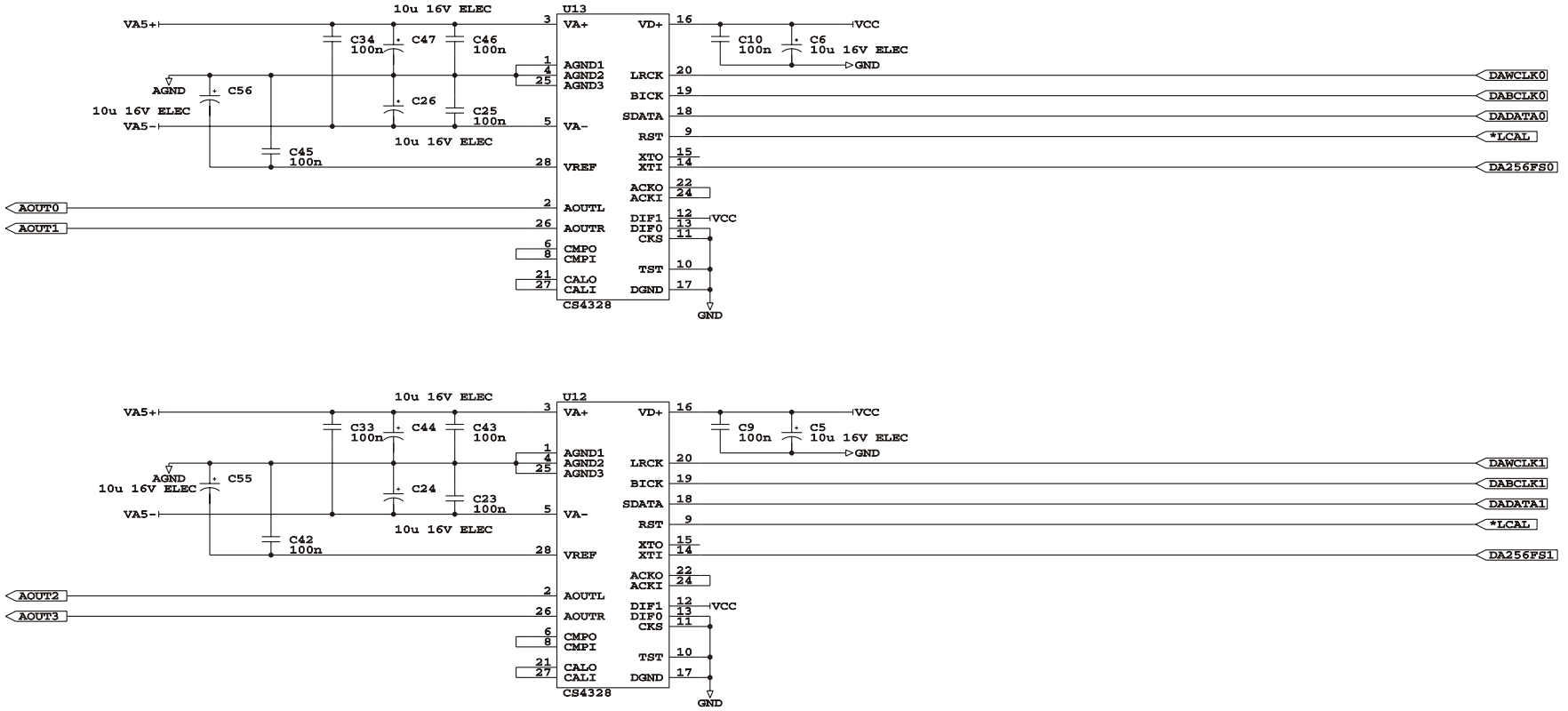

Fairlight ESP
Title
ESP-AIO ANALOG OUTPUT
Size
B
Document Number
OUTPUT.SCH
REV
2.2
Date: December 12, 1994
Sheet
3 of
9
DAC0-
DAC0+
DAC1-
DAC1+
U25
U24
U21
U20
SSM2142
AD797
C125
C126
C123
C124
C109
C107
C90
C89
C98
C97
C82
C81
C72
C71
C68
C67
R19
R17
R20
R18
R32
R31
C110
C108
R36
R35
AOUT0
AOUT1
VA12+
VA12-
AGND
FGND
10u 50V BP
100n
47p
220p
22K
6K8
5K1
10n WIMA
51R


DAC2-
DAC2+
DAC3-
DAC3+
C121 10u 50V BP
C122 10u 50V BP
C119 10u 50V BP
C120 10u 50V BP
U23
U22
SSM2142
C105 100n
C88 100n
C103 100n
C87 100n
VA12+
VA12-
AGND
PGND
C66 220p
R15 22K
C80 100n
C96 47p
U19
AD797
C70 100n
R16 6K8
R30 5K1
C106 10n WIMA
R34 51R
AOUT2
C65 220p
R13 22K
C79 100n
C95 47p
U18
C69 100n
R14 6K8
R29 5K1
C104 10n WIMA
R33 51R
AOUT3
Fairlight ESP
Title
ESP-AIO ANALOG OUTPUT
Size
B
Document Number
OUTPUT2.SCH
REV
2.2
Date: December 12, 1994
Sheet
4 of
9



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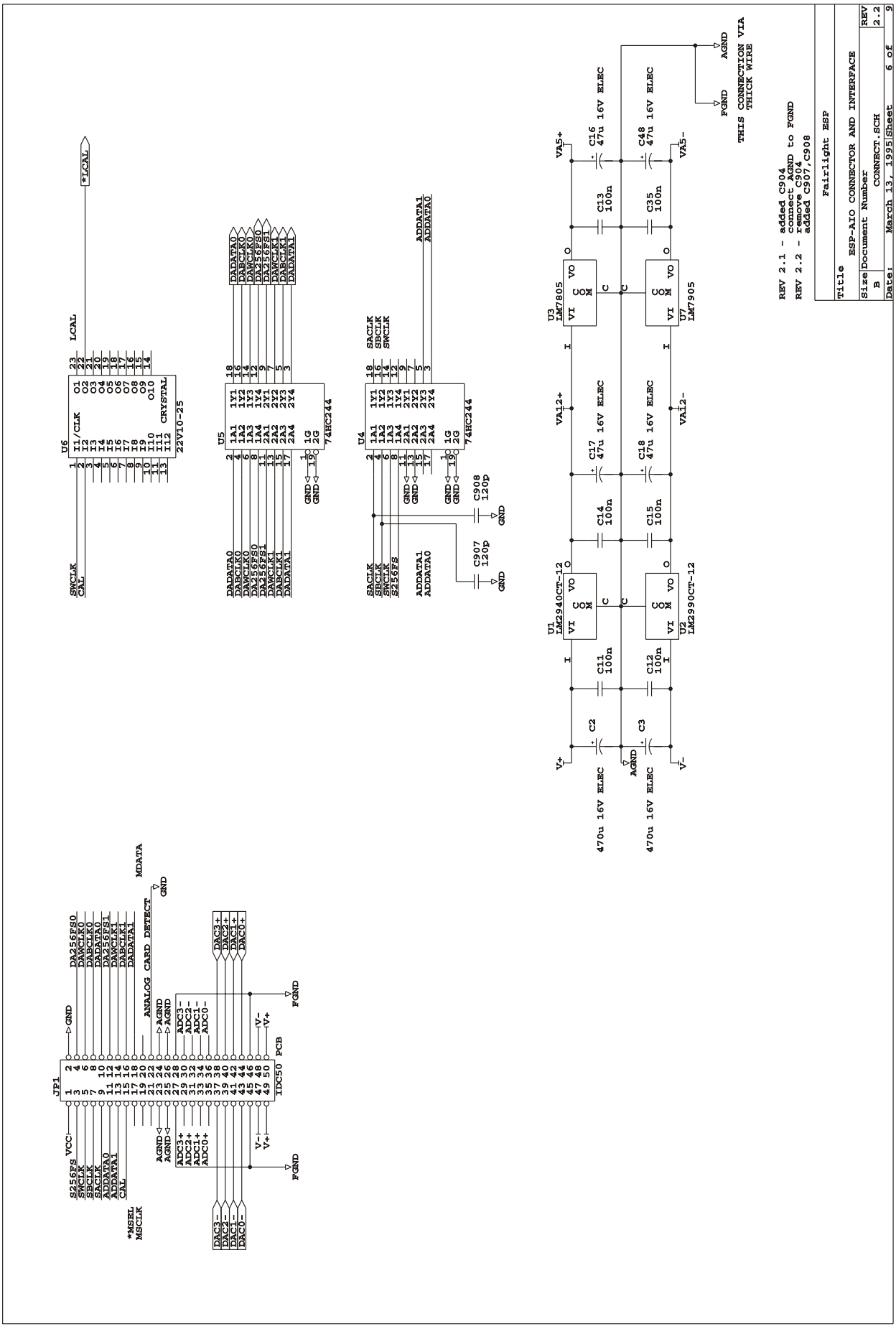
Title: ESP-AIO DAC		
Size: B	Document Number: DAC.SCH	REV: 2.2
Date: December 12, 1994	Sheet: 5 of	9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connect AGND to FGND
REV 2.2 - remove C904
added C907,C908
Fairlight ESP
Title
ESP-AIO CONNECTOR AND INTERFACE
Size Document Number REV
B CONNECT.SCH 2.2
Date: March 13, 1995 Sheet 6 of 9
THIS CONNECTION VIA THICK WIRE
AGND
FGND
VA5+
VA5-
VA12+
VA12-
U1 LM2940CT-12
U2 LM2990CT-12
U3 LM7805
U7 LM7905
C2 470u 16V ELEC
C3 470u 16V ELEC
C11 100n
C12 100n
C13 100n
C14 100n
C15 100n
C16 47u 16V ELEC
C17 47u 16V ELEC
C18 47u 16V ELEC
C35 100n
C48 47u 16V ELEC
U4 74HC244
U5 74HC244
U6 22V10-25
C907 120p
C908 120p
JP1 IDC50 PCB
ANALOG CARD DETECT
MDATA
*MSEL
MSCLK
CAL
*LCAL
LCAL
SWCLK
SACLK
SBCLK
SWCLK
S256FS
ADDATA0
ADDATA1
DADATA0
DADATA1
DABCLK0
DABCLK1
DAWCLK0
DAWCLK1
DA256FS0
DA256FS1
DAC3+
DAC2+
DAC1+
DAC0+
DAC3-
DAC2-
DAC1-
DAC0-
ADC3+
ADC2+
ADC1+
ADC0+
ADC3-
ADC2-
ADC1-
ADC0-
VCC
GND
AGND
V+
V-
FGND

Sheet 7 Removed

Sheet 8 Removed

ADDITIONAL HARDWARE

PCB1
PCB

H1
CABLE

JP2
1 2
3 4
5 6
7 8
9 10
11 12
13 14
15 16
17 18
19 20
21 22
23 24
25 26
27 28
29 30
31 32
33 34
35 36
37 38
39 40
41 42
43 44
45 46
47 48
49 50
IDC50

H2 M3 NUT NYLON
H3 M3 NUT NYLON
H4 M3 NUT NYLON
H5 M3 NUT NYLON
H6 M3x8mm NYLON
H7 M3x8mm NYLON
H8 M3x8mm NYLON
H9 M3x8mm NYLON
H10 M3 FIBRE
H11 M3 FIBRE

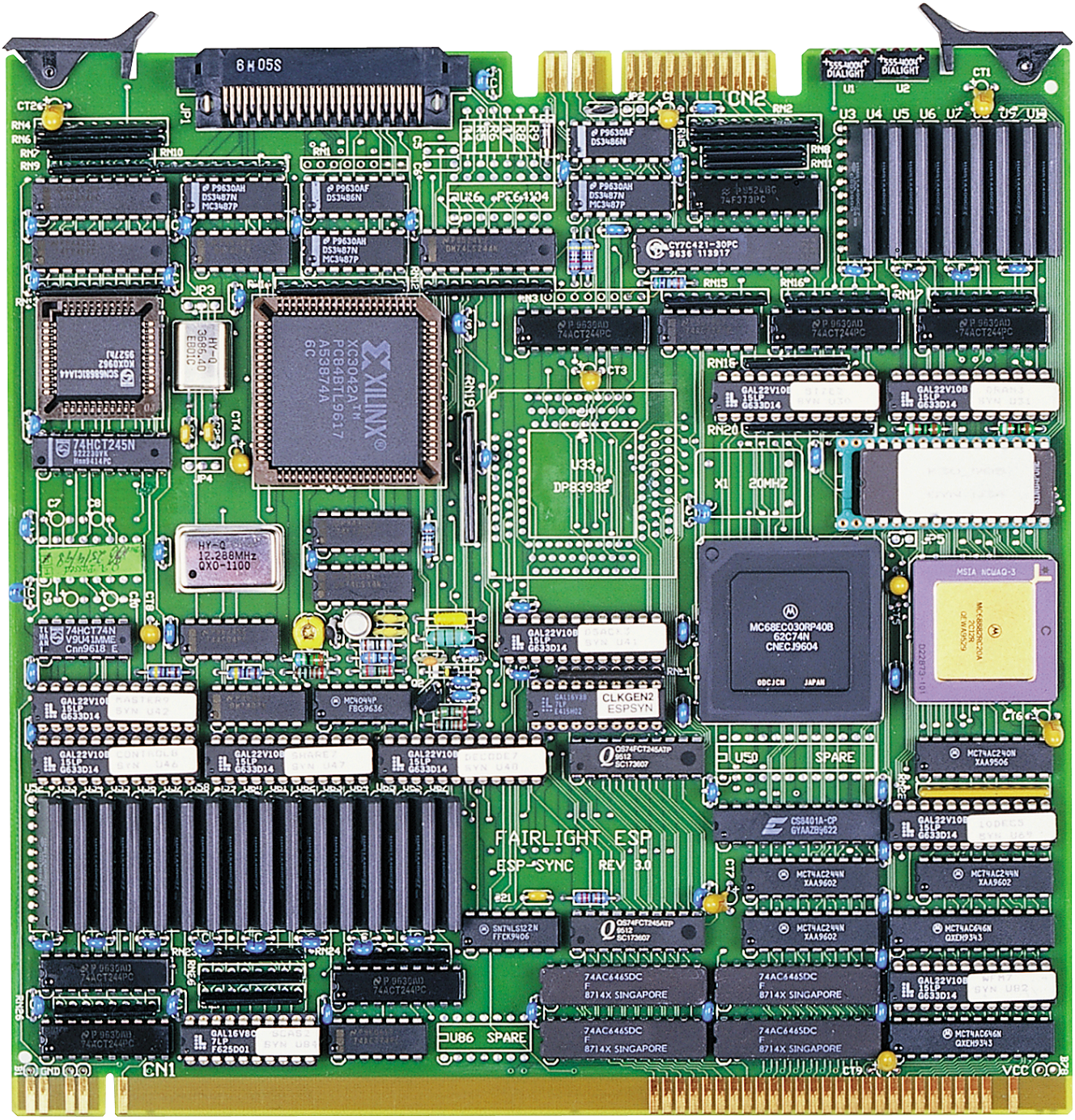
SOCKETS

SU8 SOCKET 16
SU6 SOCKET 24
SU10 SOCKET 16
SU12 SOCKET 28
SU13 SOCKET 28
SU14 SOCKET 8
SU15 SOCKET 8
SU16 SOCKET 8
SU17 SOCKET 8
SU22 SOCKET 8
SU23 SOCKET 8
SU24 SOCKET 8
SU25 SOCKET 8

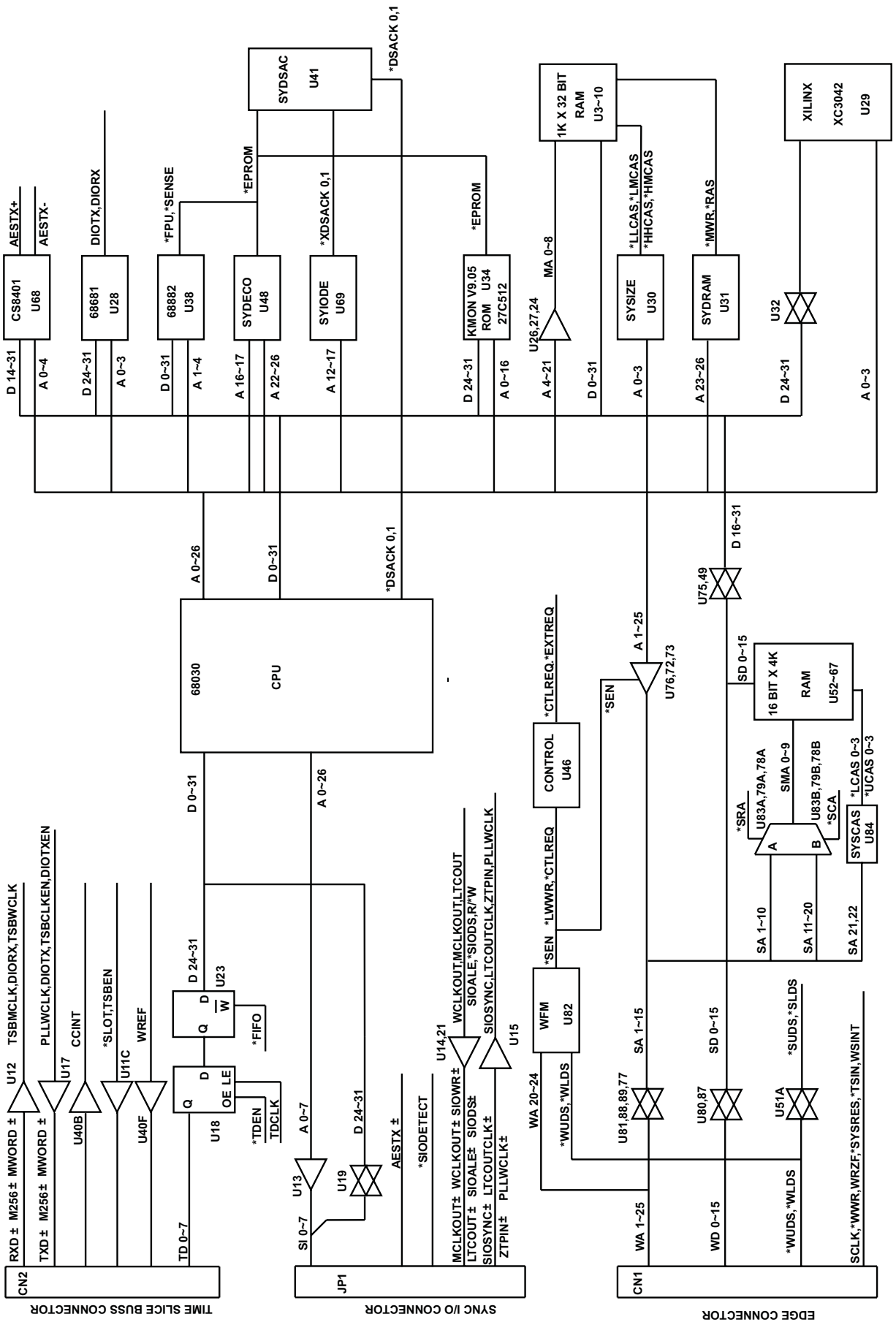
REV 2.2 - remove U9,U11 sockets

Fairlight ESP		
Title: ESP-AIO SCHEMATIC EXTRAS		
Size: B	Document Number: EXTRAS.SCH	REV: 2.2
Date: December 12, 1994	Sheet 9 of 9	

17.0 ESPSYN Sync Card



17.1 ESPSYN Block Diagram



17.2 ESPSYN Diagnostics

17.2.1 66MHz PLL

U44 (4044) provides the phase detection and voltage control. D2 (BB809 varactor) and components around Q1 (2N2369) form a voltage controlled Hartley oscillator. U45 (CLKGEN) divides 66M to produce SREF to feed back into U44 for phase comparison. When the PLL is locked, U45/12 should be high (*UNLOCKED = 1) and UNLOCKED LED (bottom LED) should be off (NOTE: led will also be off if oscillator is not running). If the oscillator is operational and the UNLOCKED LED is on, then adjust C15 until UNLOCKED LED extinguishes.

Signal states when operational

- U44/1 SCLK 100nS high/200nS low
- U44/3 SREF 100nS high/200nS low
- U44/5 1.8V
- U44/9 1.7V
- U44/8 2.03V
- D2/cathode 66MHz sine 0V to 4V
- Q1/base 66MHz sine -2.19V to 4.3V
- Q1/emitter 66MHz triangle pulse 0V to 3.3V
- U45/19 33MHz
- U45/18 33MHz (inverse of U45/19)
- U45/17 16MHz

SYNC PLL Adjustment

Note: ESPWX card must be installed. TSR and DCCs may be installed but are not necessary.

1. Turn off unit
2. Remove Sync card from unit
3. Insert extender card into unit in the slot the card came out of.
4. Insert Sync card to be tested into extender card.
5. Turn on unit.
6. Measure the DC voltage between U44 pin 8, and ground (frame ground is suitable). Adjust C15 (6-23pf variable capacitor) so the voltage at pin 8 is between 1.8 and 2.3 volts. This should correspond with the bottom led being dim.
7. Turn off unit.
8. Remove extender card and re-insert Sync card into unit.

The Oscillator should operate at about 68MHz when U44 is removed (i.e. feedback loop is open).

17.2.2 256x Wordclock crystals

(see sheet 2)

Signal states when operational

- U35/12 8.192MHz
- U35/8 11.2783MHz
- U36/12 12.2986MHz
- U36/8 12.288MHz

17.2.3 LED Indicators

The diagnostic LEDs indicate the following:

RESET	Reset
HALT	Halt
INT TO SC	Interrupt to Sync Card
INT TO WS	Interrupt to Wave Exec
SC ACCESS	Syn Card Access to Shared DRAM
WS ACCESS	Wave Exec Access to Shared DRAM
INTACK	No Interrupts Pending
UNLOCKED	PLL Unlocked

Upon reset, the RESET, HALT, and INTACK LEDs should be lit. Once the WS starts (all WS LEDs turn off), the screen will clear and the SC LEDs will show the INTACK LED lit, and the SHARE LED dim.

17.2.4 Shared memory

There is 8MB of dram accessable by both the SC and WS. For both processors, the ram appears at $4800000-$4FFFFFF. The shared memory interface operates at double the speed of the Waveform Buss with the first half cycle allocated to the SC, and the second half to the WS. If the WS is not accessing shared memory, then both halves are available to the SC.

When the SC is operational (i.e. the top two LEDs are off), the first 64k of shared memory is used for communication between the WS and SC.

17.2.5 Sync card Test

1. Connect TSB cable and sync i/o cable

2. Boot system

3. Check unlock led
   If on – adjust c15 until dim (see Sync Card PLL adjustment sheet)
   If off – restart system

4. Restart system

5. Press **space bar** at initial screen to display boot menu, you should have following menu:

```
Booting Procedures available . . . . < input > . . . . < arg >

Boot from PCI SCSI Disk Drive       -    <pci>

Boot from Turbo SCSI Disk Drive     -    <ts>

Display Devices on PCI SCSI         -    <scanpci>

Display Devices on Turbo SCSI       -    <scants>

Boot from Flash ROM                 -    <rom>

Enter Kmon30 on the Sync Card       -    <kmon>

Enter  Diagnostics                  -    <diag>

Reconfigure  NVRAM                  -    <rc>

Erase NVRAM and Restart system      -    <nure>

Restart  System                     -    <q>

Select a boot method from above menu:
```

6. Enter kmon30 on the sync card by typing:

   kmon (enter kmon30 on the sync card)

7. The following should show on screen:

```
Sync  Card  Monitor  Vxx.xx

68040 is Ready . . . . 68030 is Ready . . . .

Fairlight E.S.P 68030 Monitor Vxx.xx
```

8. At " **Q:** " prompt, type:

   z (for sync card diagnostics)

   Following should show on screen:

```
Sync Card Memory Tests Vx.xx

Features Enabled

_____________

Report Passes

Report Errors

Memory Tests Enabled

_________________

all

ADDRESS RANGE  Start: 04900000  End: 04 f f f f f f <7 Meg>

SCDIAG>
```

9. For the memory tests, type the following at the scdiag> prompt for each test:

   m 4900000-4 f f f f f f (tests shared memory 7 meg)
   (1st 1M used for communications with WX)

   m 1900000-1b f f f f f (tests local memory 3 meg)
   (1st 1M used for SC monitor)

   these are continuous tests. To halt the tests - **reset** machine and start over

17.2.6 System tests

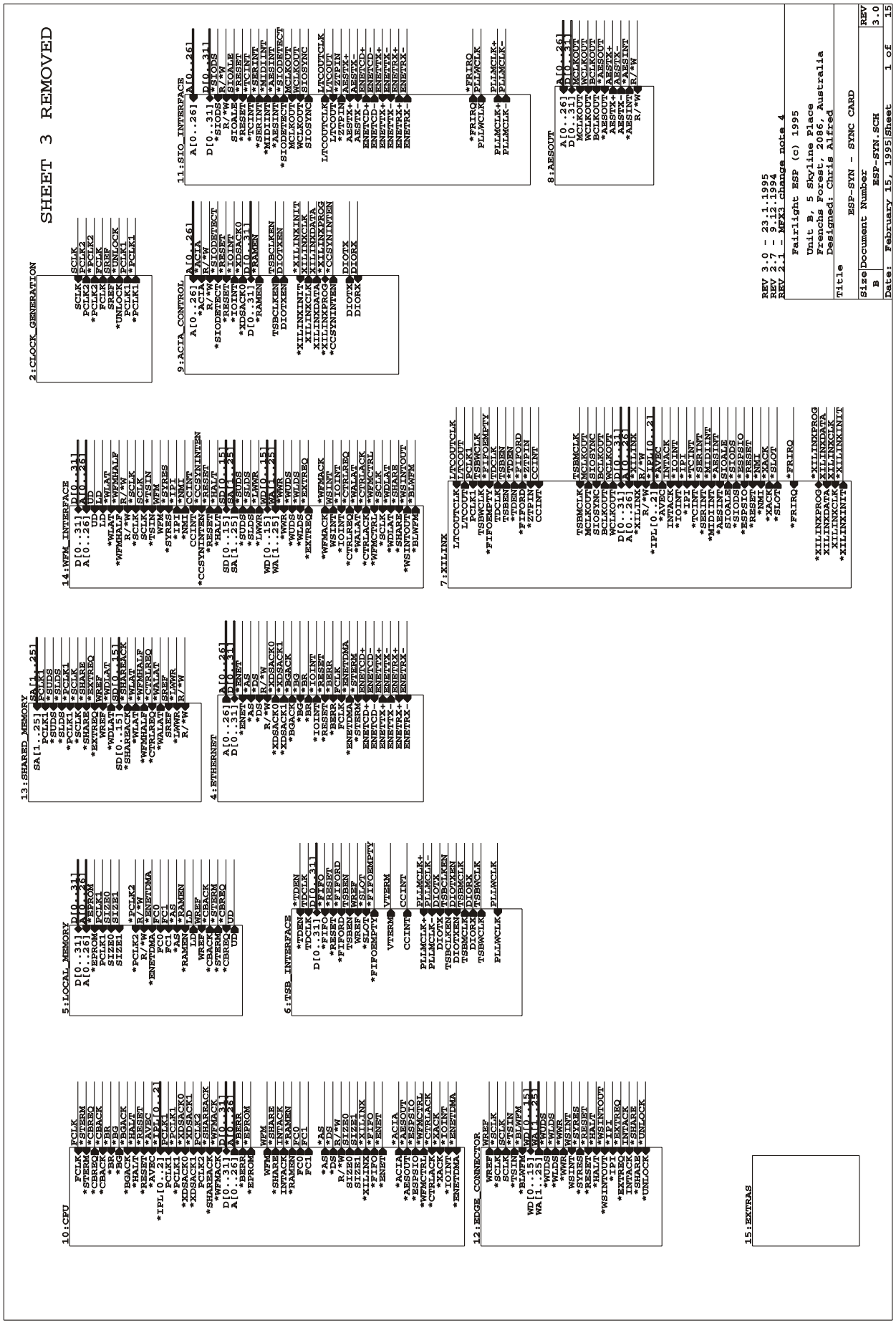
The following tests are to be made in playback and record.

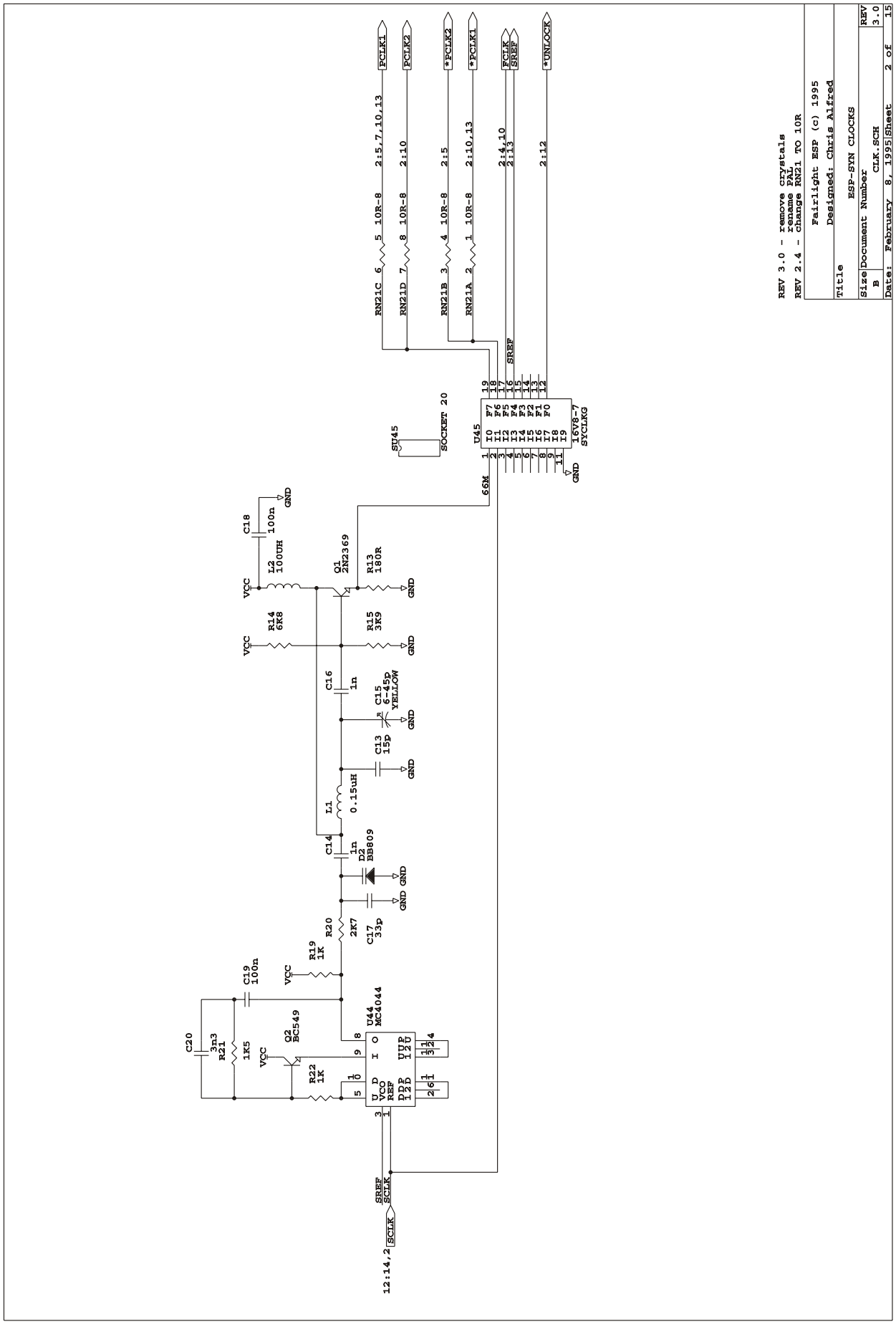
Playback and record different projects with the following Sync's:

Sync	INT	VIDEO	AES	INPUT	WCLK
	48k	25 pal	48k	48k	48k
	44.1k	DF ntsc	44.1k	44.1k	44.1k
	44.056k		32k	32k	32k
	32k				

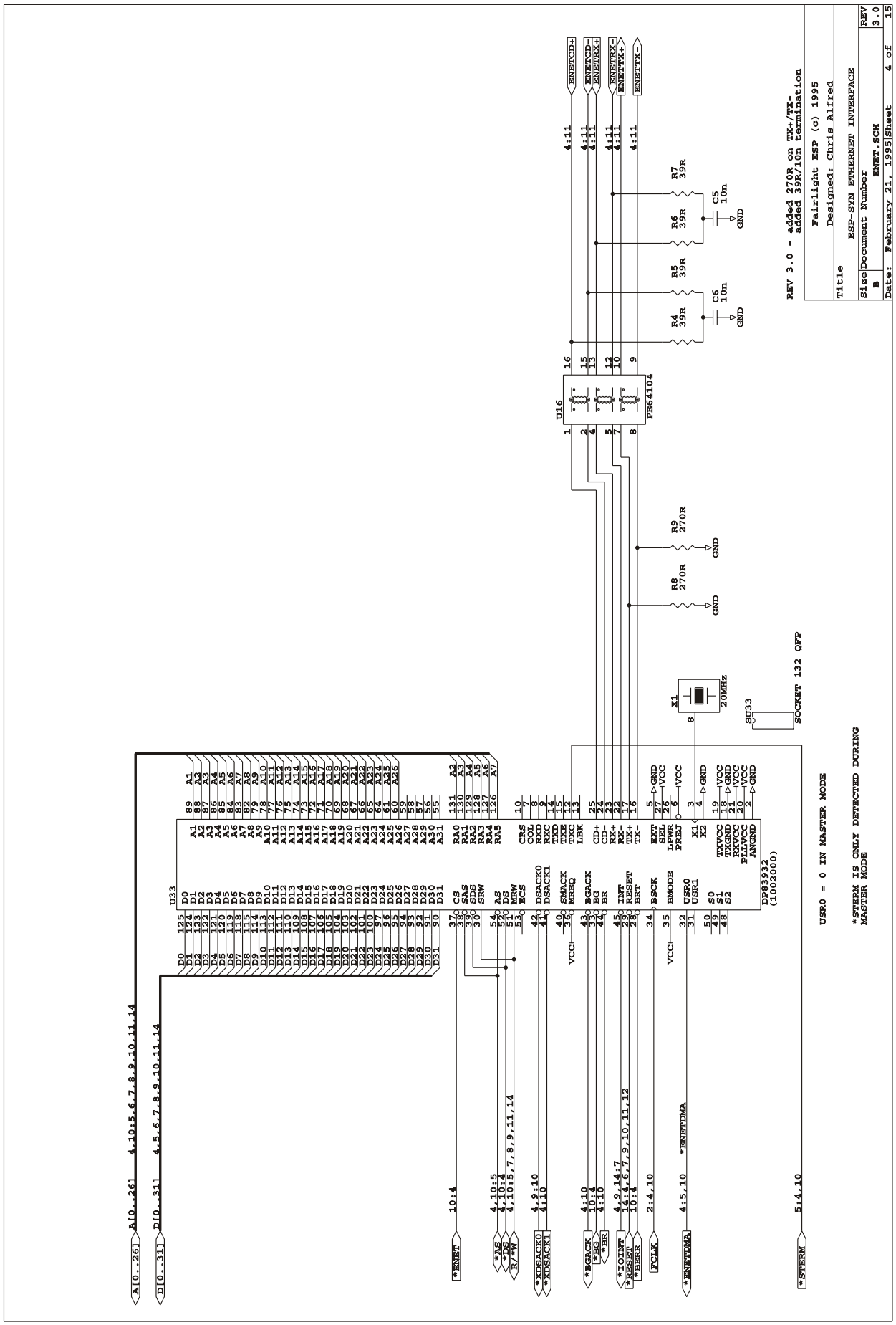
also test the LTC generator

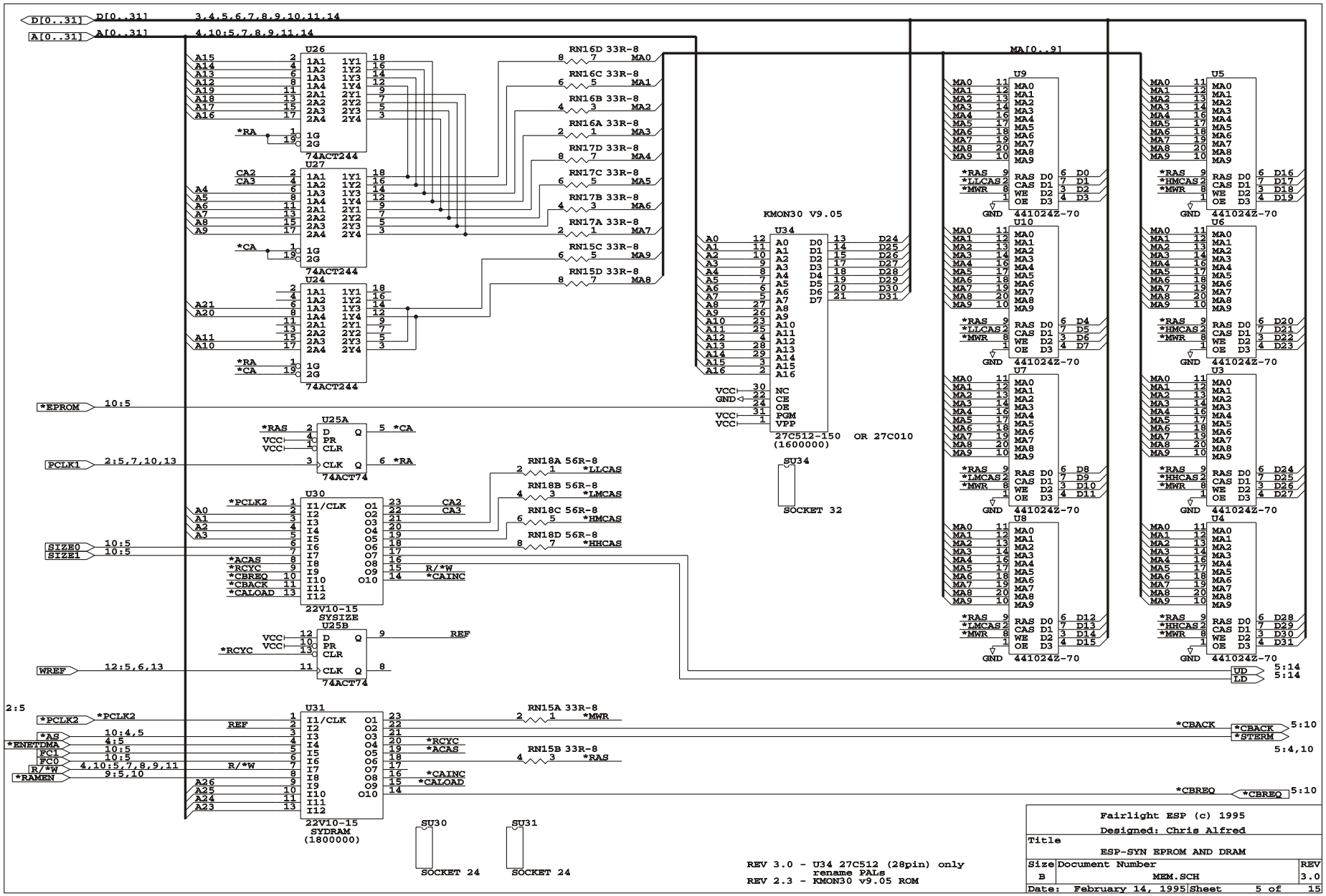
17.3 ESPSYN Sync Card Schematics

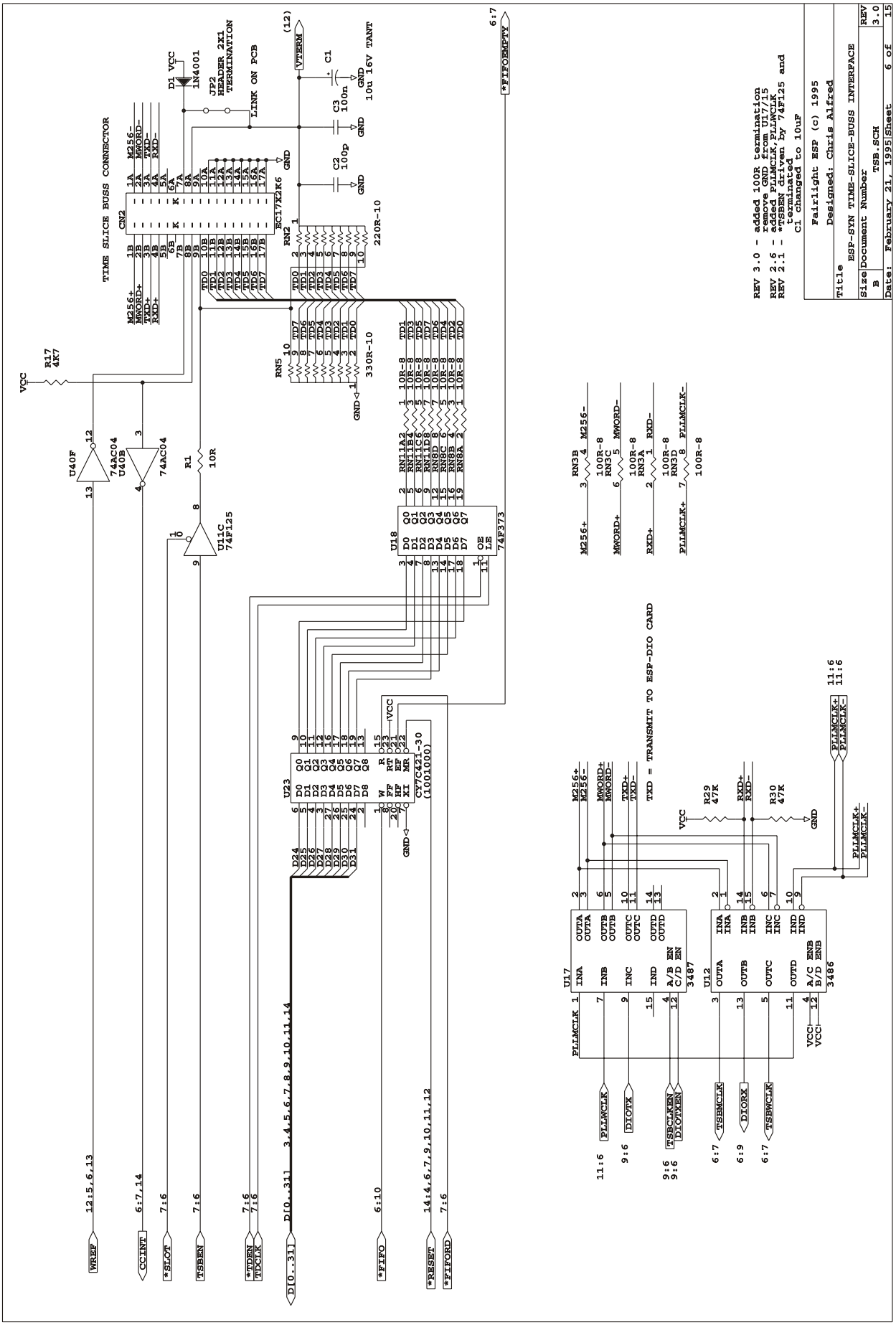


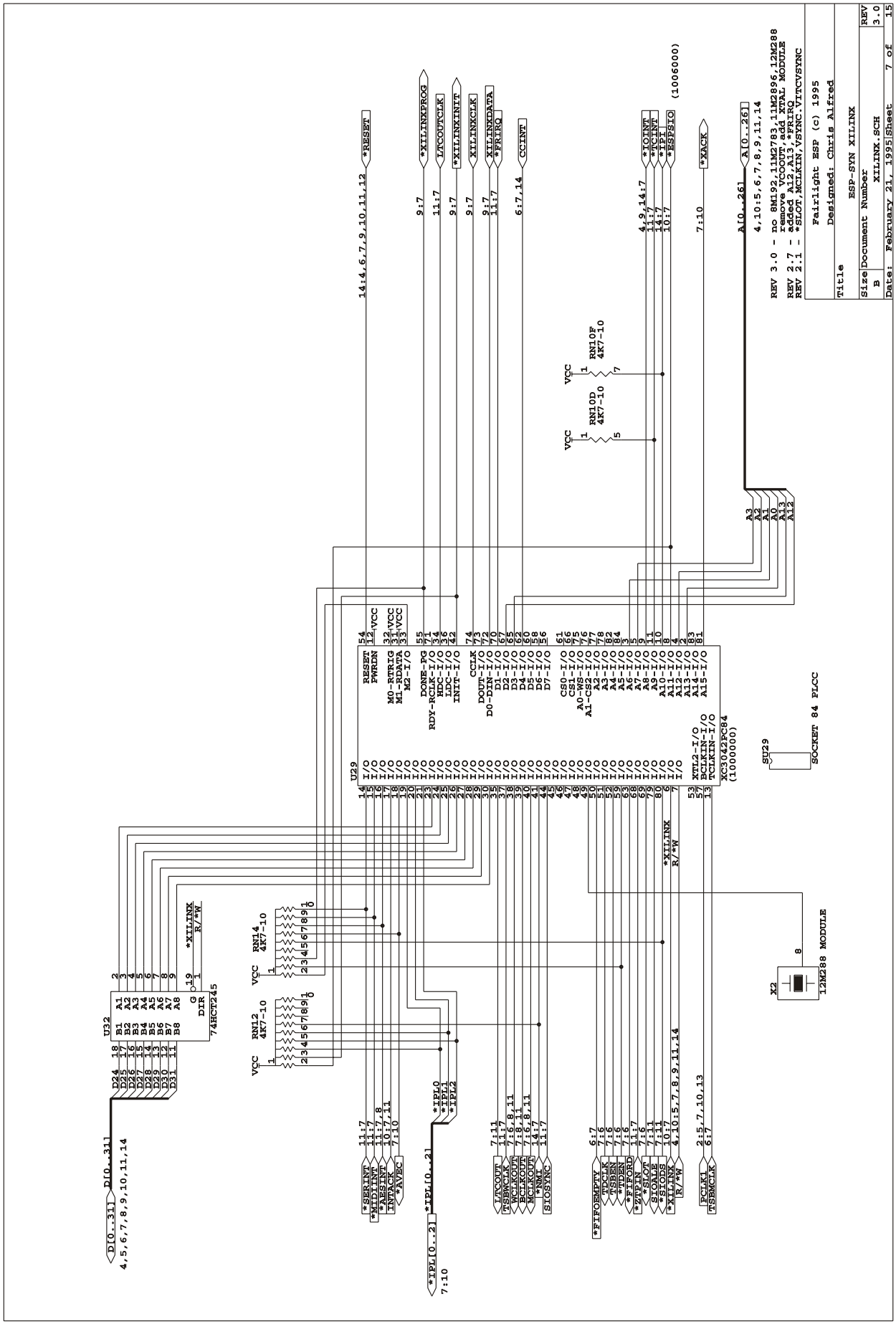

REV 3.0 - remove crystals
rename PAL
REV 2.4 - change RN21 TO 10R
Fairlight ESP (c) 1995
Designed: Chris Alfred
Title
ESP-SYN CLOCKS
Size Document Number REV
B CLK.SCH 3.0
Date: February 8, 1995 Sheet 2 of 15
FCLK1
FCLK2
*FCLK2
*FCLK1
FCLK
SREF
*UNLOCK
RN21C 6 5 10R-8 2:5,7,10,13
RN21D 7 8 10R-8 2:10
RN21B 3 4 10R-8 2:5
RN21A 2 1 10R-8 2:10,13
2:4,10
2:13
2:12
SU45
SOCKET 20
U45
16V8-7
SYCLKG
66M
C18 100n
L2 100UH
Q1 2N2369
R13 180R
R14 6K8
R15 3K9
C16 1n
C15 6-45p YELLOW
C13 15p
L1 0.15uH
C14 1n
D2 BB809
R20 2K7
C17 33p
R19 1K
C19 100n
U44 MC4044
C20 3n3
R21 1K5
Q2 BC549
R22 1K
SREF
SCLK
12:14,2 SCLK
VCC
GND

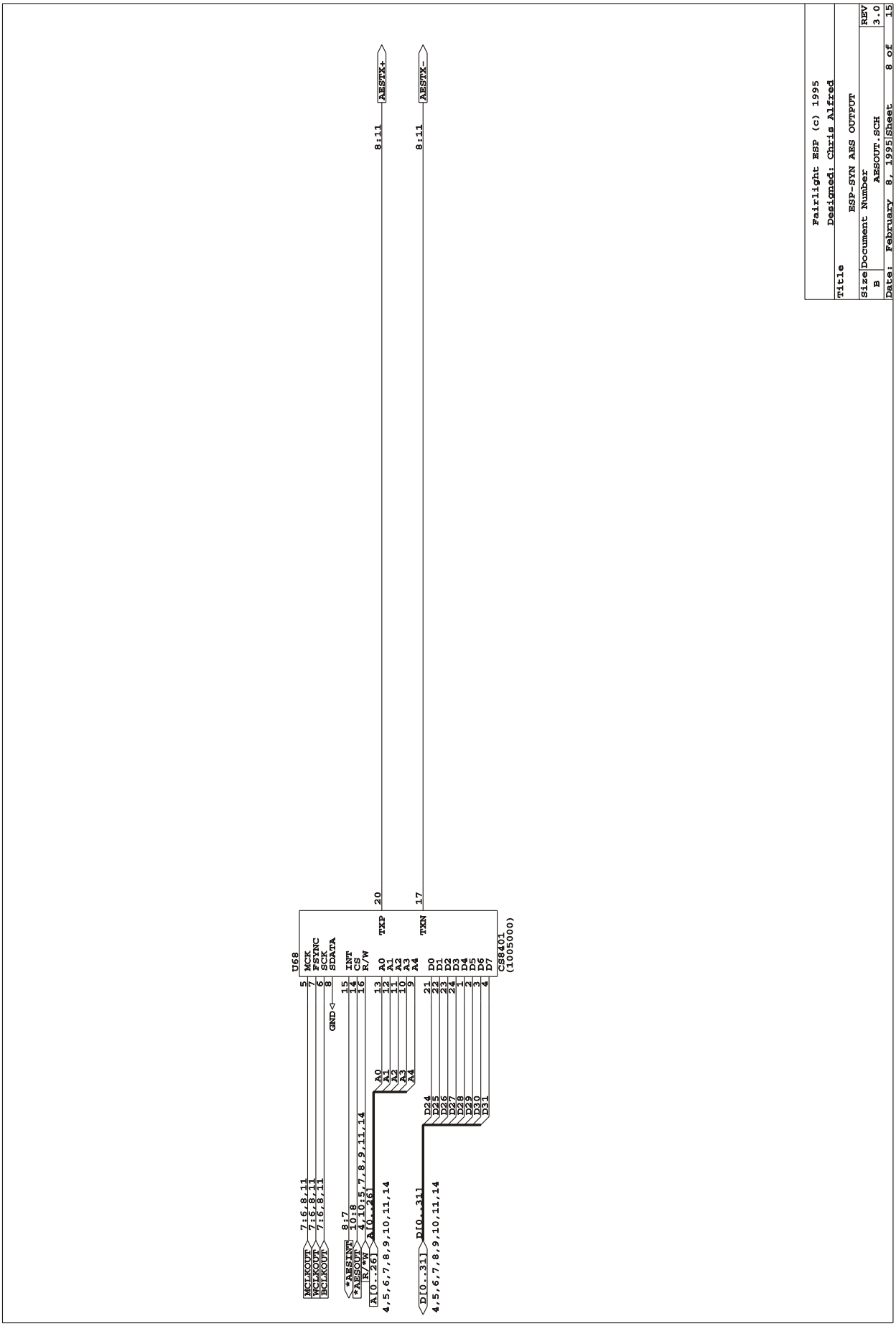
Sheet 3 Removed

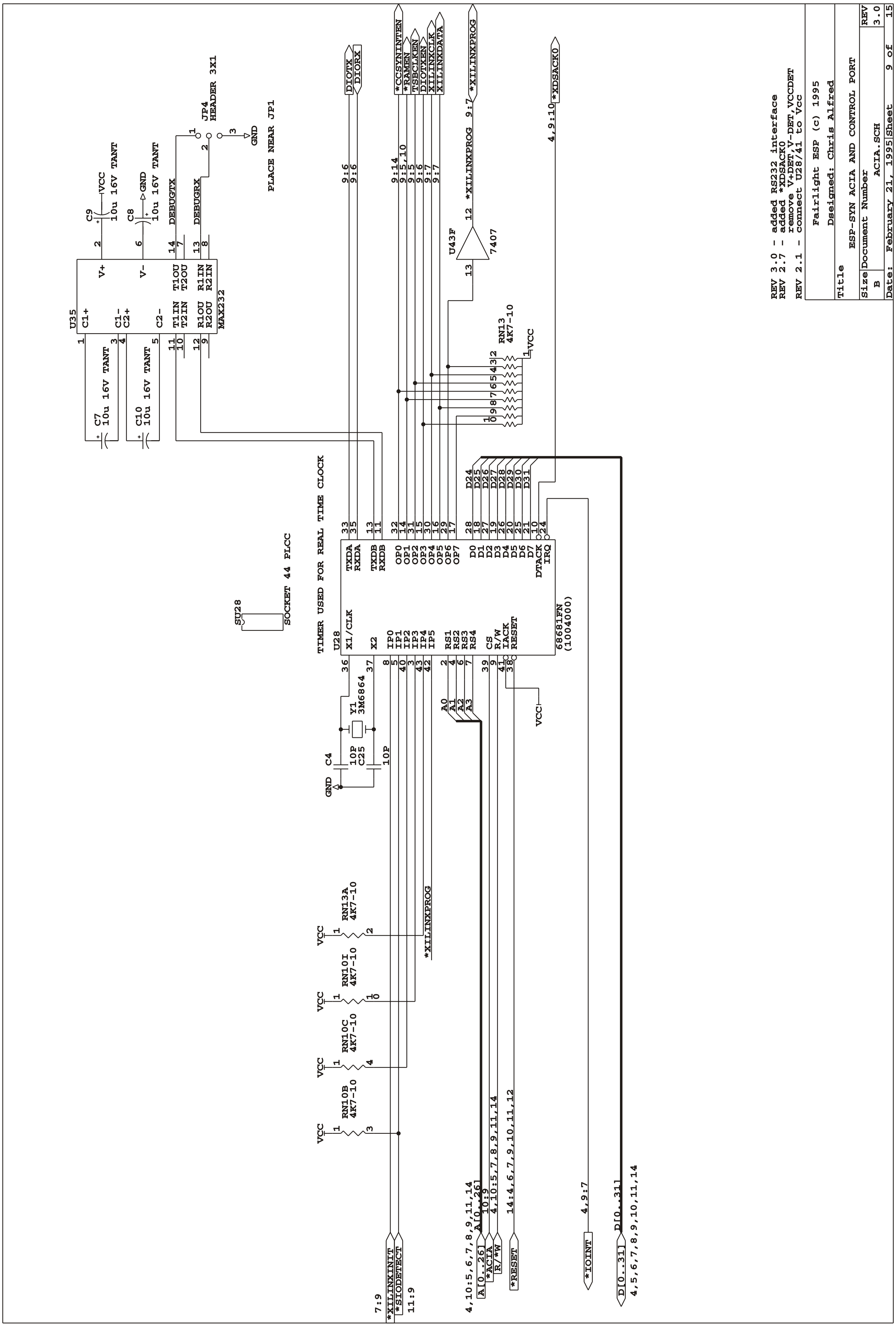

A[0..26] A[0..26] 4,10:5,6,7,8,9,10,11,14
D[0..31] D[0..31] 4,5,6,7,8,9,10,11,14
U33
DP83932 (1002000)
U16
PE64104
X1
20MHz
SU33
SOCKET 132 QFP
R4 39R
R5 39R
R6 39R
R7 39R
R8 270R
R9 270R
C5 10n
C6 10n
GND
VCC
*ENET
*AS
*DS
R/*W
*XDSACK0
*XDSACK1
*BGACK
*BR
*IOINT
*RESET
*BERR
FCLK
*ENETDMA
*STERM
ENETCD+
ENETCD-
ENETRX+
ENETRX-
ENETTX+
ENETTX-
REV 3.0 - added 270R on TX+/TX-
added 39R/10n termination
Fairlight ESP (c) 1995
Designed: Chris Alfred
Title
ESP-SYN ETHERNET INTERFACE
Size B
Document Number
ENET.SCH
REV 3.0
Date: February 21, 1995 Sheet 4 of 15
USR0 = 0 IN MASTER MODE
*STERM IS ONLY DETECTED DURING MASTER MODE

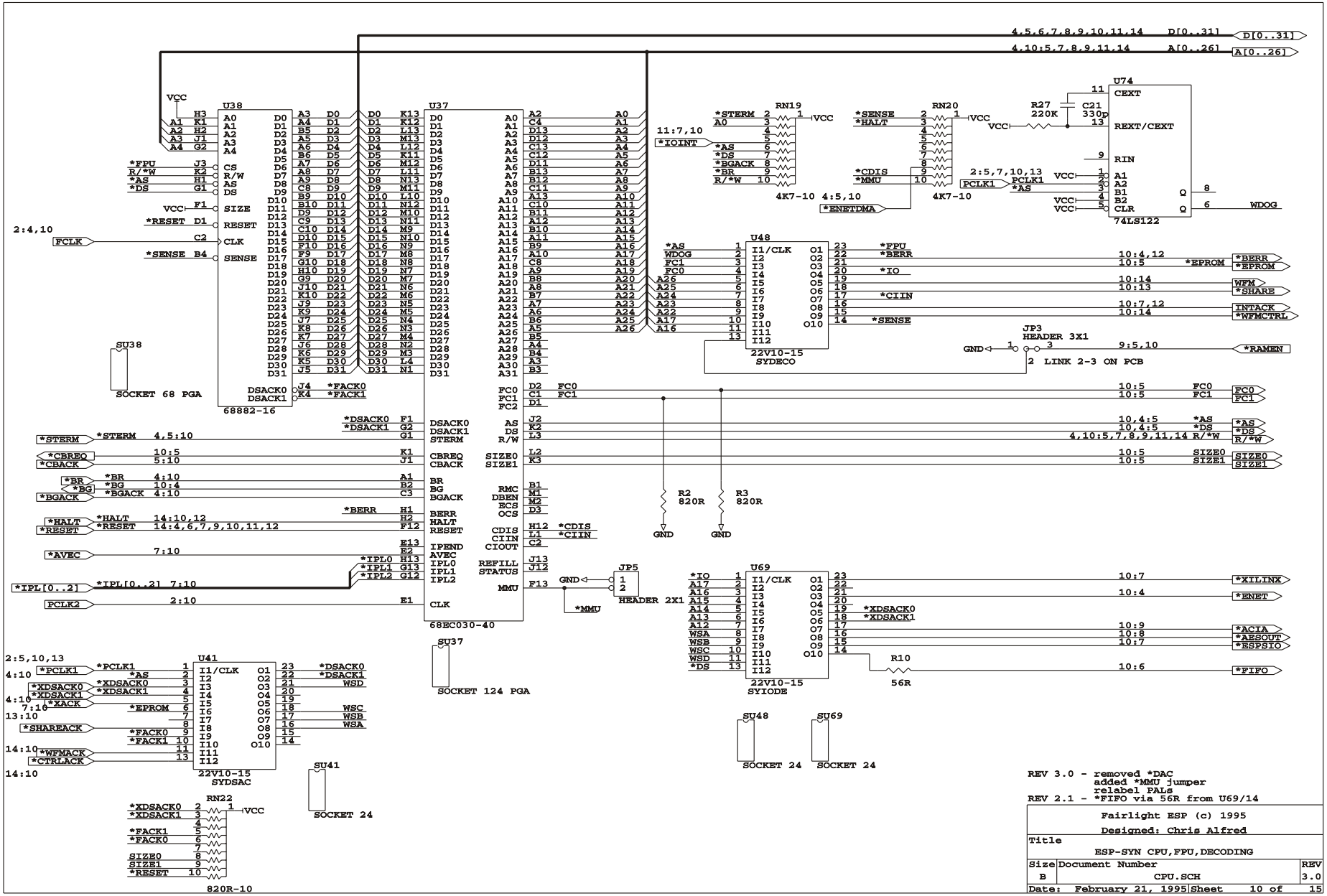

D[0..31]
A[0..31]
U26
U27
U24
74ACT244
*RA
*CA
CA2
CA3
RN16D 33R-8
RN16C 33R-8
RN16B 33R-8
RN16A 33R-8
RN17D 33R-8
RN17C 33R-8
RN17B 33R-8
RN17A 33R-8
RN15C 33R-8
RN15D 33R-8
MA0
MA1
MA2
MA3
MA4
MA5
MA6
MA7
MA8
MA9
MA[0..9]
U9
U10
U7
U8
U5
U6
U3
U4
441024Z-70
*RAS
*LLCAS
*LMCAS
*HMCAS
*MWR
RAS D0
CAS D1
WE D2
OE D3
GND
KMON30 V9.05
U34
27C512-150 OR 27C010
(1600000)
SU34
SOCKET 32
*EPROM
10:5
U25A
U25B
74ACT74
PCLK1
2:5,7,10,13
*RAS
*CA
*RA
U30
22V10-15
SYSIZE
*PCLK2
SIZE0
SIZE1
*ACAS
*RCYC
*CBREQ
*CBACK
*CALOAD
R/*W
*CAINC
REF
RCYC
WREF
12:5,6,13
RN18A 56R-8
RN18B 56R-8
RN18C 56R-8
RN18D 56R-8
*LLCAS
*LMCAS
*HMCAS
*HHCAS
UD
LD
5:14
U31
22V10-15
SYDRAM
(1800000)
2:5
*AS
*ENETDMA
FC1
FC0
*RAMEN
4:5
10:4,5
10:5
4,10:5,7,8,9,11
9:5,10
A26
A25
A24
A23
RN15A 33R-8
RN15B 33R-8
*MWR
*RAS
*CBACK
*STERM
5:10
5:4,10
*CBREQ
SU30
SU31
SOCKET 24
REV 3.0 - U34 27C512 (28pin) only
rename PALs
REV 2.3 - KMON30 v9.05 ROM
Fairlight ESP (c) 1995
Designed: Chris Alfred
Title
ESP-SYN EPROM AND DRAM
Size B
Document Number MEM.SCH
REV 3.0
Date: February 14, 1995
Sheet 5 of 15

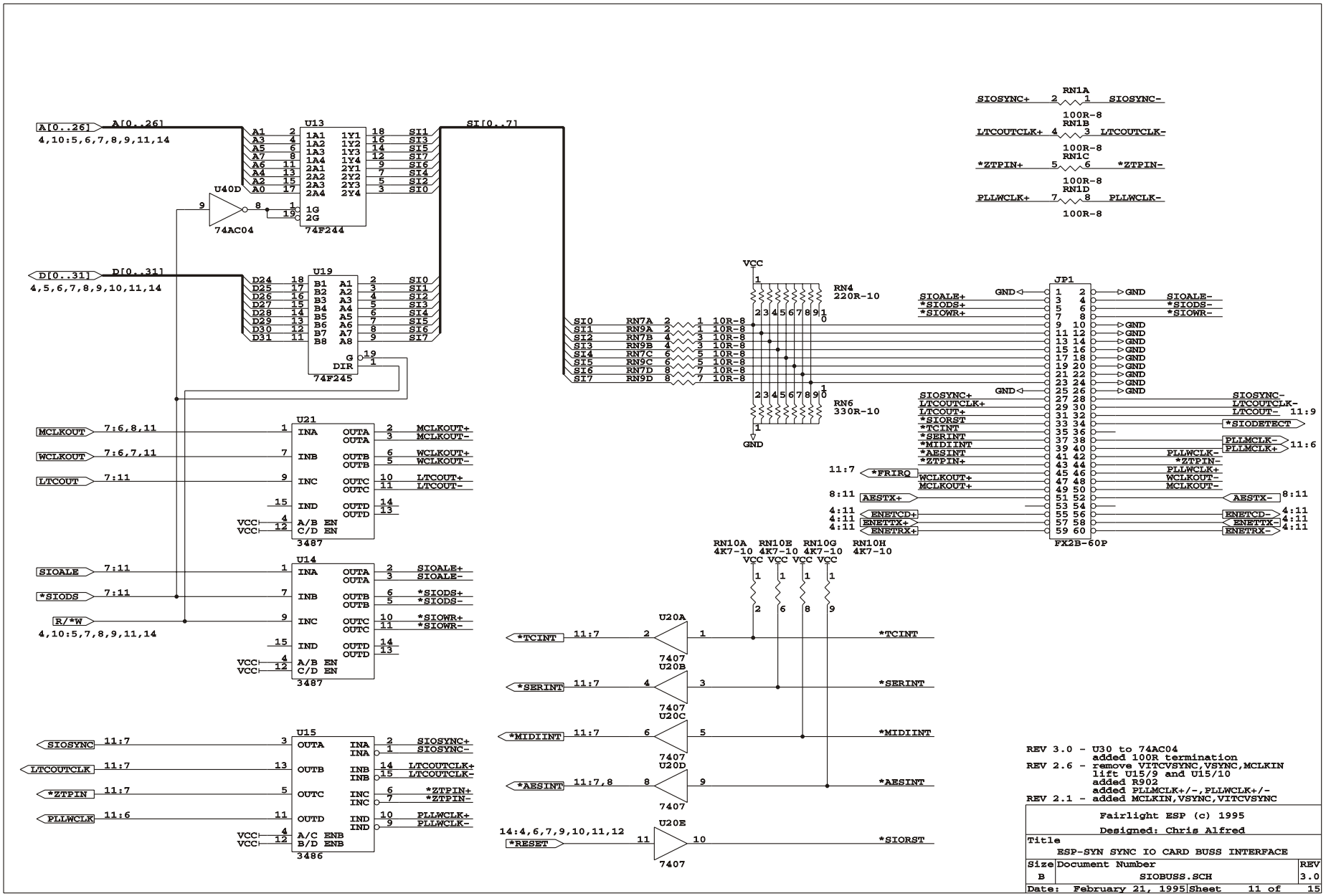

TIME SLICE BUSS CONNECTOR
CN2
EC17X2K6
M256+
MWORD+
TXD+
RXD+
M256-
MWORD-
TXD-
RXD-
D1 VCC
1N4001
JP2
HEADER 2X1
TERMINATION
LINK ON PCB
C1
10u 16V TANT
C3
100n
C2
100p
GND
VTERM
(12)
RN2
220R-10
RN5
330R-10
R17
4K7
VCC
R1
10R
U40F
74AC04
U40B
74AC04
U11C
74F125
U18
74F373
RN11A2
RN11B4
RN11C6
RN11D8
RN8C
RN8B
RN8A
10R-8
RN3B
RN3C
RN3D
RN3A
100R-8
*FIFOEMPTY
U23
CY7C421-30
(1001000)
D[0..31]
*FIFO
*RESET
*FIFORD
*TDEN
TDCLK
*SLOT
TSBEN
CCLNT
WRRF
TXD = TRANSMITT TO ESP-DIO CARD
R29
47K
R30
47K
U17
3487
U12
3486
PLLMCLK
PLLMCLK+
PLLMCLK-
DIOTX
DIORX
TSBCLKEN
DIOTXEN
TSBMCLK
REV 3.0 - added 100R termination
remove GND from U17/15
REV 2.6 - added PLLMCLK,PLLMCLK
REV 2.1 - *TSBEN driven by 74F125 and
terminated
C1 changed to 10uF
Fairlight ESP (c) 1995
Designed: Chris Alfred
Title
ESP-SYN TIME-SLICE-BUSS INTERFACE
Size
B
Document Number
TSB.SCH
REV
3 0
Date: February 21, 1995
Sheet
6 of
15


Fairlight ESP (c) 1995
Designed: Chris Alfred
Title ESP-SYN XILINX
Size B | Document Number XILINX.SCH | REV 3.0
Date: February 21, 1995 | Sheet 7 of 15
REV 3.0 - no 8M192,11M2783,11M2896,12M288
remove VCOUT, add XTAL MODULE
REV 2.7 - added A11,A12,A13 PIN
REV 2.1 - *SLOT,MCLKIN,VSYNC.VITCVSYNC
U29
XC3042PC84
(1000000)
SOCKET 84 PLCC
SU29
12M288 MODULE
X2
U32
74HCT245
RN12 4K7-10
RN14 4K7-10
RN10D 4K7-10
RN10F 4K7-10
D[0..31]
A[0..26]
*TPL[0..21]
*RESET
*XILINXPROG
LTCOUTCLK
*XILINXINIT
XILINXCLK
XILINXDATA
*FRIRQ
CCINT
*XACK
*IOINT
*TCINT
*TPI
*ESPSIO
(1006000)
*SBRINT
*MIDIINT
*AESINT
INTACK
*AVEC
LTCOUT
TSBWCLK
WCLKOUT
BCLKOUT
MCLKOUT
*VSYNC
SIOSYNC
*FIFOEMPTY
HDCLK
TSBEN
TSDEN
*ZTPIN
*SLOT
STOADE
*STOPS
*XILINX
R/*W
PCLK1
TSBMCLK


Fairlight ESP (c) 1995
Designed: Chris Alfred
Title
ESP-SYN AES OUTPUT
Size Document Number REV
B AESOUT.SCH 3 0
Date: February 8, 1995 Sheet 8 of 15
U68
CS8401
(1005000)
MCLKOUT
MCLKOUT
MCLKOUT
BOMOUT
*AESINT
*AESOUT
R/W
A[0..26]
D[0..31]
MCK
FSYNC
SCK
SDATA
INT
CS
R/W
A0
A1
A2
A3
A4
TXP
TXN
D0
D1
D2
D3
D4
D5
D6
D7
D24
D25
D26
D27
D28
D29
D30
D31
GND
AESTX+
AESTX-


REV 3.0 - added RS232 interface
REV 2.7 - added *XDSACK0
remove V+DET,V-DET,VCCDET
REV 2.1 - connect U28/41 to Vcc
Fairlight ESP (c) 1995
Dseigned: Chris Alfred
Title
ESP-SYN ACIA AND CONTROL PORT
Size Document Number REV
B ACIA.SCH 3.0
Date: February 21, 1995 Sheet 9 of 15
TIMER USED FOR REAL TIME CLOCK
SOCKET 44 PLCC
PLACE NEAR JP1
JP4 HEADER 3X1
U35 MAX232
U28 68681FN (1004000)
U43F 7407
Y1 3M6864


U38
68882-16
U37
68EC030-40
U74
74LS122
U48
22V10-15
SYDECO
U69
22V10-15
SYIODE
U41
22V10-15
SYDSAC
RN19
RN20
RN22
820R-10
4K7-10
JP3
HEADER 3X1
JP5
HEADER 2X1
R2
820R
R3
820R
R10
56R
SU38
SOCKET 68 PGA
SU37
SOCKET 124 PGA
SU41
SOCKET 24
SU48
SOCKET 24
SU69
SOCKET 24
2 LINK 2-3 ON PCB
REV 3.0 - removed *DAC
added *MMU jumper
relabel PALs
REV 2.1 - *FIFO via 56R from U69/14
Fairlight ESP (c) 1995
Designed: Chris Alfred
Title
ESP-SYN CPU,FPU,DECODING
Size B
Document Number CPU.SCH
REV 3.0
Date: February 21, 1995
Sheet 10 of 15



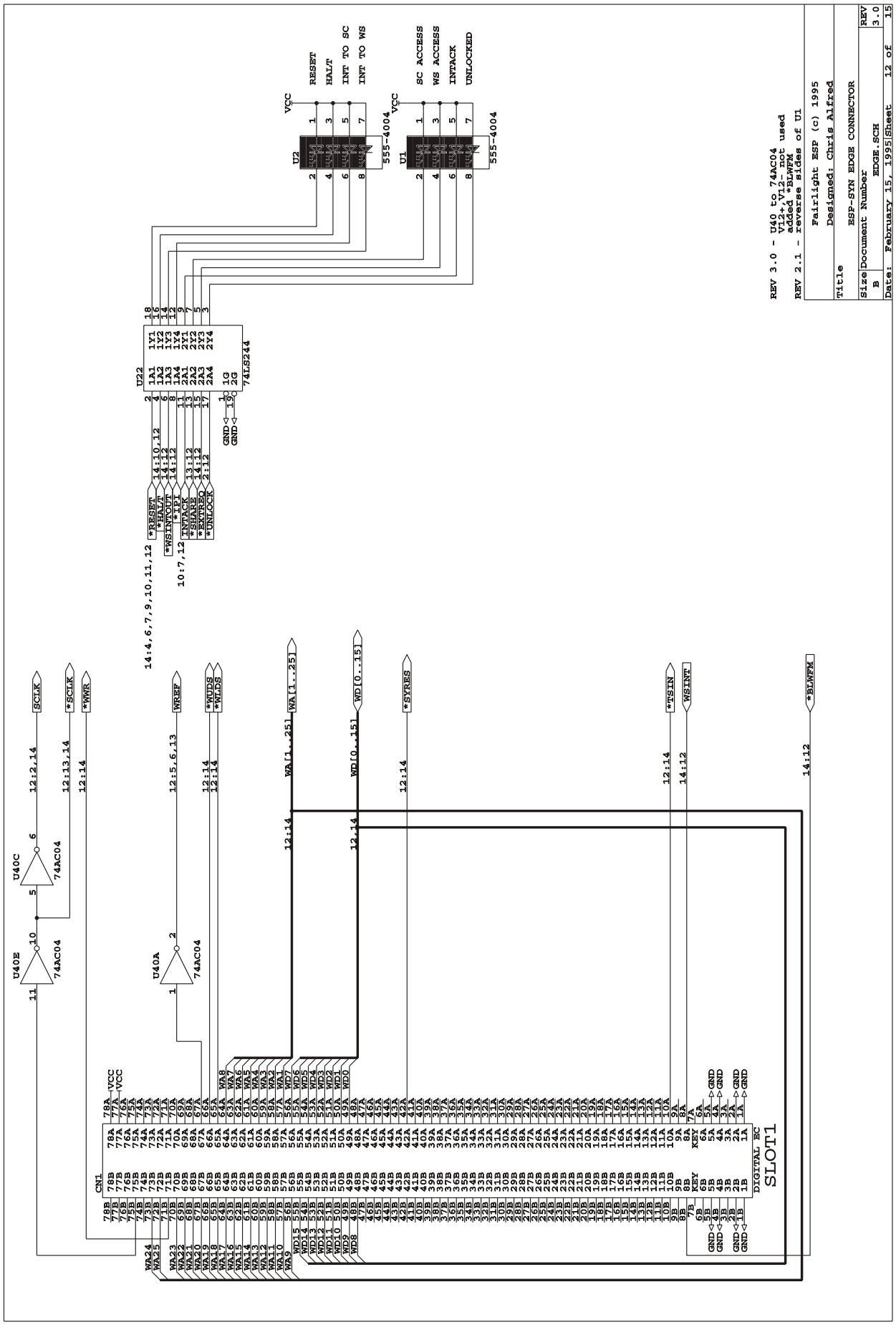
REV 3.0 - U30 to 74AC04
added 100R termination
REV 2.6 - remove VITCVSYNC,VSYNC,MCLKIN
lift U15/9 and U15/10
added R902
added PLLMCLK+/-,PLLWCLK+/-
REV 2.1 - added MCLKIN,VSYNC,VITCVSYNC

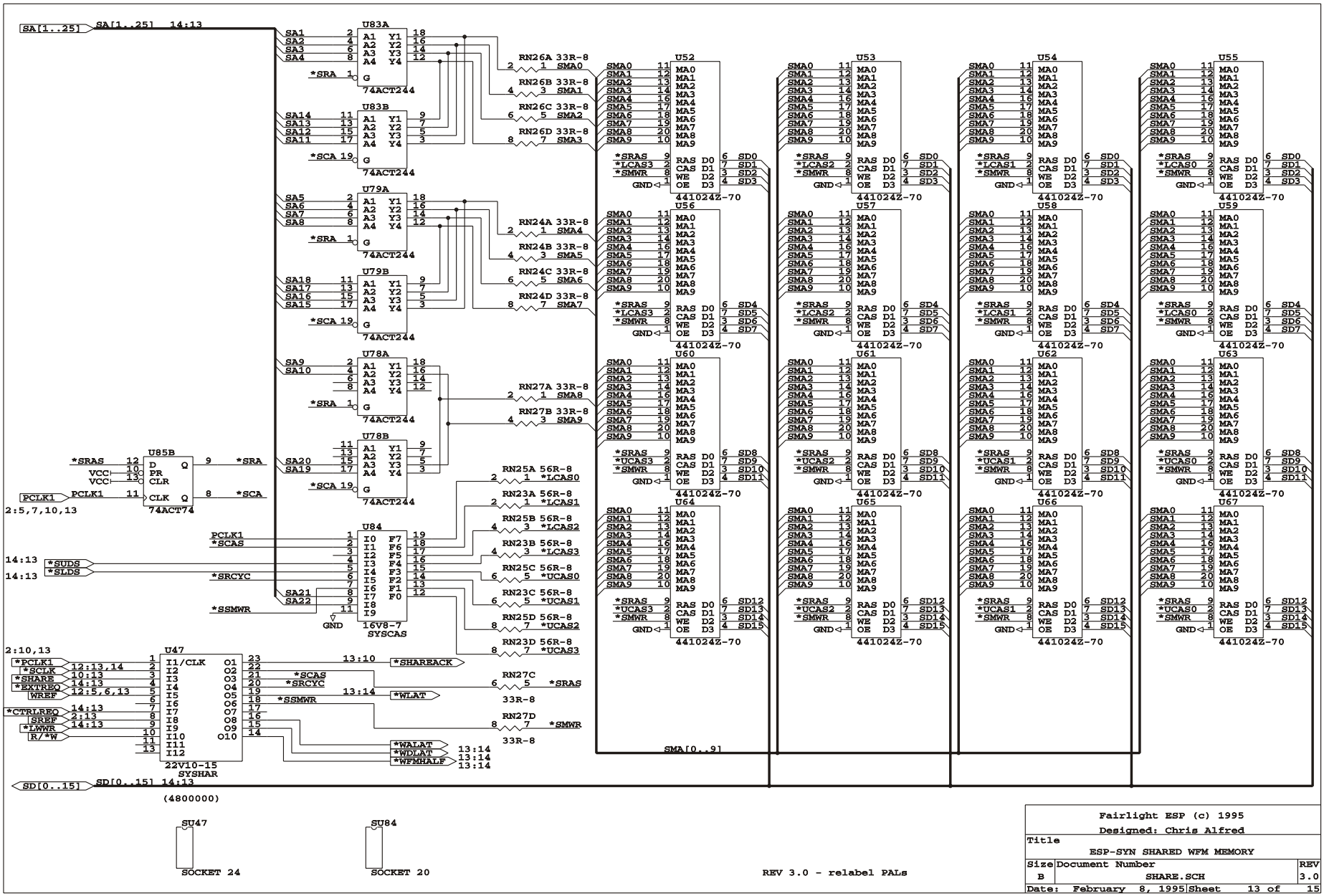
Fairlight ESP (c) 1995

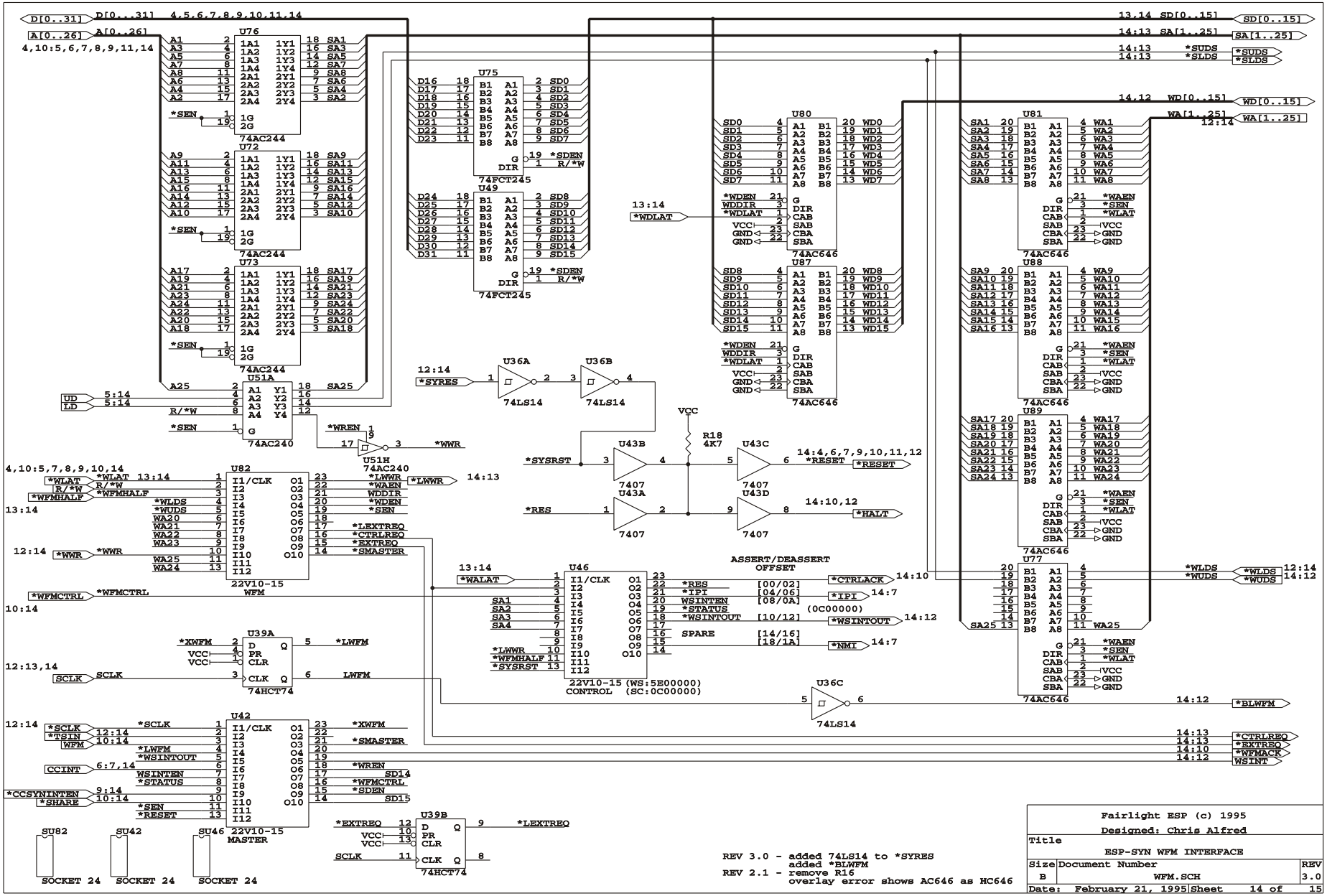
Designed: Chris Alfred

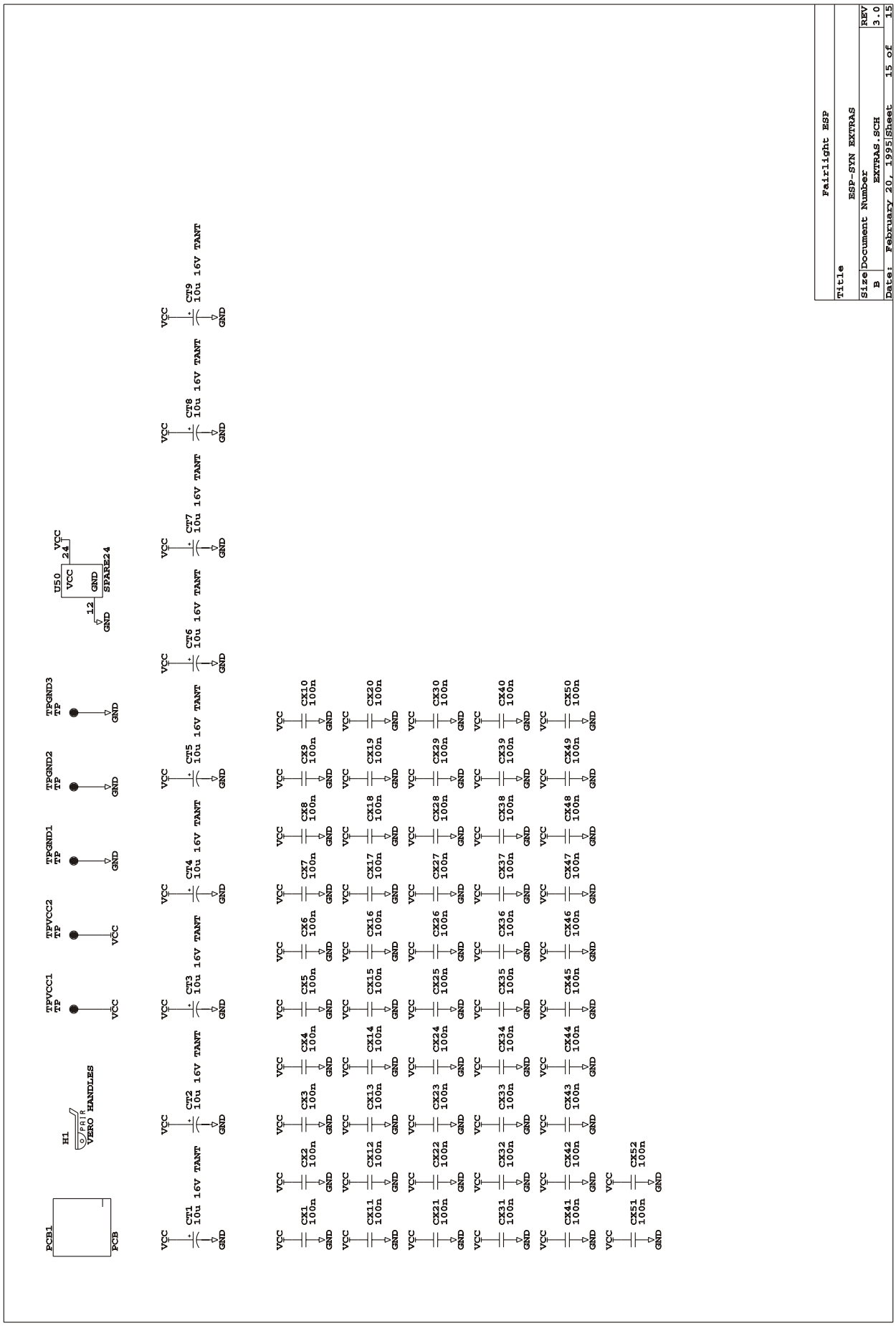
Title: ESP-SYN SYNC IO CARD BUSS INTERFACE

Size	Document Number	REV
B	SIOBUSS.SCH	3.0
Date: February 21, 1995	Sheet 11 of 15	

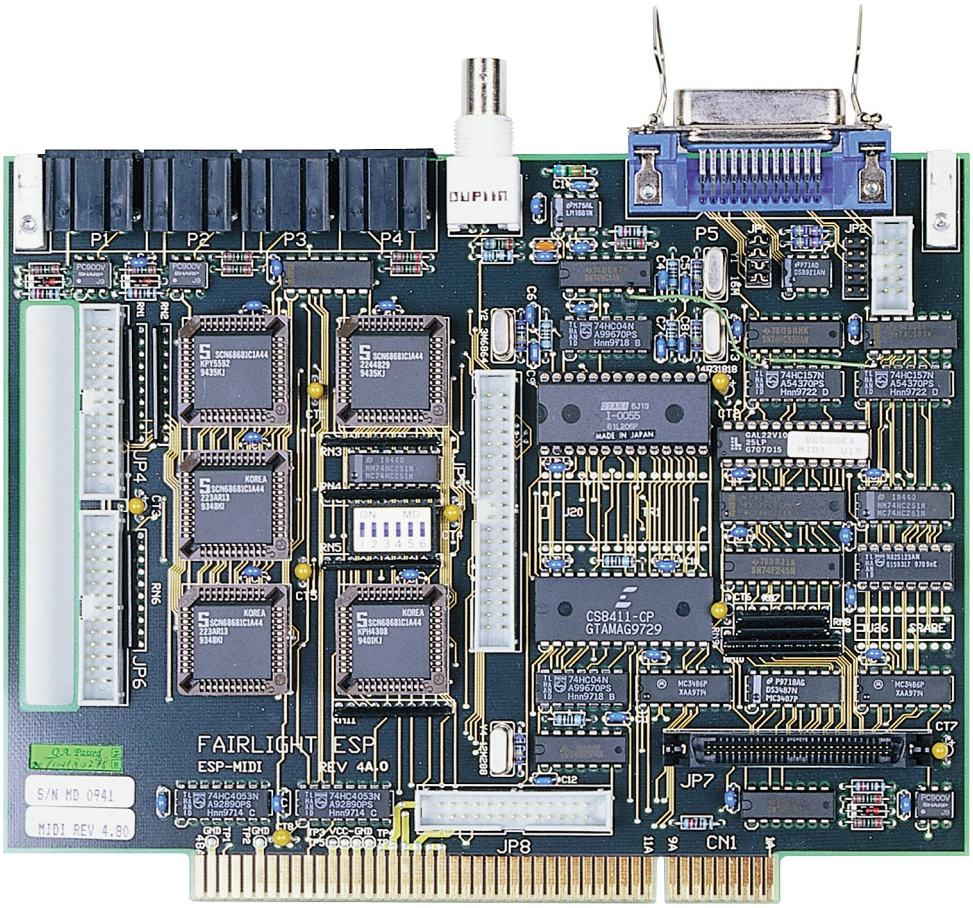

REV 3.0 - U40 to 74AC04
V12+,V12- not used
added *BLWFM
REV 2.1 - reverse sides of U1
Fairlight ESP (c) 1995
Designed: Chris Alfred
Title
ESP-SYN EDGE CONNECTOR
Size
B
Document Number
EDGE.SCH
REV
3.0
Date: February 15, 1995
Sheet 12 of 15
U40E
U40A
U40C
74AC04
SCLK
*SCLK
*WWR
WREF
*WUDS
*WLDS
WA[1..25]
WD[0..15]
*STRES
*TSIN
WSINT
*BLWFM
U22
74LS244
*RESET
*HALT
*WSINTOUT
*WLOCK
*SHARE
*EXTREQ
*UNLOCK
U2
U1
555-4004
VCC
RESET
HALT
INT TO SC
INT TO WS
SC ACCESS
WS ACCESS
INTACK
UNLOCKED
CN1
SLOT1
DIGITAL EC
KEY


SA[1..25]
SA[1..25] 14:13
U83A
U83B
U79A
U79B
U78A
U78B
74ACT244
RN26A 33R-8
RN26B 33R-8
RN26C 33R-8
RN26D 33R-8
RN24A 33R-8
RN24B 33R-8
RN24C 33R-8
RN24D 33R-8
RN27A 33R-8
RN27B 33R-8
U52
U53
U54
U55
U56
U57
U58
U59
U60
U61
U62
U63
U64
U65
U66
U67
441024Z-70
SMA[0..9]
U85B
74ACT74
PCLK1
2:5,7,10,13
U84
16V8-7
SYSCAS
RN25A 56R-8
RN23A 56R-8
RN25B 56R-8
RN23B 56R-8
RN25C 56R-8
RN23C 56R-8
RN25D 56R-8
RN23D 56R-8
U47
22V10-15
SYSHAR
2:10,13
RN27C
RN27D
33R-8
SD[0..15]
SD[0..15] 14:13
(4800000)
SU47
SOCKET 24
SU84
SOCKET 20
REV 3.0 - relabel PALs
Fairlight ESP (c) 1995
Designed: Chris Alfred
Title
ESP-SYN SHARED WFM MEMORY
Size B
Document Number SHARE.SCH
REV 3.0
Date: February 8, 1995
Sheet 13 of 15

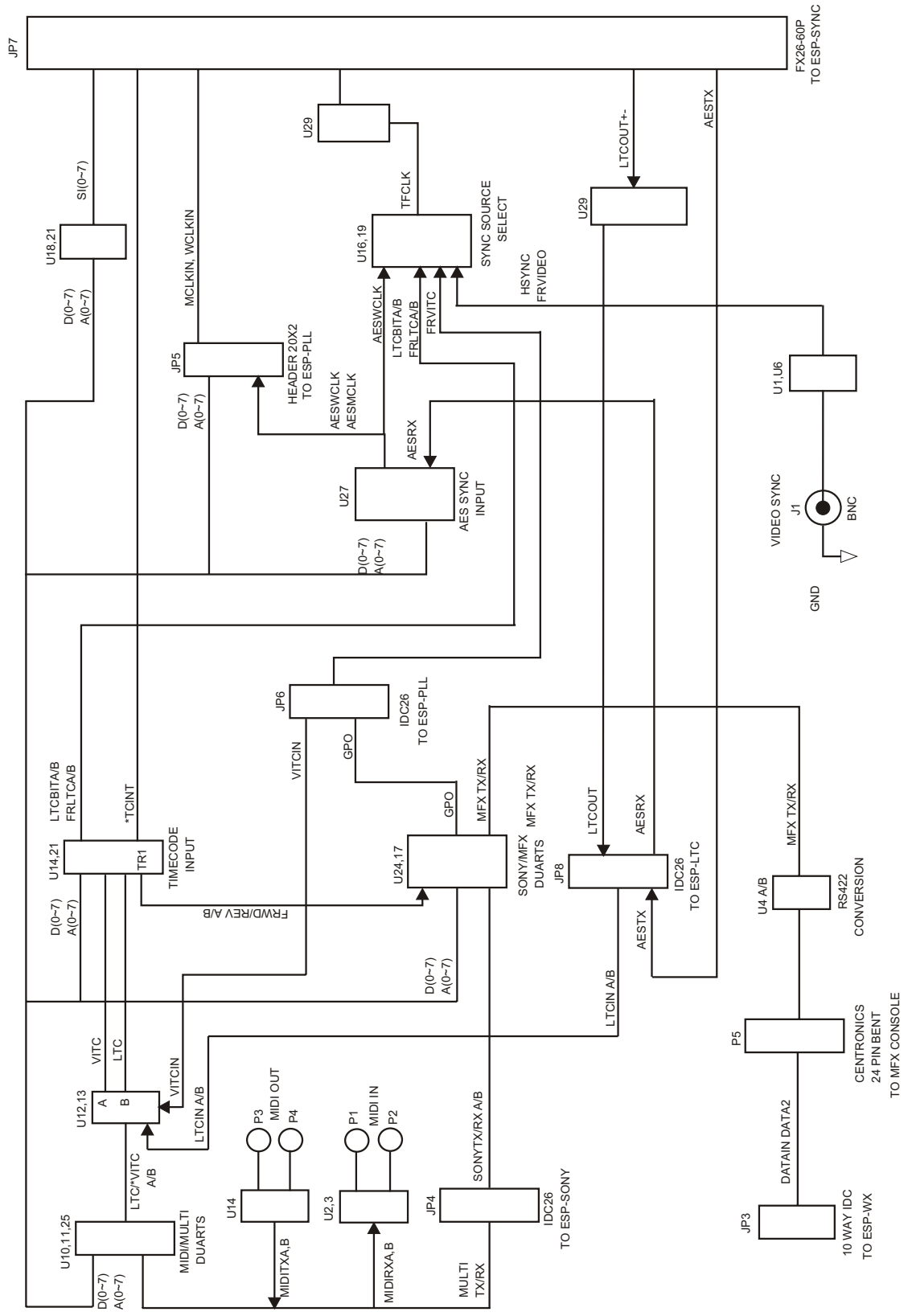

U76
U72
U73
U75
U49
U80
U87
U81
U88
U89
U77
U51A
U36A
U36B
U43A
U43B
U43C
U43D
U82
U46
U42
U39A
U39B
U36C
U51H
74AC244
74AC240
74FCT245
74AC646
74LS14
74HCT74
7407
22V10-15
R18 4K7
VCC
Fairlight ESP (c) 1995
Designed: Chris Alfred
Title
ESP-SYN WFM INTERFACE
Size B
Document Number WFM.SCH
REV 3.0
Date: February 21, 1995
Sheet 14 of 15
REV 3.0 - added 74LS14 to *SYRES
added *BLWFM
REV 2.1 - remove R16
overlay error shows AC646 as HC646
SU82 SOCKET 24
SU42 SOCKET 24
SU46 SOCKET 24


Fairlight ESP
Title
ESP-SYN EXTRAS
Size
B
Document Number
EXTRAS.SCH
REV
3.0
Date: February 20, 1995
Sheet
15 of
15
PCB1
PCB
H1
O/PAIR
VERO HANDLES
TPVCC1
TPVCC2
TPGND1
TPGND2
TPGND3
U50
VCC
GND
SPARE24
CT1 10u 16V TANT
CT2 10u 16V TANT
CT3 10u 16V TANT
CT4 10u 16V TANT
CT5 10u 16V TANT
CT6 10u 16V TANT
CT7 10u 16V TANT
CT8 10u 16V TANT
CT9 10u 16V TANT
CX1 100n
CX2 100n
CX3 100n
CX4 100n
CX5 100n
CX6 100n
CX7 100n
CX8 100n
CX9 100n
CX10 100n
CX11 100n
CX12 100n
CX13 100n
CX14 100n
CX15 100n
CX16 100n
CX17 100n
CX18 100n
CX19 100n
CX20 100n
CX21 100n
CX22 100n
CX23 100n
CX24 100n
CX25 100n
CX26 100n
CX27 100n
CX28 100n
CX29 100n
CX30 100n
CX31 100n
CX32 100n
CX33 100n
CX34 100n
CX35 100n
CX36 100n
CX37 100n
CX38 100n
CX39 100n
CX40 100n
CX41 100n
CX42 100n
CX43 100n
CX44 100n
CX45 100n
CX46 100n
CX47 100n
CX48 100n
CX49 100n
CX50 100n
CX51 100n
CX52 100n

18.0 ESPMIDI MIDI I/O Card



18.1 ESPMIDI Block Diagram



18.2 ESPMIDI Diagnostics

18.2.1 Running Diagnostics

System must have an ESP-SYN Sync Card and cable connecting it to the ESP-MIDI Card.

Type:	osk30	enters OSK30 operating system
	scdiag	start Sync Card diagnostics
		(should get SC> prompt)

18.2.2 MIDI ports

(1) Setup: Connect MIDI OUT A to MIDI IN A

Connect MIDI OUT B to MIDI IN B

Type: m

If successful, the display should show:

	MIDI OUT		MIDI IN	
Send	A	B	A	B
___	___	___	___	___
xx	pass	pass	pass	pass

The xx digits should be incrementing and show the current value

transmitted by each MIDI OUT port.

(2) Press q to exit diagnostic.

MIDI Generation

The diagnostic transmits the value in the Send field via the duarts at U25 (for ports A,B). The data output rate generated from the MIDICLK (500kHz) signal which is divided by 16 in the duarts to produce the MIDI baud rate of 31.25KHz. Midi data is transmitted and received as 8 bits, 1 stop bit and no parity.

As the Midi Processor (CMI28) can also use the MIDI output ports, the MOUTSELA..B signals are set low during the diagnostic so the Sync Card is driving the output.

MIDI Receivers

MIDI received at the input ports are optically isolated by U1 to U4 (all PC900). The TTL outputs MIDIRXA..B are fed to the receive lines of duart U25 (68681) for the Sync Card.

Diagnostic Description

The possible status values displayed by the diagnostic are:

pass	Current test value was sent/received correctly.
fail	Current test value was not sent or a different value was received.
....	No value has been received by the port.
I:nn	Extra interrupt received with byte nn.
L:nn	Lost interrupt, received byte was nn.
[nn]	Incorrect value received.

The diagnostic transmits the value in the Send field by enabling transmitter interrupts from the duarts (*MIDIINT). As all duarts should be ready to transmit, the interrupt will be requested immediately by the assertion of *MIDIINT. The value to be sent will be written to the duarts and transmission begins. The diagnostic then waits for 20mS which is more than adequate time for the byte to be transmitted and received. The receiver interrupt is then enabled which will immediately request an interrupt via the assertion of *MIDIINT as the byte has been received by the duart. The diagnostic then checks the received value for transmission integrity.

18.2.3 Video Sync input

(1) Setup: connect video source to VIDEO SYNC.

Type: vs

(2) Press q to exit diagnostic.

If successful the screen should show (assuming PAL input)

/ FRAME: 25.000Hz HSYNC:15625.000Hz

Note that these values may vary slightly depending on the accuaracy of the video reference and sync card 12.288MHz crystal.

Video Sync separation

The video signal fed into VIDEO SYNC is filtered by R1 (680R), C3 (470pF) and C2 (100nF) to remove any video signal and colour burst signal. This filtered signal is fed into the LM1881 (U5) sync separator chip to produce FRVIDEO and HSYNC.

Diagnostic Description

The diagnostic controls SYNCSEL0..3 to select the appropriate video signal to detect via U17,U16 (74HC251) to be fed as SIOSYNC to the sync card XILINX. Software writes a prescale value of 5 to the XILINX to divide SIOSYNC to a reasonable frequency. Once divided, the XILINX will generate an interrupt at level 6. Between these interrupts, the period is counted by using the 12.288MHz crystal as a reference to determine the input frequency.

18.2.4 DIP SWITCHES

(1) Setup: None

Type: d

(2) Change each dip switch (S1) and check display shows state.

(3) Press q to exit.

Diagnostic Description

The diagnostic reads the status of the DIP switches via the 68681 duart at U24. Data read shows - (minus sign) when ON and _ (underscore) when OFF.

5. Bipolar Prom

(1) Setup: None

Type: bp

The diagnostics will display the contents of the bipolar PROM at U22 (82S123 32 bytes). If the PROM is empty, all data should be zero.

6. MFX RS422 Interface

(1) Setup: Install loopback connector between MFX cable and main frame. All connections are straight-thru except loop pins 5-6 and 17-18 at main frame end.

(2) Type: mfx

If successful, the display will show:

Send	OUT	IN
——	———	———
nn	Pass	Pass

(3) Press q to exit diagnostic.

MFX RS422 Transmit

The diagnostic transmits the value in the Send field via the duarts at U18 (port A). The data output rate generated from the duart crystal clock ACIACLK (3.6864MHz) signal which is divided by the duart to produce the RS422 baudrate of 38.4KHz. Data is transmitted as MFXOUT and received as MFXRXD 8 bits 1 stop bit and odd parity. The duart data is converted to RS422 format by U35 (8921).

MFX RS422 Receive.

Data received is converted from RS422 by U35 (8921) and fed into the duart at U18 as MFXRX.

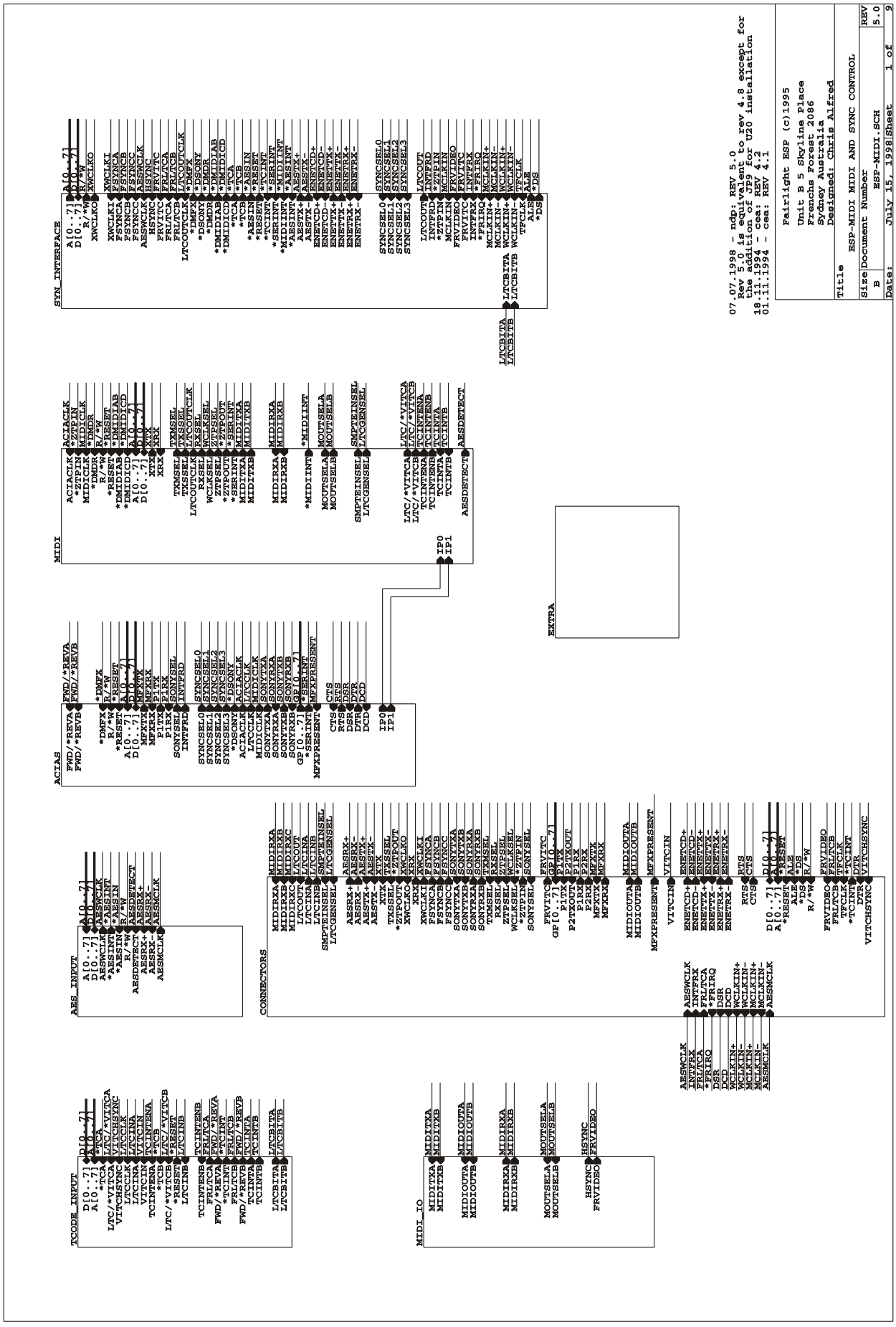
Diagnostic Description

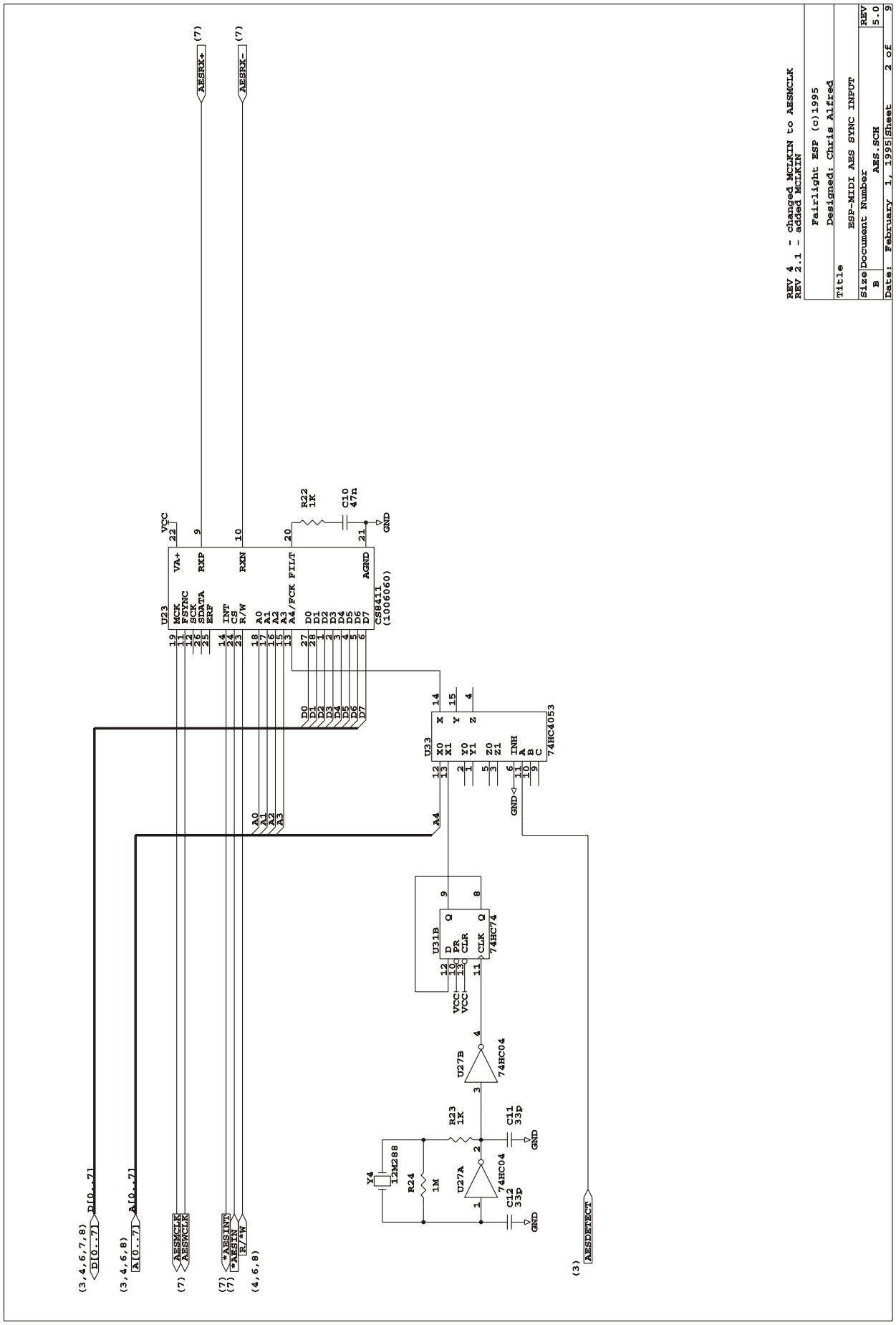
The possible status values displayed by the diagnostic are:

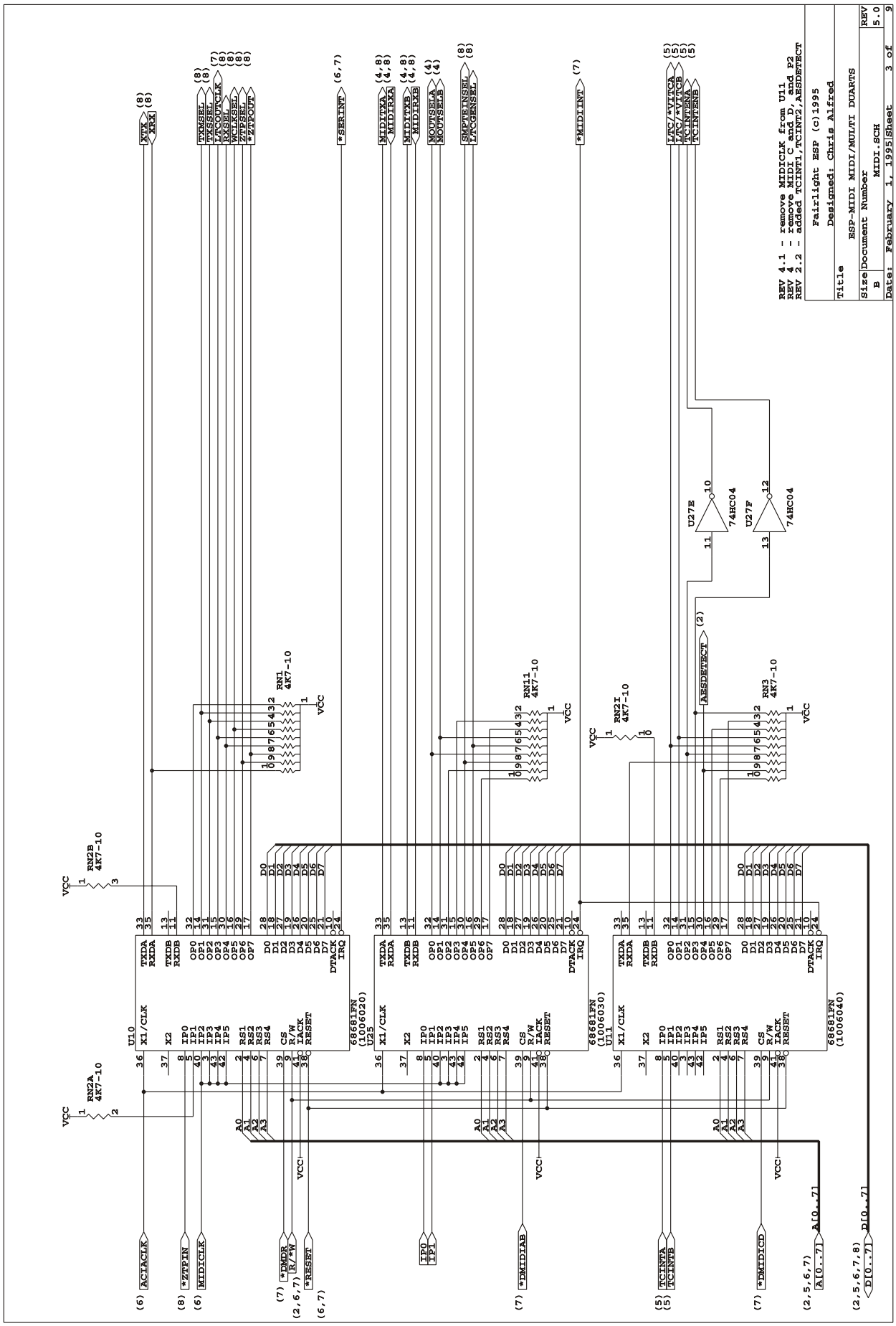
pass	Current test value was sent/received correctly.
fail	Current test value was not sent or a different value was received.
....	No value has been received by the port.
I:nn	Extra interrupt, received byte nn.
L:nn	Lost interrupt, received byte nn.
[nn]	Incorrect value received.

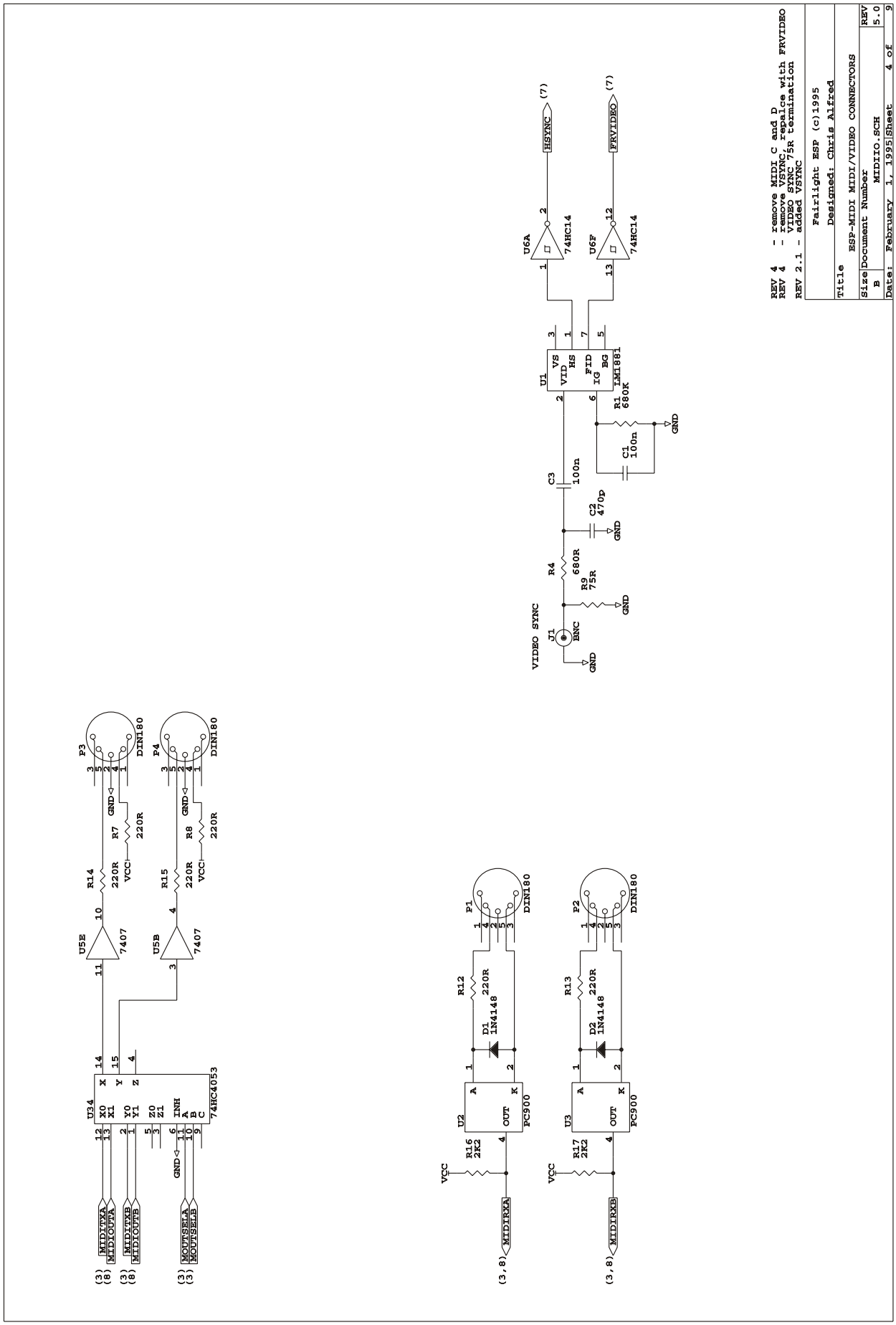
The diagnostic transmits the value in the Send field by enabling transmitter interrupts from the duart (*SERINT). As the duart should be ready to transmit, the interrupt will be requested immediately by the assertion of *SERINT. The value to be sent will be written to the duart and transmission begins. The diagnostic then waits for 20mS which is more than adequate time for the byte to be transmitted and received. The receiver interrupt is then enabled which will immediately request an interrupt via the assertion of *SERINT as the byte has been received by the duart. The diagnostic then checks the received value for transmission integrity.

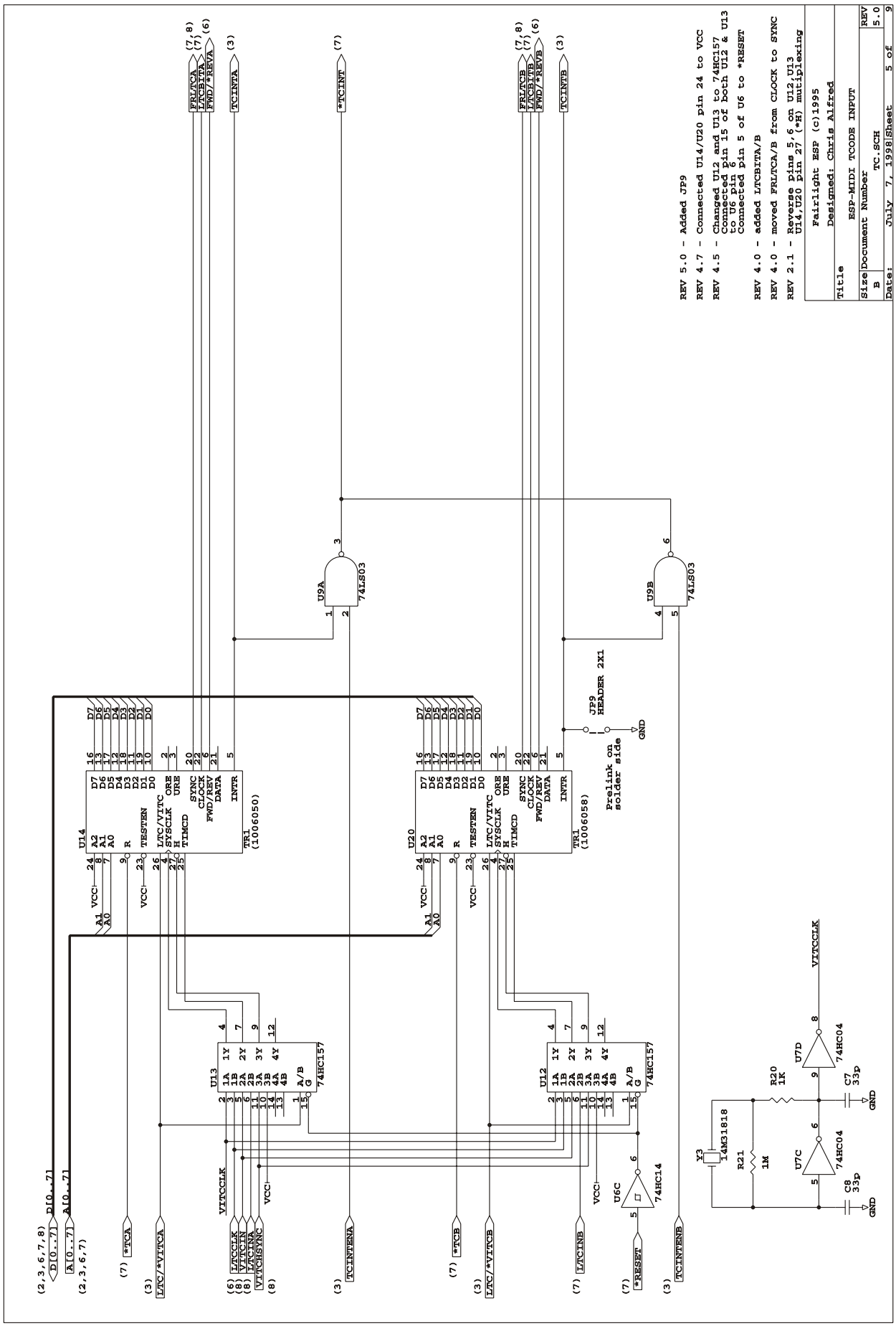
18.3 ESPMIDI SCHEMATICS

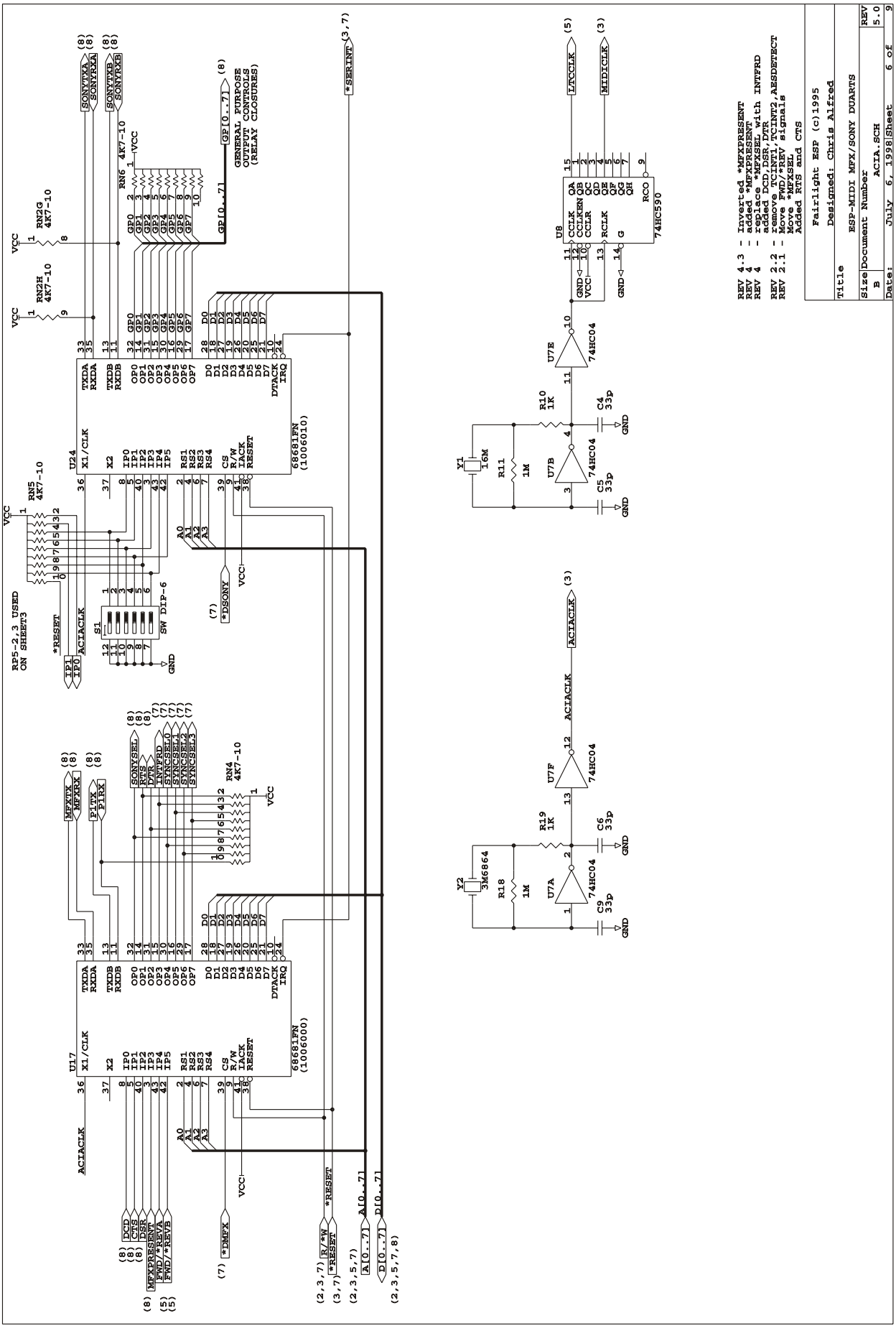


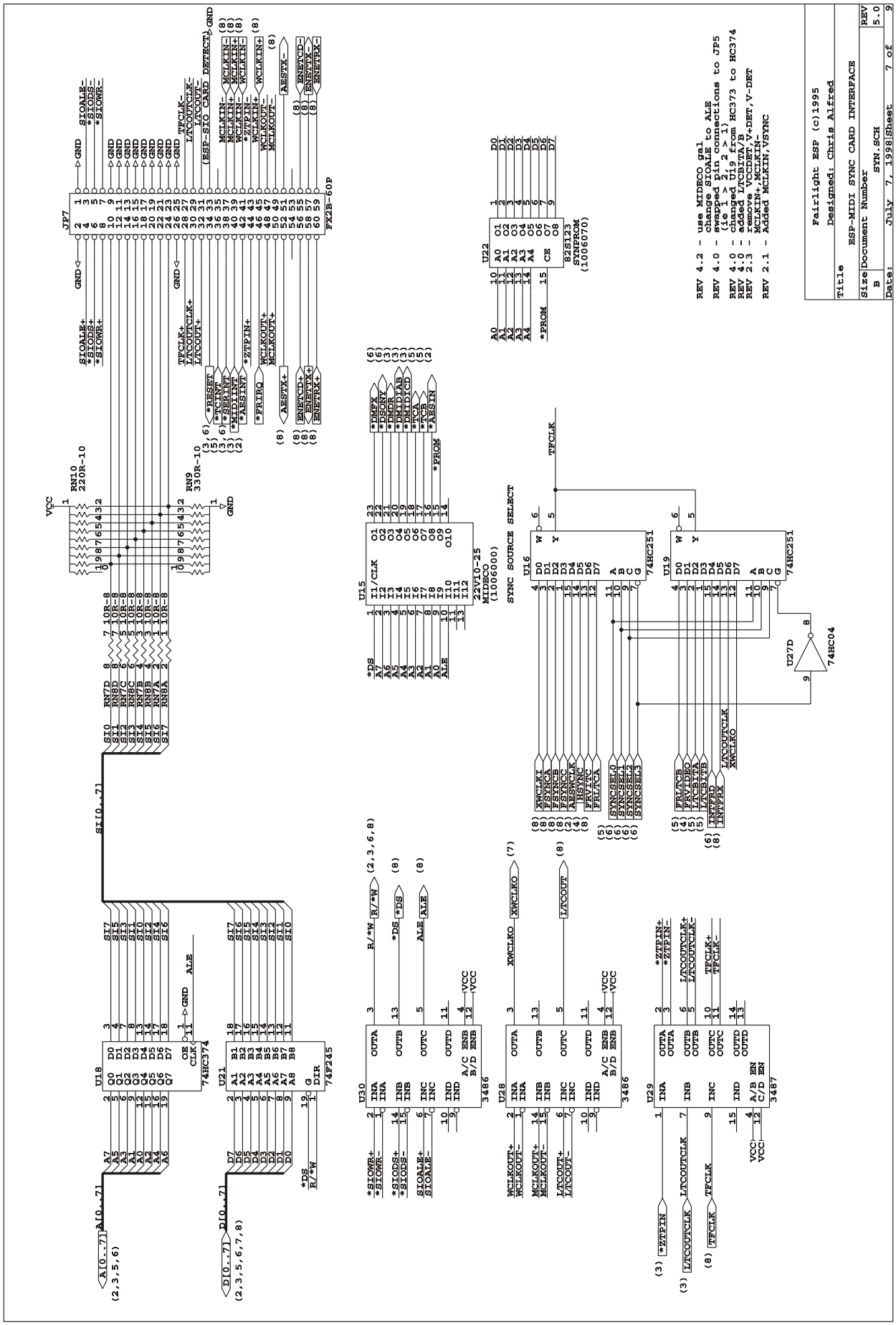

REV 4 - changed MCLKIN to AESMCLK
REV 2.1 - added MCLKIN
Fairlight ESP (c)1995
Designed: Chris Alfred
Title ESP-MIDI AES SYNC INPUT
Size B Document Number AES.SCH REV 5.0
Date: February 1, 1995 Sheet 2 of 9
U23 CS8411 (1006060)
MCK RSYNC SCK SDATA ERF INT CS R/W A0 A1 A2 A3 A4/FCK D0 D1 D2 D3 D4 D5 D6 D7 VA+ RXP RXN FILT AGND
VCC
GND
R22 1K
C10 47n
AESRX+
AESRX-
U33 74HC4053
U31B 74HC74
U27A U27B 74HC04
R23 1K
R24 1M
C11 33p
C12 33p
Y4 12M288
D[0..7]
A[0..7]
AESMCLK
AESWCLK
*AESINT
*AESCS
R/*W
AESDETECT

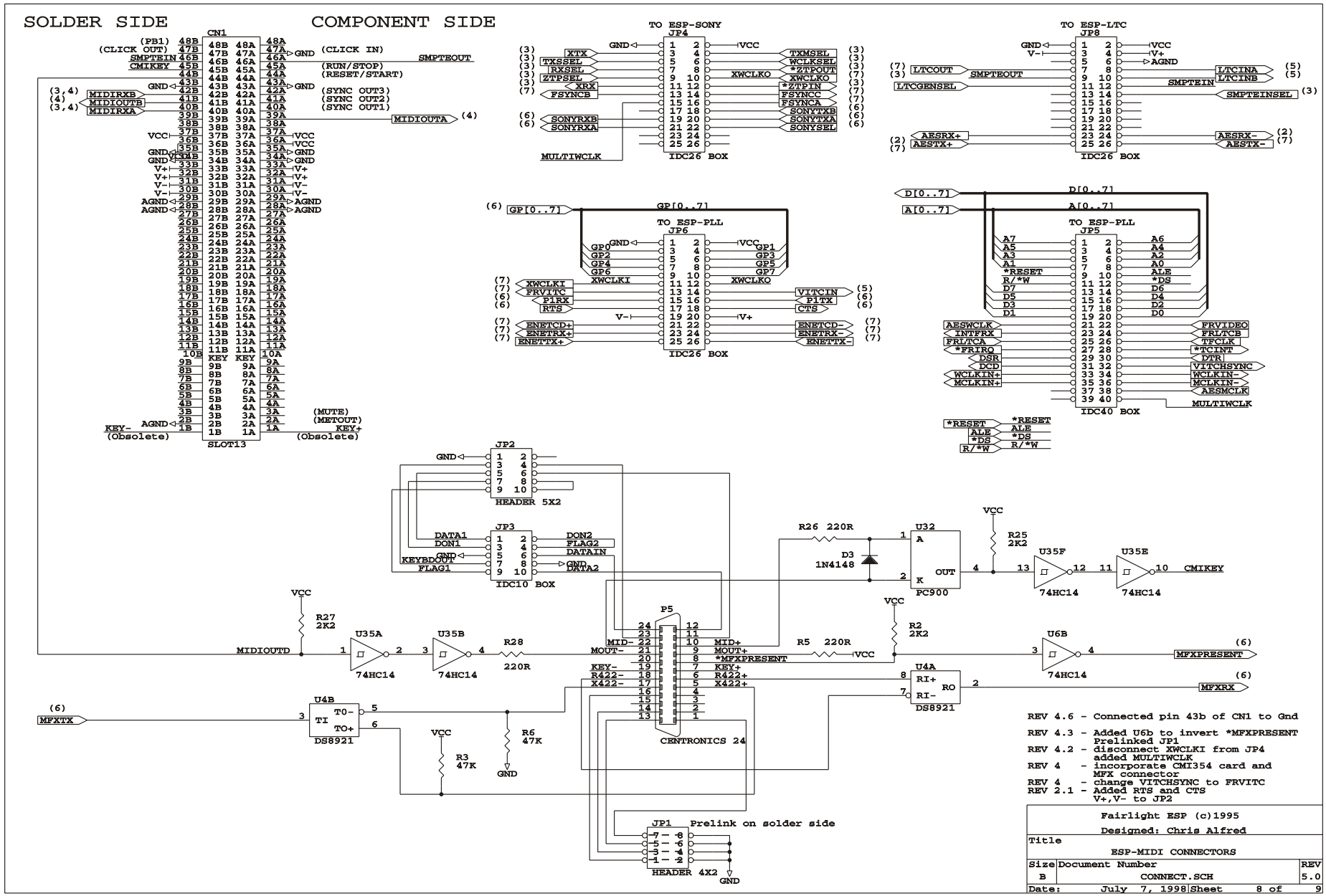

REV 4.1 - remove MIDICLK from U11
REV 4.1 - remove MIDI_and_D_pad P2
REV 4.2 - added TCINT1,TCINT2,AESDETECT
Fairlight ESP (c)1995
Designed: Chris Alfred
Title
ESP-MIDI MIDI/MULTI DUARTS
Size
B
Document Number
MIDI.SCH
REV
5.0
Date: February 1, 1995
Sheet 3 of 9
RN2B 4K7-10
RN2A 4K7-10
RN1 4K7-10
RN11 4K7-10
RN2I 4K7-10
RN3 4K7-10
U27E
U27F
74HC04
68681FN (1006020)
68681FN (1006030)
68681FN (1006040)
U10
U25
U11
VCC
VCCI
ACFACLK
MIDICLK
*ZFPIN
*ZFPOUT
*SERINT
*MIDINT
*DMIDTAB
*DMIDICD
*DMDR
*RESET
AESDETECT
TCINTA
TCINTB
A[0..7]
D[0..7]


REV 4 - remove MIDI C and D
REV 4 - remove VSYNC, repalce with FRVIDEO
REV 2.1 - VIDEO SYNC 75R termination
REV 2.1 - added VSYNC
Fairlight ESP (c)1995
Designed: Chris Alfred
Title
ESP-MIDI MIDI/VIDEO CONNECTORS
Size Document Number REV
B MIDIIO.SCH 5.0
Date: February 1, 1995 Sheet 4 of 9
VIDEO SYNC
U1 VID VS HS FID IG BG IAM1881
U5A 74HC14
U5F 74HC14
HSYNC (7)
FRVIDEO (7)
R1 680K
R4 680R
R9 75R
C1 100n
C2 470p
C3 100n
J1 BNC
GND
VCC
U34 74HC4053
U5E 7407
U5B 7407
P1 P2 P3 P4 DIN180
R7 R8 R12 R13 R14 R15 220R
R15 2K2
R16 R17 2K2
D1 D2 1N4148
U2 U3 PC900
MIDITXA
MIDIOUTA
MIDITXB
MIDIOUTB
MOUTSELA
MOUTSELB
MIDIRXA
MIDIRXB
(3,8)
(3)


REV 5.0 - Added JP9
REV 4.7 - Connected U14/U20 pin 24 to VCC
REV 4.5 - Changed U12 and U13 to 74HC157
Connected pin 15 of both U12 & U13 to U6 pin 6
Connected pin 5 of U6 to *RESET
REV 4.0 - added LTCBITA/B
REV 4.0 - moved FRLTCA/B from CLOCK to SYNC
REV 2.1 - Reverse pins 5,6 on U12,U13
U14,U20 pin 27 (*H) mutiplexing
Fairlight ESP (c)1995
Designed: Chris Alfred
Title ESP-MIDI TCODE INPUT
Size B Document Number TC.SCH REV 5.0
Date: July 7, 1998 Sheet 5 of 9
U14 TR1 (1006050)
U20 TR1 (1006058)
U13 74HC157
U12 74HC157
U9A 74LS03
U9B 74LS03
U6C 74HC14
U7C 74HC04
U7D 74HC04
JP9 HEADER 2X1
Prelink on solder side
X3 14M31818
R20 1K
R21 1M
C7 33p
C8 33p
VCC
GND
*TCA
*TCB
*TCINT
*RESET
LTC/*VITCA
LTC/*VITCB
TCINTENA
TCINTENB
LACINB
LACCLK
VITCIN
LACINA
VITCHSYNC
VITCCLK
FRLTCA
LTCBITA
FWD/*REVA
TCINTA
FRLTCB
LTCBITB
FWD/*REVB
TCINTB
D[0..7]
A[0..7]

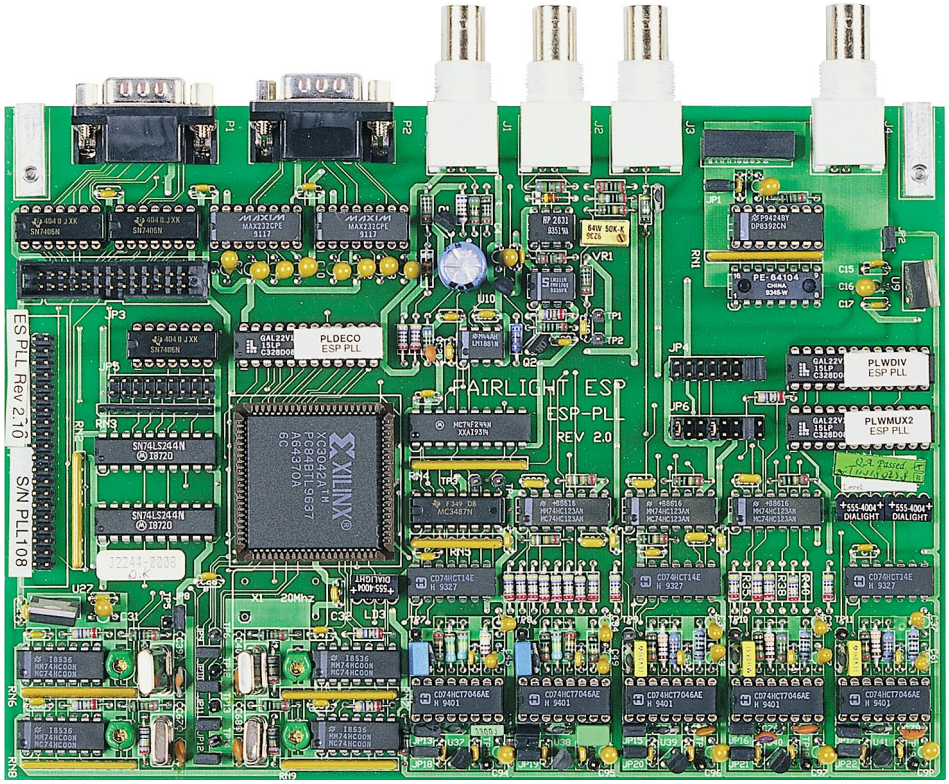

REV 4.3 - Inverted *MFXPRESENT
REV 4 - added *MFXPRESENT
REV 4 - added MIDI CLK with INTFRD
REV 2.2 - added DCD,DSR,DTR
REV 2.1 - remove TCINT1,TCINT2,ASSDETECT
Move FWD/*REV signals
Move *MFXSEL
Added RTS and CTS
Fairlight ESP (c)1995
Designed: Chris Alfred
Title
ESP-MIDI MFX/SONY DUARTS
Size B
Document Number
ACIA.SCH
REV 5.0
Date: July 6, 1998 Sheet 6 of 9
RP5-2,3 USED ON SHEET3
SW DIP-6
68681PN (10066010)
68681PN (10066000)
74HC04
74HC590
3M6864
16M
*RESET
ACIACLK
*SERINT
*DSONY
*DMFX
MFXTRX
P1TX
P1RX
SONYSEL
INTFRD
SYNCSEL0
SYNCSEL1
SYNCSEL2
SYNCSEL3
SONYTXA
SONYRXA
SONYTXB
SONYRXB
GP[0..7]
GENERAL PURPOSE OUTPUT CONTROLS (RELAY CLOSURES)
TACCLK
MIDICLK
DCD
CTS
DSR
MFXPRESENT
FWD/*REVA
FWD/*REVB
R/*W
A[0..7]
D[0..7]


Fairlight ESP (c)1995
Designed: Chris Alfred
Title
ESP-MIDI SYNC CARD INTERFACE
Size B
Document Number SYN.SCH
REV 5.0
Date: July 7, 1998 Sheet 7 of 9
REV 4.2 - use MIDECO gal
change SIOALE to ALE
REV 4.0 - swapped pin connections to JP5
(ie 1 > 2, 2 > 1)
REV 4.0 - changed U19 from HC373 to HC374
REV 4.0 - added VCCSEL 0 ohm R
REV 2.3 - removed VCCSEL, V-DET
REV 2.1 - Added MCLKIN,VSYNC
JP7
FX2B-60P
U18
74HC374
U21
74F245
U30
3486
U28
3486
U29
3487
U15
22V10-25
MIDECO
(1006000)
U16
74HC251
U19
74HC251
U27D
74HC04
U22
82S123
SYNPROM
(1006070)
RN10
220R-10
RN9
330R-10
SYNC SOURCE SELECT

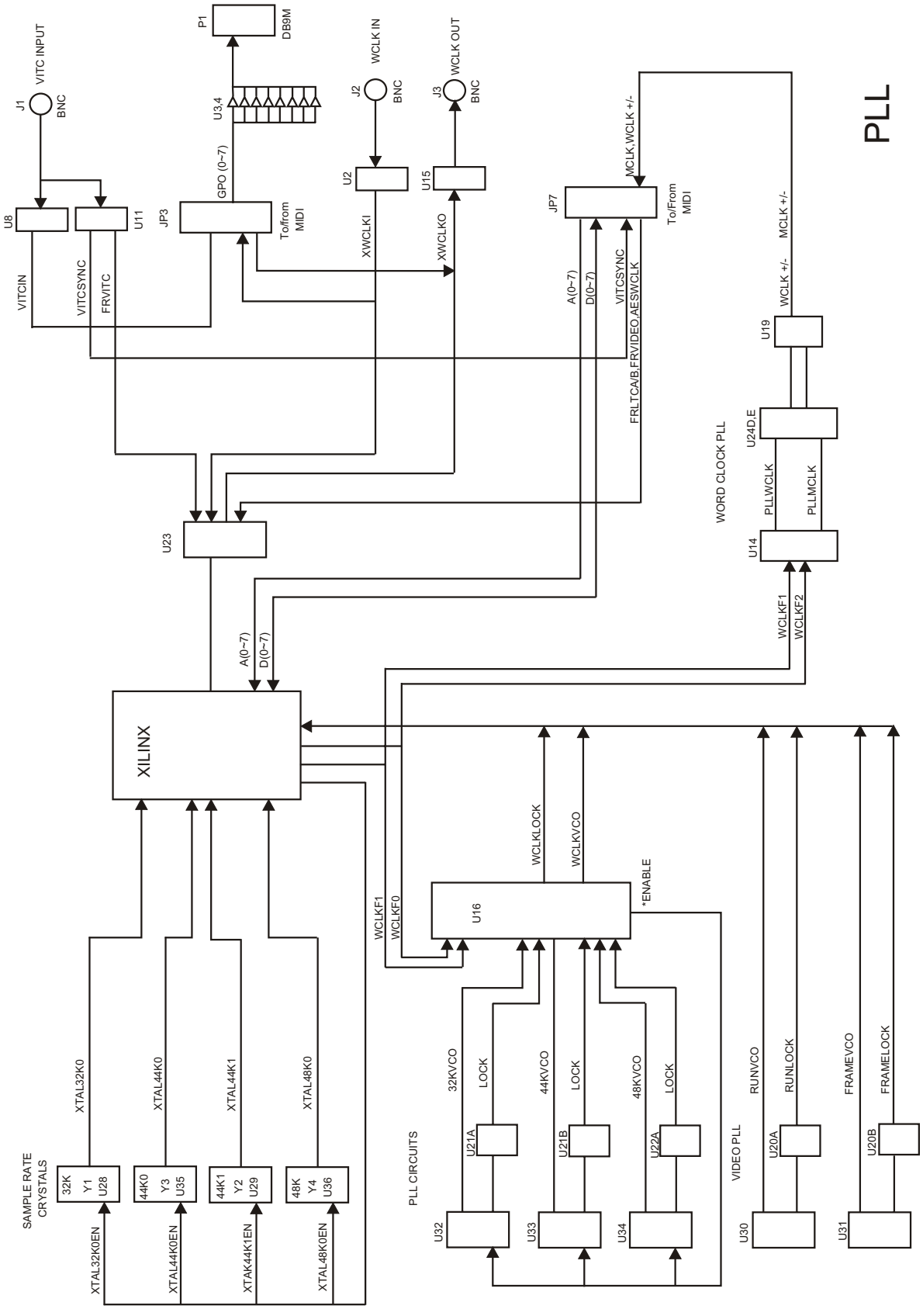

SOLDER SIDE
COMPONENT SIDE
CN1
SLOT13
(PB1)
(CLICK OUT)
SMPTEIN
CMIKEY
(CLICK IN)
SMPTEOUT
(RUN/STOP)
(RESET/START)
(SYNC OUT3)
(SYNC OUT2)
(SYNC OUT1)
MIDIOUTA
MIDIRXB
MIDIOUTB
MIDIRXA
(MUTE)
(METOUT)
KEY-
KEY+
(Obsolete)
TO ESP-SONY
JP4
IDC26 BOX
MULTIWCLK
TO ESP-LTC
JP8
IDC26 BOX
TO ESP-PLL
JP6
IDC26 BOX
TO ESP-PLL
JP5
IDC40 BOX
JP2
HEADER 5X2
JP3
IDC10 BOX
P5
CENTRONICS 24
JP1 Prelink on solder side
HEADER 4X2
U35A
U35B
U35F
U35E
74HC14
U32
PC900
D3
1N4148
U4A
U4B
U6B
DS8921
R26 220R
R25 2K2
R27 2K2
R28 220R
R5 220R
R2 2K2
R3 47K
R6 47K
MIDIOUTD
MFXTX
MFXPRESENT
MFXRX
CMIKEY
REV 4.6 - Connected pin 43b of CN1 to Gnd
REV 4.3 - Added U6b to invert *MFXPRESENT Prelinked JP1
REV 4.2 - disconnect XWCLKI from JP4 added MULTIWCLK
REV 4 - incorporate CMI354 card and MFX connector
REV 4 - change VITCHSYNC to FRVITC
REV 2.1 - Added RTS and CTS V+,V- to JP2
Fairlight ESP (c)1995
Designed: Chris Alfred
Title
ESP-MIDI CONNECTORS
Size B
Document Number CONNECT.SCH
REV 5.0
Date: July 7, 1998
Sheet 8 of 9

Fairlight ESP (c)1995
Designed: Chris Alfred
Title
ESP-MIDI EXTRAS
Size Document Number REV
B EXTRA.SCH 5.0
Date: February 1, 1995 Sheet 9 of 9
H1 ALUM SUPPORT
H2 ALUM SUPPORT
H3 M3x8mm
H4 M3x8mm
H5 4/40 1/4"
H6 4/40 1/4"
H7 M3 STAR
H8 M3 STAR
H9 M3 STAR
H10 M3 STAR
SU10 SOCKET 44 PLCC
SU11 SOCKET 44 PLCC
SU17 SOCKET 44 PLCC
SU24 SOCKET 44 PLCC
SU25 SOCKET 44 PLCC
SU22 SOCKET 16
SU15 SOCKET 24
PCB1 PCB
U26 SPARE16
TP1 TP
TP2 TP
TP3 TP
TP4 TP
TP5 TP
TP6 TP
VCC
GND
CT1 10u 16V TANT
CT2 10u 16V TANT
CT3 10u 16V TANT
CT4 10u 16V TANT
CT5 10u 16V TANT
CT6 10u 16V TANT
CT7 10u 16V TANT
CT8 10u 16V TANT
CX1 100n
CX2 100n
CX3 100n
CX4 100n
CX5 100n
CX6 100n
CX7 100n
CX8 100n
CX9 100n
CX10 100n
CX11 100n
CX12 100n
CX13 100n
CX14 100n
CX15 100n
CX16 100n
CX17 100n
CX18 100n
CX19 100n
CX20 100n
CX21 100n
CX22 100n
CX23 100n
CX24 100n
CX25 100n
CX26 100n

19.0 ESPPLL Phase Lock Loop Card



19.1 ESPPLL Block Diagram



19.2 ESPPLL Diagnostics

19.2.1 Equipment required

	Example device
3.5 digit digital voltmeter	FLUKE
100MHz or better frequency meter	LEADER LDC823A
Test connectors for SIO	

19.2.2 Setup

Shorting plug jumpers should be installed at:

JP1 ,JP8 ,JP9 ,JP10,JP11,JP12,JP13,JP14

JP15,JP16,JP17,JP18,JP19,JP20,JP21,JP22

JP4/13-14 JP4/15-16

Connect ESP-PLL to ESP-MIDI card installed to system, turn-on system.

Ensure the system does not boot to the disk-recorder.

19.2.3 VITC reader alignment

Please note that this is currently not supported.

(see schematic io.sch)

Connect voltmeter +ve to TP1.

Connect voltmeter -ve to TP2.

Adjust VR1 for 350mV +/- 10mV. [340mV to 360mV]

19.2.4 PLL low frequency check

(see schematic videopll.sch)

Connect frequency meter GND to TP15.

Connect frequency meter probe to TP7.

Check frequency is 18kHz +/- 1kHz. [17kHz to 19kHz]

NOTE: The low frequency checks for the PLLs are only approximate and will drift with temperature, however, they should be in the range specified. These checks are included as a quick way of checking the components around each PLL are correct.

19.2.5 FRAME PLL LOW FREQUENCY CHECK

Connect frequency meter GND to TP16.

Connect frequency meter probe to TP8.

Check frequency is 60kHz +/- 5kHz. [55kHz to 65kHz]

19.2.6 32kHz PLL LOW FREQUENCY CHECK

Install shorting plugs JP6/5-6, JP6/11-12, JP6/15-16.

Connect frequency meter GND to TP17.

Connect frequency meter probe to TP3.

Check frequency is 6.5MHz +/- 0.5MHz. [6.0MHz to 7.0MHz]

Connect frequency meter probe to TP4.

Check frequency is 25400Hz +/- 1900Hz. [23500Hz to 27300Hz]

Remove shorting plugs from JP6.

19.2.7 44kHz PLL LOW FREQUENCY CHECK

Install shorting plugs JP6/3-4, JP6/11-12, JP6/15-16.

Connect frequency meter GND to TP18.

Connect frequency meter probe to TP3.

Check frequency is 9.5MHz +/- 0.5MHz. [9.0MHz to 10.0MHz]

Connect frequency meter probe to TP4.

Check frequency is 37100Hz +/- 1900Hz. [35200Hz to 39000Hz]

Remove shorting plugs from JP6.

19.2.8 48kHz PLL LOW FREQUENCY CHECK

Install shorting plugs JP6/3-4, JP6/9-10, JP6/15-16.

Connect frequency meter GND to TP19.

Connect frequency meter probe to TP3.

Check frequency is 10.5MHz +/- 0.5MHz. [10.0MHz to 11.0MHz]

Connect frequency meter probe to TP4.

Check frequency is 41000Hz +/- 1900Hz. [39100Hz to 49200Hz]

Remove shorting plugs from JP6.

19.2.9 Crystal frequency adjustment

Connect frequency meter GND to TP5.

Connect frequency meter probe to TP6.

Adjust C62 for 16384.000 kHz +/- 100Hz. [16383.900kHz to 16384.100kHz]

Connect frequency meter probe to TP13.

Adjust C80 for 22556.620 kHz +/- 100Hz. [22556.520kHz to 22556.720kHz]

Connect frequency meter probe to TP12.

Adjust C63 for 22579.200 kHz +/- 100Hz. [22579.100kHz to 22597.300kHz]

Connect frequency meter probe to TP14.

Adjust C81 for 24576.000 kHz +/- 100Hz. [24575.900kHz to 24576.100kHz]

Useful Technique

Set the GATE TIME on the frequency meter to a fast time (e.g. 0.1s) to set the approximate frequency, then set the GATE TIME to a slow time (e.g. 1s) to trim to desired value. This procedure makes alignment much quicker and easier.

19.2.10 Final Shorting Plug Locations

Install shorting plugs JP6/1-2, JP6/7-8, JP6-13-14.

19.2.11 Running IO Diagnostics

System must have an ESP-SYN Sync Card and cable connecting it to the ESP-MIDI Card and the ESP-PLL installed (other SIO modules need not be installed).

Type: osk30<RETURN>	enters OSK30 operating system
scdiag <return>	start Sync Card diagnostics
	(should get SC> prompt)

Shorting plugs:

GPO

DB9 female

Pins 2-9 connect to anode of LEDs. Cathodes connected

together and to RS232 connector pin 3 via 1k resistor.

RS232

DB9 female

2-3

4-6

7-8-1

19.2.12 General Purpose Outputs (GPO)

(1) Setup: Connect GPO and RS232 shorting plugs.

Type: gpo

(2) Check that LEDs cycle ON.

(3) Press q to exit test.

Diagnostic Description

The diagnostics assertes GP0..7 signals (outputs of U24 on ESP-MIDI) in sequence in 250mS intervals. U6 and U7 open-collector buffer the signals to conector P1 (GPO).

As the test LEDs are commoned, they will not turn off completely, however, the currently driven LED should be obviously brighter.

19.2.13 Printer Port 1 (RS232)

(1) Setup: Connect RS232 shorting plug

Type: p1

(2) Press q to exit test.

IF successful, the display should show:

Send	OUT	IN	RTS->CTS	DTR->DSR	RTS->DCD
nn	pass	pass	pass	pass	pass

Diagnostics Description

For each value in the Send field, the transmit interrupt is enabled requesting to send the byte. As the transmitter should be ready, the interrupt is asserted immediately (*SERINT) by P1 duart port in U18 (68681) on ESP-MIDI and the byte is sent. The software waits 20mS which is longer than required for the data to be transmitted and received. The receive interrupts are then enabled and *SERINT interrupt should be asserted immediately as the data is received. The data received is then compared with the transmitted value. The RTS bit is set high and then low and CTS is checked that is follows RTS - similarly for DTR-DSR and RTS-DCD.

19.2.14 WCLK OUT AND WCLK IN

(1) Setup: Connect WCLK OUT to WCLK IN

Type: ep xtal 48k [starts clocks at 48k]

w

(2) Verify that received frequency is approximatly 48000Hz.

(3) Press q to exit diagnostic.

If successful, the display should show:

/ WCLK IN: 48000Hz

Diagnostics Description

The diagnostic enables the 12.288MHz crystal on the ESP-SYN card to generate 48kHz to XWCLKO and is used to measure the returned frequency from XWCLKI. As the frequency is sampled, the measurement may jitter, but should stay near 48kHz.

19.2.15 VITC SYNC INPUT

Please note that this is not currently supported.

(1) Setup: Connect video signal to VITC IN

Type: vts

(2) Verify that the horizontal sync frequency is about 25Hz for

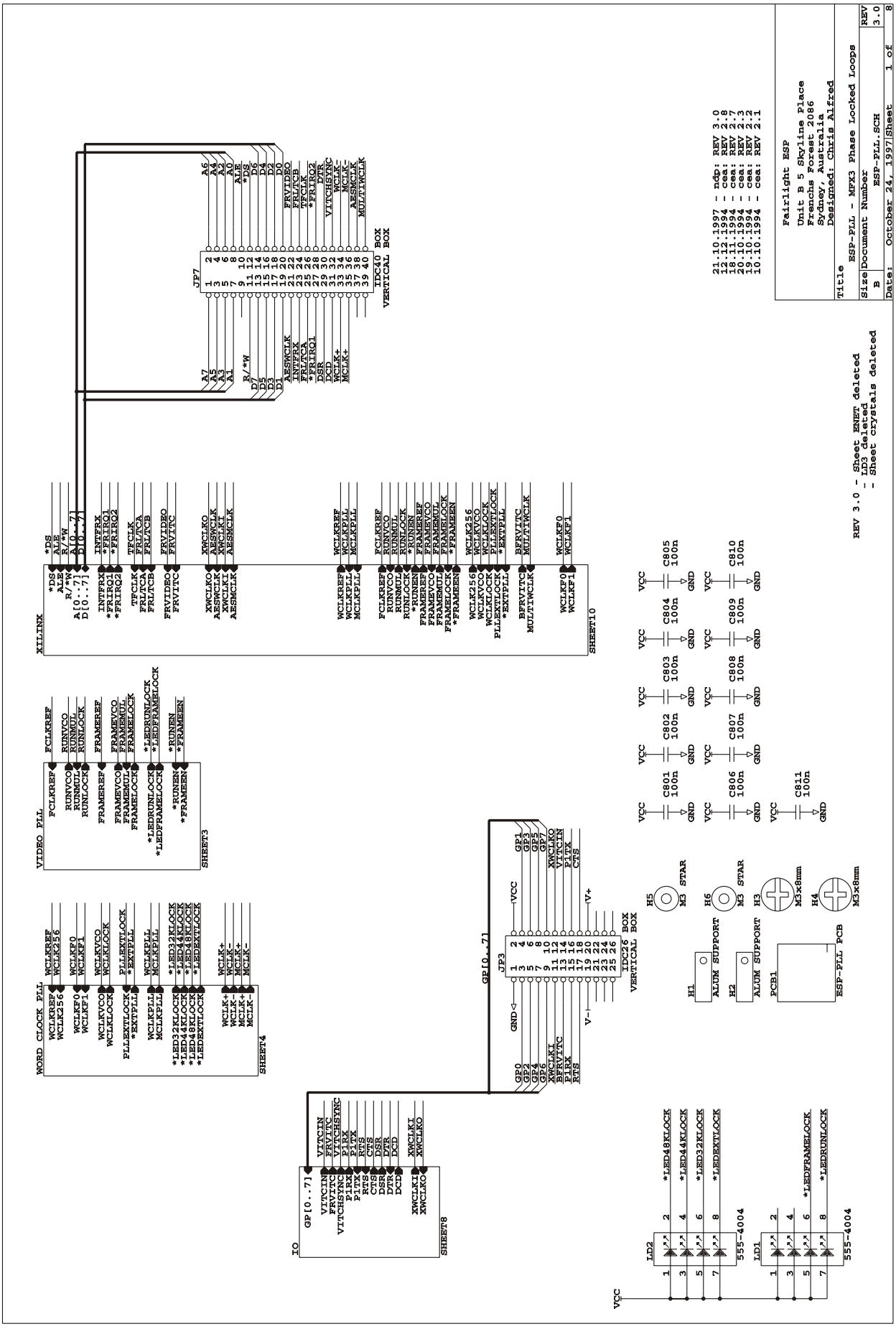
a PAL input.

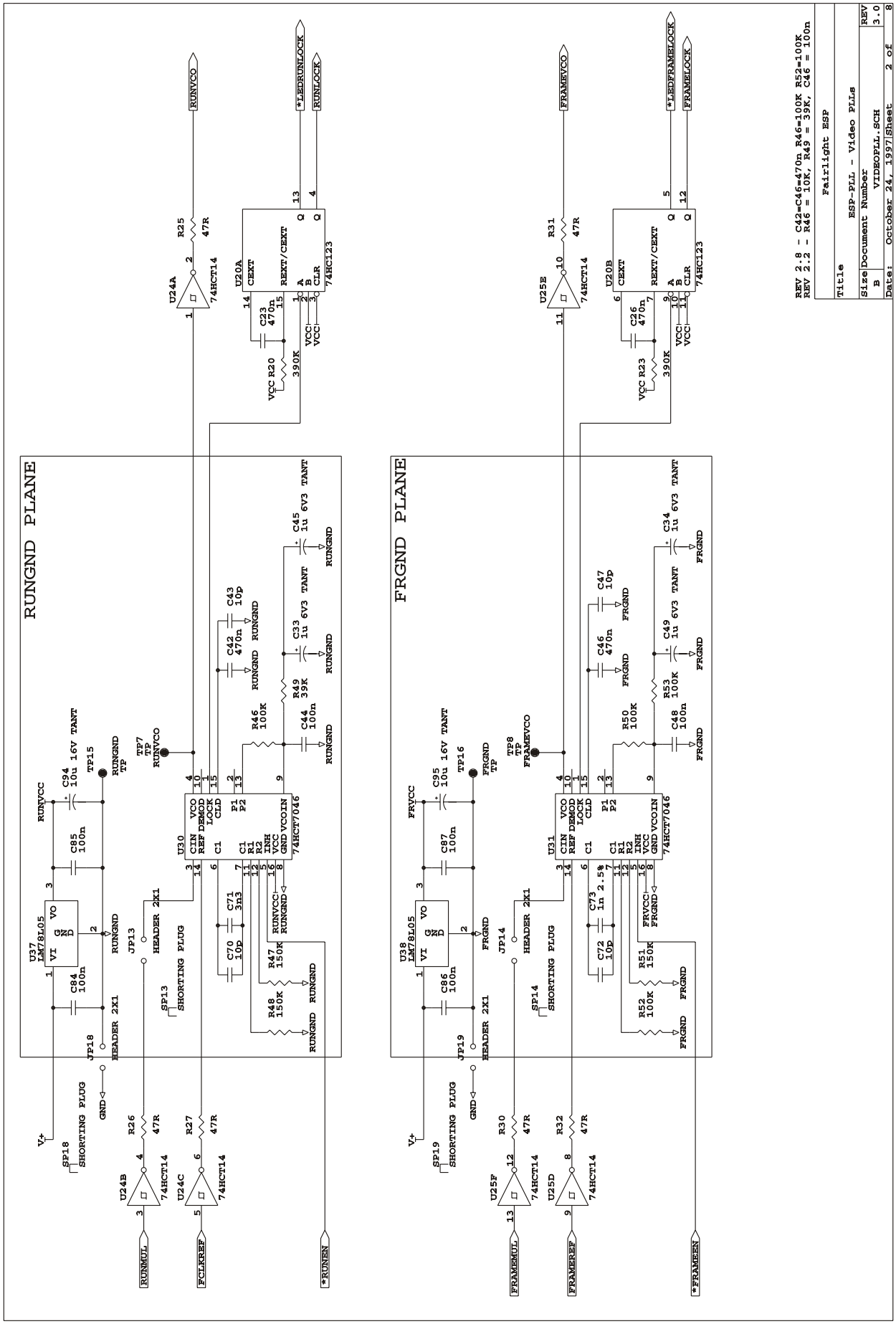
(3) Press q to exit test.

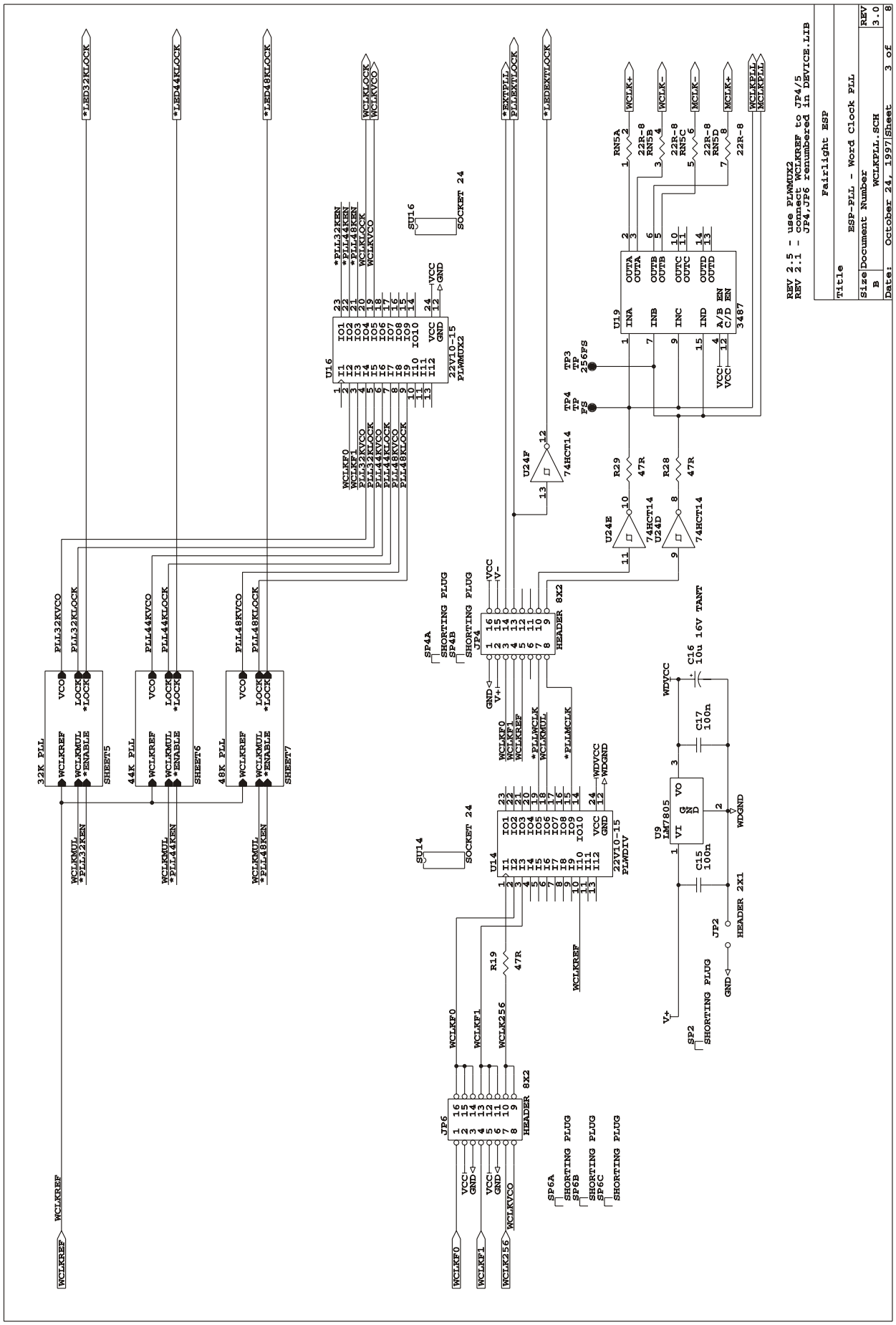
Diagnostic Description

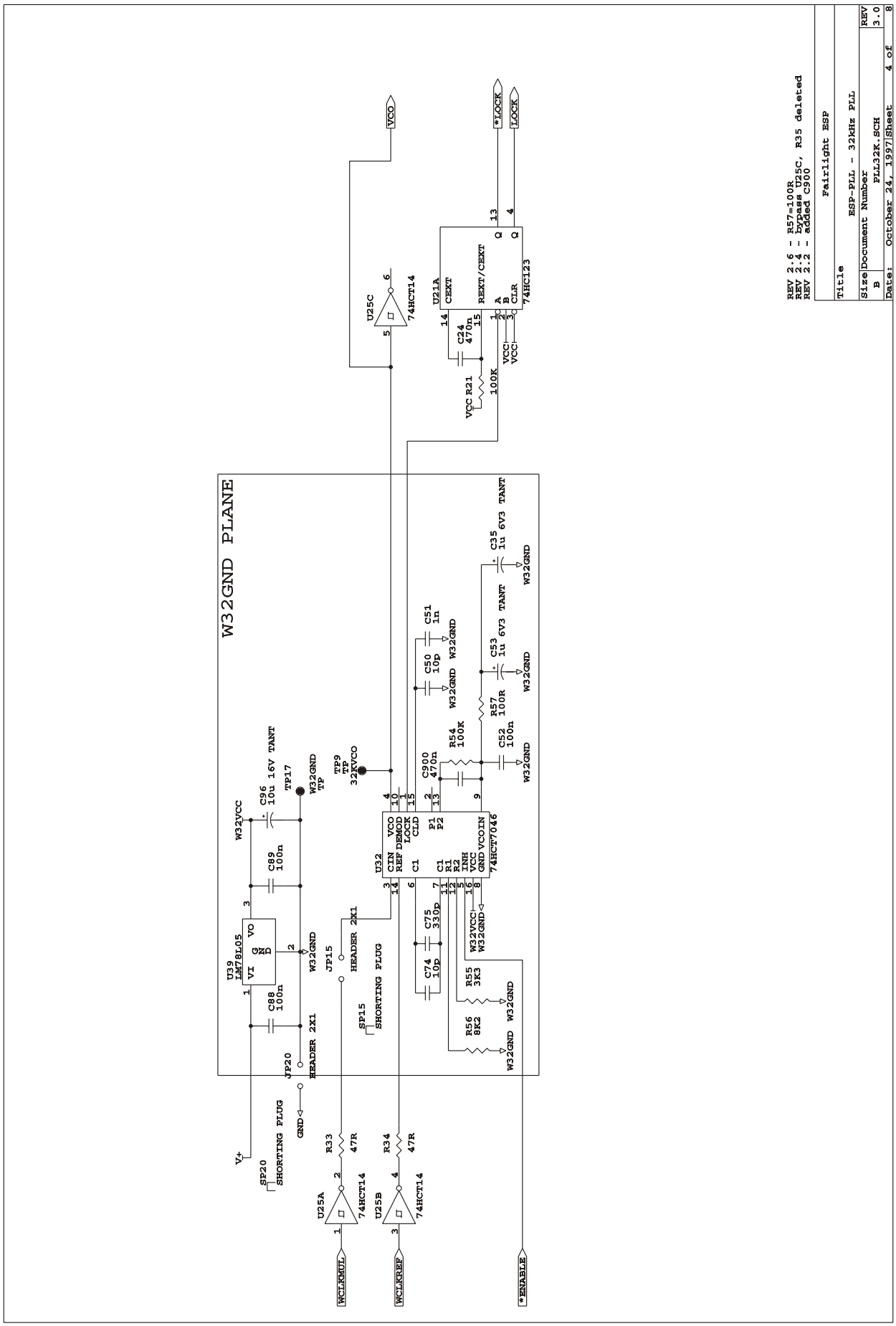
The 12.288MHz crystal is selected by the XILINX as a reference to caluculate the frequency of SIOSYNC which is selected to be VITCHSYNC.

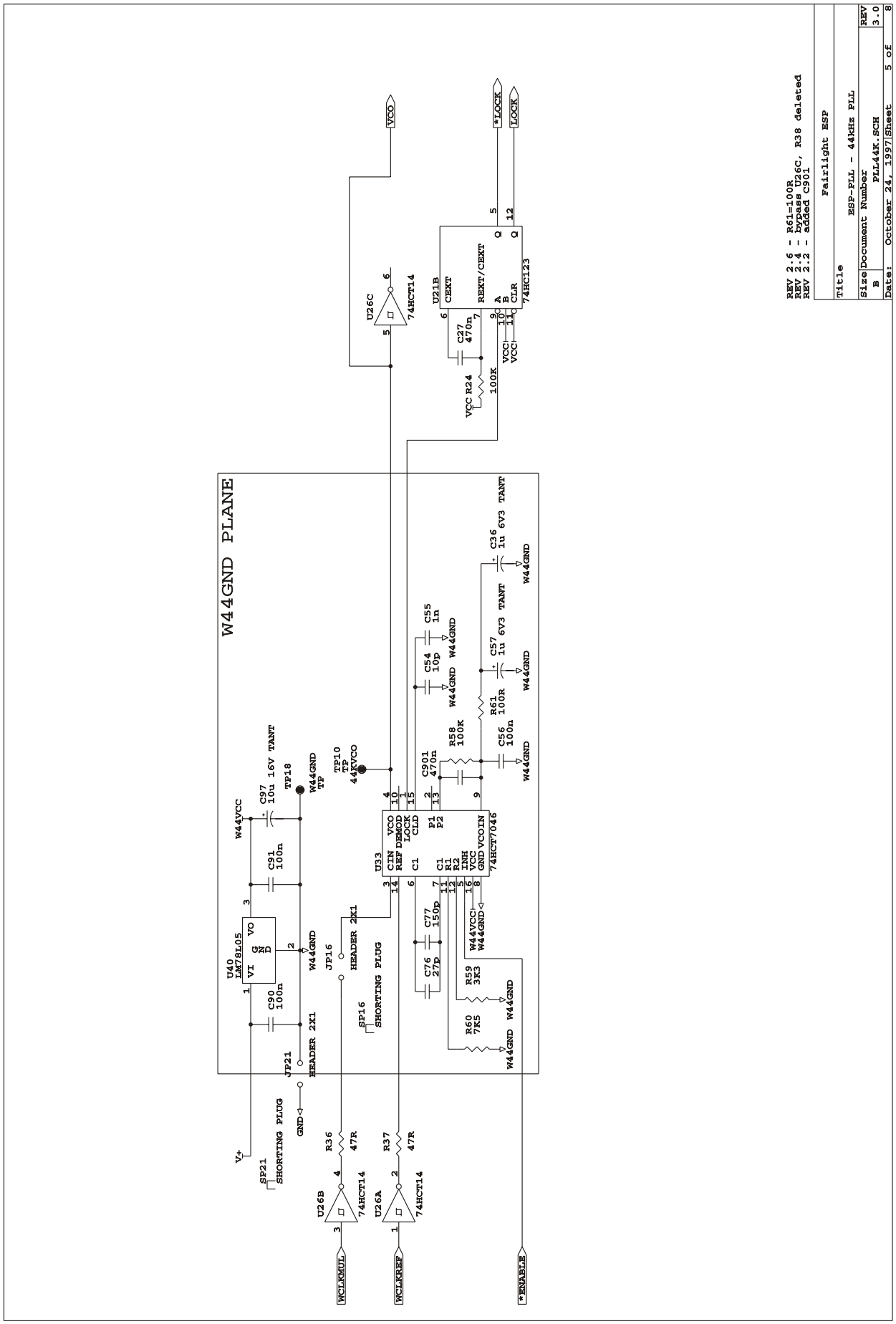
19.3 ESPPLL SCEMATICS

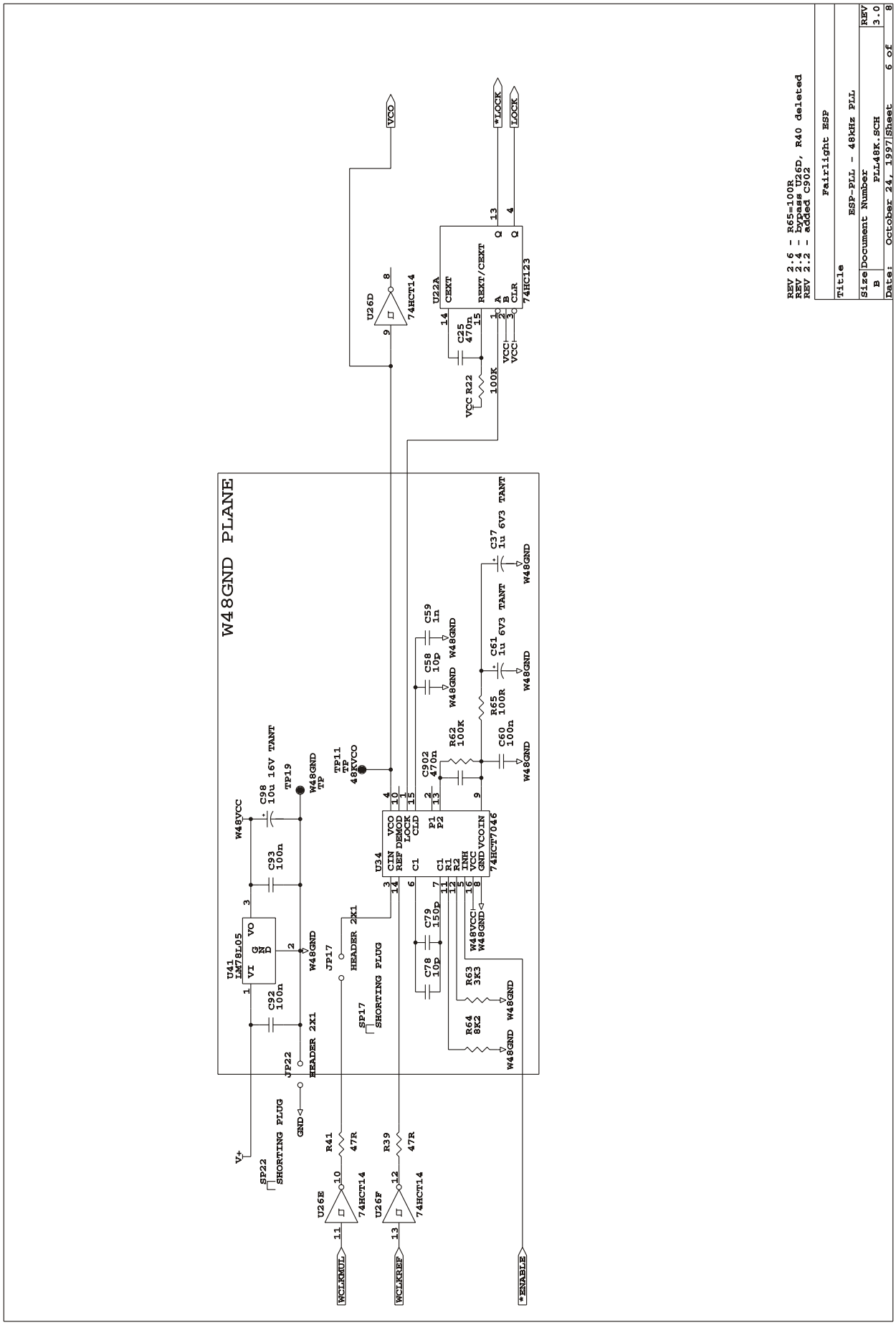


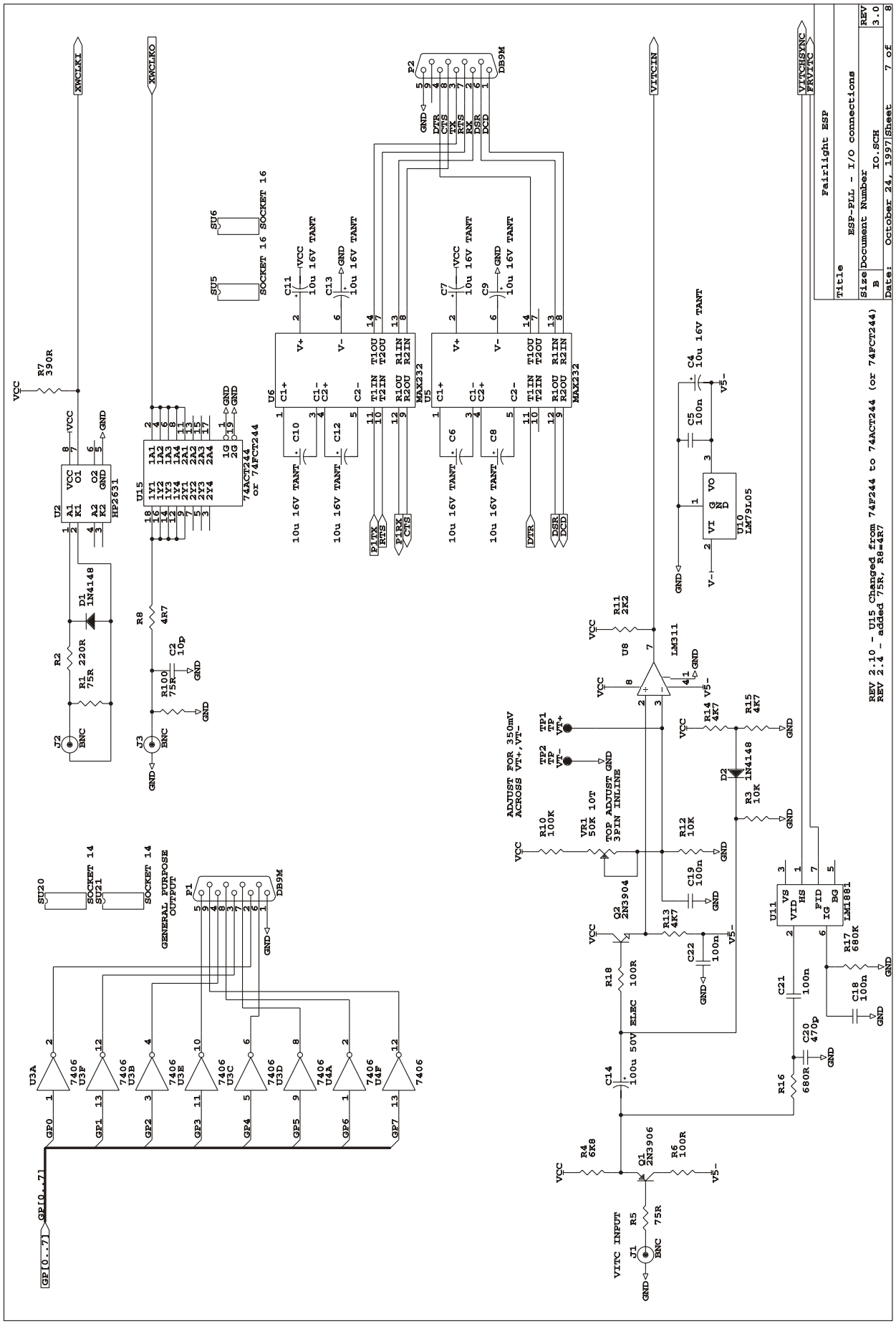

RUNGND PLANE
FRGND PLANE
U37 LM78L05
U38 LM78L05
U30 74HCT7046
U31 74HCT7046
U24A 74HCT14
U24B 74HCT14
U24C 74HCT14
U25D 74HCT14
U25E 74HCT14
U25F 74HCT14
U20A 74HC123
U20B 74HC123
RUNVCO
FRAMEVCO
*LEDRUNLOCK
RUNLOCK
*LEDFRAMELOCK
FRAMELOCK
RUNMUL
FCLKREF
*RUNEN
FRAMEMUL
FRAMEREF
*FRAMEEN
SHORTING PLUG
HEADER 2X1
REV 2.8 - C42=C46=470n, R46=100K R52=100K
REV 2.2 - R46 = 10K, R49 = 39K, C46 = 100n
Fairlight ESP
ESP-PLL - Video PLLs
VIDEOPLL.SCH
October 24, 1997
2 of 8
3.0

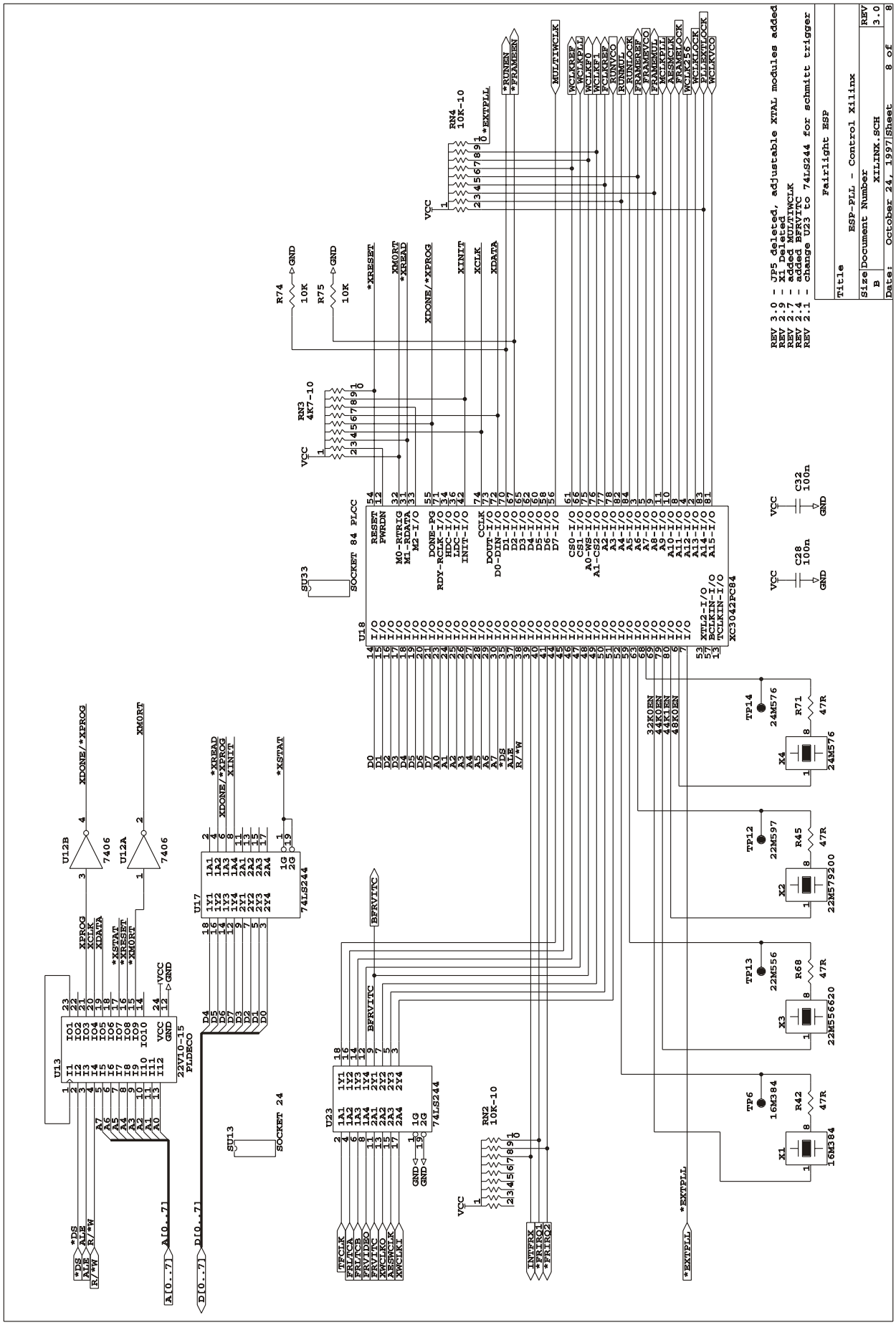

REV 2.5 - use PLWMUX2
REV 2.1 - connect WCLKREF to JP4/5
JP4,JP6 renumbered in DEVICE.LIB
Fairlight ESP
Title
ESP-PLL - Word Clock PLL
Size B
Document Number WCLKPLL.SCH
REV 3.0
Date: October 24, 1997 Sheet 3 of 8
32K PLL
44K PLL
48K PLL
SHEET5
SHEET6
SHEET7
WCLKREF
WCLKMUL
*PLL32KEN
*PLL44KEN
*PLL48KEN
PLL32KVCO
PLL32KLOCK
PLL44KVCO
PLL44KLOCK
PLL48KVCO
PLL48KLOCK
*LED32KLOCK
*LED44KLOCK
*LED48KLOCK
WCLKLOCK
WCLKVCO
*EXTPLL
PLLEXTLOCK
*LEDEXTLOCK
U16
22V10-15
PLWMUX2
SU16
SOCKET 24
WCLKF0
WCLKF1
WCLK256
U14
SU14
PLWDIV
JP6
HEADER 8X2
SP4A
SP4B
SP6A
SP6B
SP6C
SHORTING PLUG
JP4
U24F
U24E
U24D
74HCT14
R29
R28
R19
47R
TP3
TP4
256FS
FS
U19
3487
RN5A
RN5B
RN5C
RN5D
22R-8
WCLK+
WCLK-
MCLK-
MCLK+
WCLKFPLL
MCLKFPLL
U9
LM7805
C15
C16
C17
10u 16V TANT
100n
WDVCC
WDGND
JP2
SP2
VCC
GND
V+
V-


W32GND PLANE
REV 2.6 - R57=100R
REV 2.4 - bypass U25C, R35 deleted
REV 2.2 - added C900
Fairlight ESP
Title
ESP-PLL - 32kHz PLL
Size
B
Document Number
PLL32K.SCH
REV
3.0
Date: October 24, 1997
Sheet 4 of 8
U39
LM78L05
C88 100n
C89 100n
C96 10u 16V TANT
TP17
W32GND TP
TP9 TP 32KVCO
JP15 HEADER 2X1
SP15 SHORTING PLUG
JP20 HEADER 2X1
SP20 SHORTING PLUG
U32
74HCT7046
C74 10p
C75 330p
C900 470n
C50 10p
C51 1n
C52 100n
C53 1u 6V3 TANT
C35 1u 6V3 TANT
R54 100K
R55 3K3
R56 8K2
R57 100R
R33 47R
R34 47R
U25A
U25B
U25C
74HCT14
U21A
74HC123
C24 470n
VCC R21 100K
VCO
*LOCK
LOCK
W32VCC
W32GND
*ENABLE
WCLKMUL
WCLKREF

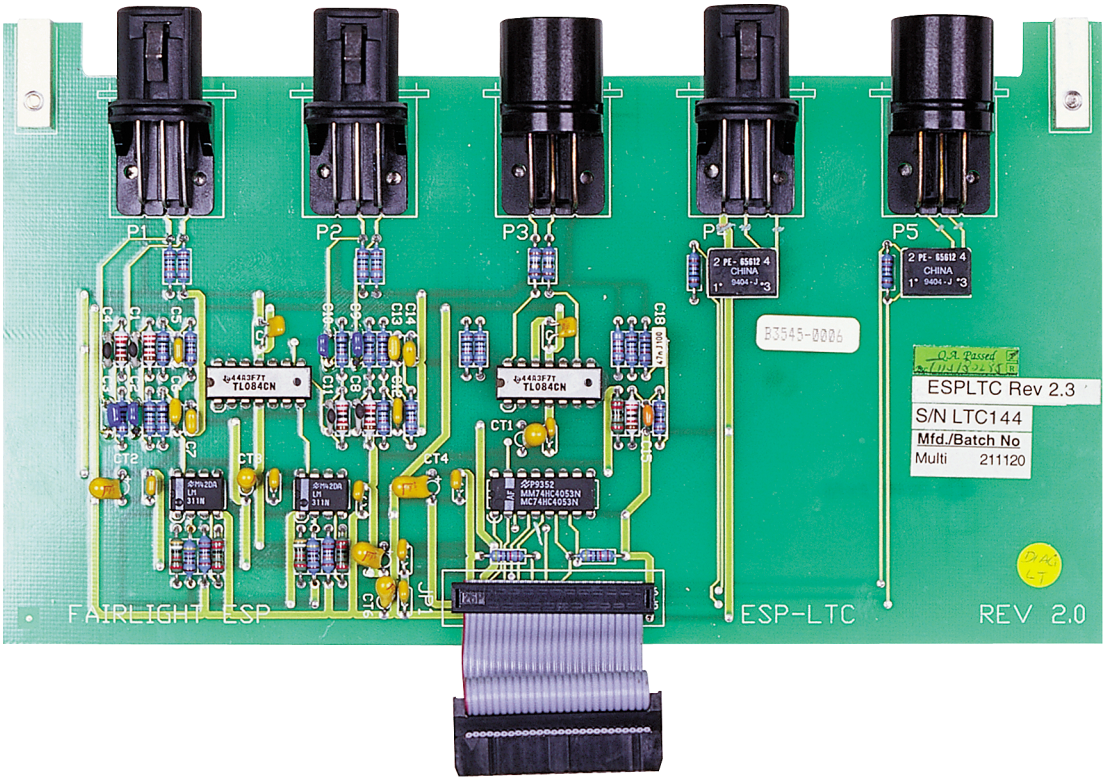

W44GND PLANE
REV 2.6 - R61=100R
REV 2:4 - bypass U26C, R38 deleted
REV 2:2 - added C901
Fairlight ESP
Title
ESP-PLL - 44KHz PLL
Size Document Number REV
B PLL44K.SCH 3.0
Date: October 24, 1997 Sheet 5 of 8
U40 LM78L05
C97 10u 16V TANT
C91 100n
C90 100n
TP18
W44GND TP
TP10 TP 44KVCO
JP16 HEADER 2X1
SP16 SHORTING PLUG
JP21 HEADER 2X1
SP21 SHORTING PLUG
U33 74HCT7046
C901 470n
R58 100K
C54 10p
C55 1n
C57 1u 6V3 TANT
C36 1u 6V3 TANT
R61 100R
C56 100n
C77 150p
C76 27p
R59 3K3
R60 7K5
R36 47R
R37 47R
U26B 74HCT14
U26A 74HCT14
U26C 74HCT14
U21B 74HC123
C27 470n
VCC R24 100K
WCLKMUL
WCLKREF
*ENABLE
VCO
*LOCK
LOCK
W44VCC
W44GND
V+
GND


W48GND PLANE
REV 2.6 - R65-100R
REV 2.4 - bypass U26D, R40 deleted
REV 2.2 - added C902
Fairlight ESP
Title
ESP-PLL - 48kHz PLL
Size B
Document Number PLL48K.SCH
REV 3.0
Date: October 24, 1997 Sheet 6 of 8
U41 LM78L05
C92 100n
C93 100n
C98 10u 16V TANT
TP19
W48GND TP
TP11 TP 48KVCO
W48VCC
JP22 HEADER 2X1
SP17 SHORTING PLUG
JP17 HEADER 2K1
SP22 SHORTING PLUG
GND
V+
U34 74HCT7046
C1
C78 10p
C79 150p
R63 3K3
R64 8K2
C902 470n
R62 100K
C58 10p
C59 1n
C60 100n
R65 100R
C61 1u 6V3 TANT
C37 1u 6V3 TANT
U26D 74HCT14
U22A CEXT
C25 470n
R22 100K
REXT/CEXT
74HC123
VCC
*LOCK
LOCK
U26E 74HCT14
U26F 74HCT14
R41 47R
R39 47R
WCLKOUT
WCLKREF
*ENABLE

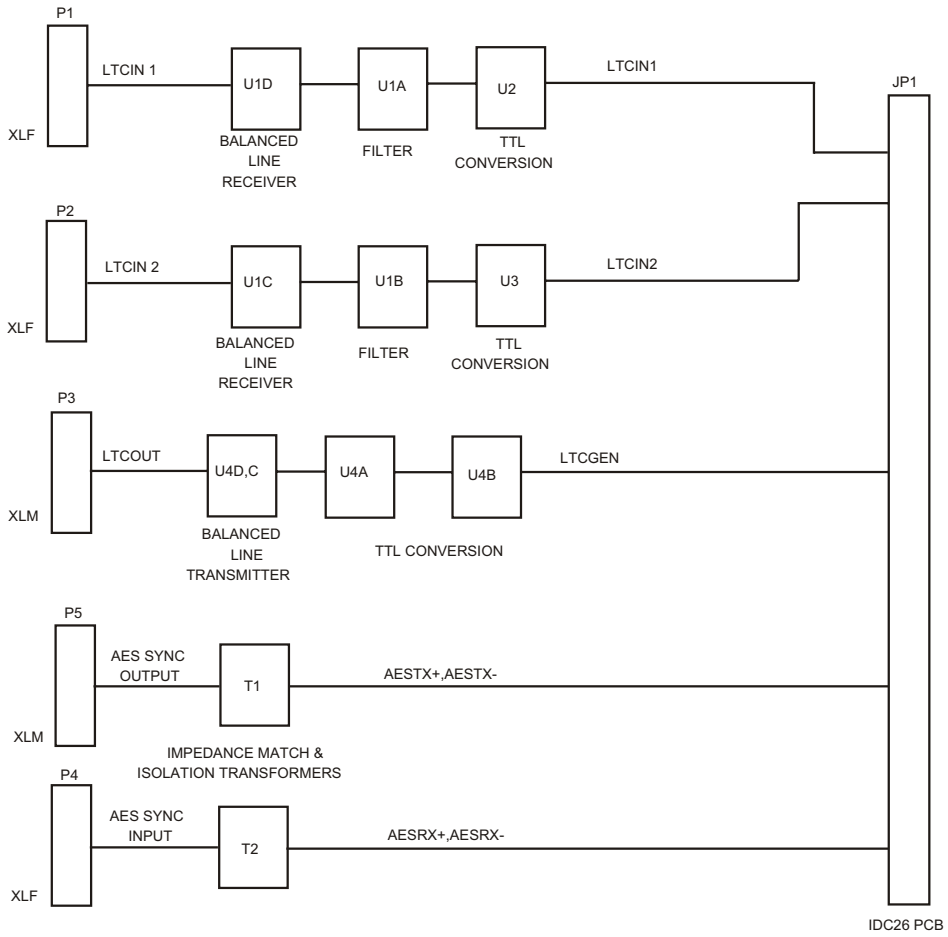

Fairlight ESP
ESP-PLL - I/O connections
Size B
Document Number IO.SCH
Date: October 24, 1997 Sheet 7 of 8
REV 3.0
REV 2.10 - U15 Changed from 74F244 to 74ACT244 (or 74FCT244)
REV 2.4 - added 75R, R8=4R7
XWCLKI
XWCLKO
VTTCHSYNC
FRVTTC
VTTCIN
GP[0..7]
VCC
GND
V5-
U2 HP2631
U15 74ACT244 or 74FCT244
U5 MAX232
U6 MAX232
U8 LM311
U10 LM79L05
U11 LM1881
D1 1N4148
D2 1N4148
R1 75R
R2 220R
R3 10K
R4 6K8
R5 75R
R6 100R
R7 390R
R8 4R7
R10 100K
R11 2K2
R12 10K
R13 4K7
R14 4K7
R15 4K7
R16 680R
R17 680K
R18 100R
R100 75R
VR1 50K 10T TOP ADJUST 3PIN INLINE
ADJUST FOR 350mV ACROSS VT+,VT-
Q1 2N3906
Q2 2N3904
C2 10p
C4 10u 16V TANT
C5 100n
C6 10u 16V TANT
C7 10u 16V TANT
C8 10u 16V TANT
C9 10u 16V TANT
C10 10u 16V TANT
C11 10u 16V TANT
C12 10u 16V TANT
C13 10u 16V TANT
C14 100u 50V ELEC
C18 100n
C19 100n
C20 470p
C21 100n
C22 100n
J1 VITC INPUT
J2 BNC
J3 BNC
P1 DB9M
P2 DB9M
SU5 SOCKET 16
SU6 SOCKET 16
SU20 SOCKET 14
SU21 SOCKET 14
GENERAL PURPOSE OUTPUT
TP1 TP VT+
TP2 TP VT-
P1TX RTS
P1RX CTS
DTR
DSR DCD
U3A 7406 U3F 7406 U3B 7406 U3E 7406 U3C 7406 U3D 7406 U4A 7406 U4F 7406


REV 3.0 - JP5 deleted, adjustable XTAL modules added
REV 2.9 - X1 Deleted
REV 2.8 - added MULTIWCLK
REV 2.7 - added BFRVITC
REV 2.1 - change U23 to 74LS244 for schmitt trigger
Fairlight ESP
Title
ESP-PLL - Control Xilinx
Size B
Document Number XILINX.SCH
REV 3.0
Date: October 24, 1997 Sheet 8 of 8
U13
22V10-15 PLDECO
U12B
U12A
7406
U17
74LS244
U23
74LS244
SU33
SOCKET 84 PLCC
U18
XC3042PC84
SU13
SOCKET 24
RN2 10K-10
RN3 4K7-10
RN4 10K-10
R74 10K
R75 10K
X1 16M384
X2 22M579200
X3 22M556620
X4 24M576
R42 47R
R45 47R
R68 47R
R71 47R
TP6 16M384
TP12 22M597
TP13 22M556
TP14 24M576
C28 100n
C32 100n
*DS
ALE
R/*W
A[0..7]
D[0..7]
XPROG
XCLK
XDATA
*XSTAT
*XRESET
*XMORT
XDONE/*XPROG
*XRESET
*XREAD
XMORT
XINIT
XCLK
XDATA
*RUNEN
*FRAMEEN
MULTIWCLK
WCLKREF
WCLKPLL
WCLKF0
WCLKF1
FCLKREF
RUNVCO
RUNMULTI
FRAMEREF
FRAMEVCO
FRAMEMUL
MCLKPLL
FRAMELOCK
WCLK256
WCLKLOCK
PLLEXTLOCK
WCLKVCO
BFRVITC
*EXTPLL
32K0EN
44K0EN
44K1EN
48K0EN
TFCLK
FRVCLK
FRVDATA
FRVIDEO
FRVITC
XWCLKO
ABSWCLK
XMCLKI
INTRQ
*FRIRQ
*FRTRQ

20.0 ESPLTC LTC Card



20.1 Block Diagram



20.2 Diagnostics

20.2.1 Running Diagnostics

Equipment Required

Time code Generator/Reader

XLR Male to XLR Female cable

System must have an ESP-SYN Sync Card and cable connecting it to the ESP-MIDI Card and the ESP-LTC installed (other SIO modules need not be installed).

Type:

osk30	enters OSK30 operating system
scdiag	start Sync Card diagnostics

(should get SC> prompt)

20.2.2 LTC readers

(1) Setup: Connect LTC IN A to GEN CODE OUT on Time code Generator

Type: lr<return>

Verify that the code is changing.

20.2.3 LTC Generator and Readers

(1) Setup: Connect LTCOUT to LTC IN A

Type: l 12345678

Linear timecode is generated at LTCOUT with the user data set to 12345678. Verify that the code is changing at realtime speed by timing one minute of timecode time, and verify that LTC IN A reports the data sent.

(2) Press <space> to revese direction of generated data.

Verify that LTC IN A reports the correct direction of timecode.

Also check that timecode passes backwards through midnight correctly.

(3) Setup: Connect LTCOUT to LTC IN B

Verify that the code is changing at realtime speed and that LTC IN B reports the data sent.

(4) Press <space> to reverse direction of generated data.

Verify that LTC IN B reports the correct direction of timecode.

Also check that timecode passes backwards through midnight

correctly.

(5) Setup: Connect LTCOUT to MASTER CODE IN of ZETA-THREE

timecode reader.

Press DISPLAY button on ZETA-THREE until M_TC

appears on the display.

The ZETA-THREE should show the generated time and the green MTC

LED should light and not extinguish (unless the <SPACE> is pressed to reverse the direction).

(6) Press q to exit diagnostic.

LTC Generation

The LTC generator is clocked by LTCOUTCLK generated by the 68681 DUART at U10 on the ESP-MIDI Card by dividing the MIDICLK input. This clock is transmitted to the XILINX (U29) on the ESP-SYN Card. An interrupt is generated every LTCOUTCLK period on *SERINT to reload the 68681 divder used to generate the clock.

Every 16 clocks, an interrupt at level 6 is sent to the 68030 CPU. In response, the next data byte is written to the XILINX. In the XILINX, data is clocked out on every second LTCOUTCLK clock. If the data is a 1 the output is at LTCOUTCLK frequency; is the data is a 0 the output is at half the LTCOUTCLK frequency. The resulting encoded data is transmitted to the ESP-LTC card as LTCOUT.

Upon entering the diagnostics, the LTCGENSEL control bit is set low so that U5 (74HC4053) selects LTCGEN to be LTCOUT from the ESP-SYN Card. LTCGEN is filtered by U4B (TL084) and differentially buffered by U4A,U4C,U4D to the output socket.

As most of the generation circuitry is in the XILINX, debugging pins are provided on the XILINX (U29 on ESP-SYN).

Pin 71	Active low signal used to load the next byte into the shift register for transmission.
Pin 75	The raw serial data shifted out by LTCOUTCLK divided by two.
Pin 73	The selected clock (LTCOUTCLK/2 or LTCOUTCLK) used to encode the data.

LTC Readers

The LTC data at the LTC IN A/B sockets is filered by U1 (TL084) and Schmitt triggered by U2, 3 (LM311) to produce LTCINA and LTCINB to be sent to the TR1 decoder (U14 on ESP-MIDI). The TR1 decoder uses the 8MHz LTCCLK input to interpret the encoded input. Every frame received generates an interrupt on *TCINT to be sent to the ESP-SYN Card. Opon servicing the interrupt, the 68030 CPU on the ESP-SYN card reads all 8 registers from the TR1 chip.

The TR1 chip detects the direction of incoming timecode. The direction signals (FWD/*REVA, FWD/*REVA) are fed into the 68681 duart at U18 on the ESP-MIDI. It is the value of these signals that are reported by the diagnostic.

20.2.4 AES SYNC IN AND OUT

1. Setup: Connect AES SYNC OUT to AES SYNC IN

   Type: ep xtal 32k

   a

   The AES SYNC OUT will generate valid AES code at 32kHz.

   Once locked to the input, the display should show:

   AES SYNC OUTPUT AES SYNC INPUT

Sample Rate	Type	Source Rate	Detected Rate
32000Hz	AES	32k	32k 400ppm

2. Type: ep xtal 44k0

   a

   The AES SYNC OUT will generate valid AES code at 44056Hz.

   Once locked to the input, the display should show:

   AES SYNC OUTPUT AES SYNC INPUT

Sample Rate	Type	Source Rate	Detected Rate
44056Hz	AES	44k1	44k056 400ppm

3. Type: ep xtal 44k1

   a

   The AES SYNC OUT will generate valid AES code at 44100Hz.

   Once locked to the input, the display should show:

   AES SYNC OUTPUT AES SYNC INPUT

Sample Rate	Type	Source Rate	Detected Rate
44100Hz	AES	44k1	44k1 400ppm

4. Type: ep xtal 48k

   a

The AES SYNC OUT will generate valid AES code at 48kHz.

Once locked (may take several seconds) to the input, the display should show:

AES SYNC OUTPUT AES SYNC INPUT

Sample Rate	Type	Source Rate	Detected Rate
48000Hz	AES	48k	48k 400ppm

5. Press q to exit test.

20.2.5 AES Sync Generation

The output frequency is generated by selecting the appropriate crystal on the ESP-PLL Card. The ESP-PLL divides the selected crystal by 512 to generate WCLKOUT (digital word clock). These clocks are fed into the CS8401 AES encoder at U68 on the ESP-SYN Sync Card. Data is written into the AES encoder to generate a valid AES output stream so an external AES receiver should lock correctly to the AES SYNC OUT. The differential output from the encoder is sent via the 60way cable to the ESP-LTC Card to be transformer isolated and impedence matched.

The audio data input to the AES encoder is connected to GND to produce an 'AES black' signal required for synchronisation.

20.2.6 AES Sync Reception

Differential data received on the ESP-LTC Card is impedence matched and transformer isolated before feeding the signals into the CS8411 decoder at U23 on the ESP-MIDI. The decoder phase locks to the incoming stream to extract clocks at AESMCLK (at 256 times sample rate) and AESWCLK (at sample rate).

Address line A4 (pin 13) on the decoder has 6.144MHz connected to it by asserting AESDETECT on U33 (74HC4053 on ESP-MIDI). This clock is used by the decoder to detect the incoming data sample rate.

Diagnostic Field Description

Sample Rate:

Sample rate at AES SYNC OUT.

Type:

Type of digital data detected (AES or SPDIF). Only AES

should used for synchronisation purposes.

Source Rate:

The sample rate of the original source material. Note that data transmitted at 44k056 is always 44k1 source material running 0.1% slow.

Detected Rate:

The incoming sample rate as detected by the decoder.

20.2.7 AES Sync Frequency

1. Setup: Connect AES SYNC IN to AES SYNC OUT

   Type: ep xtal 48k

   af

2. Check that received frequency is approximately 48kHz.

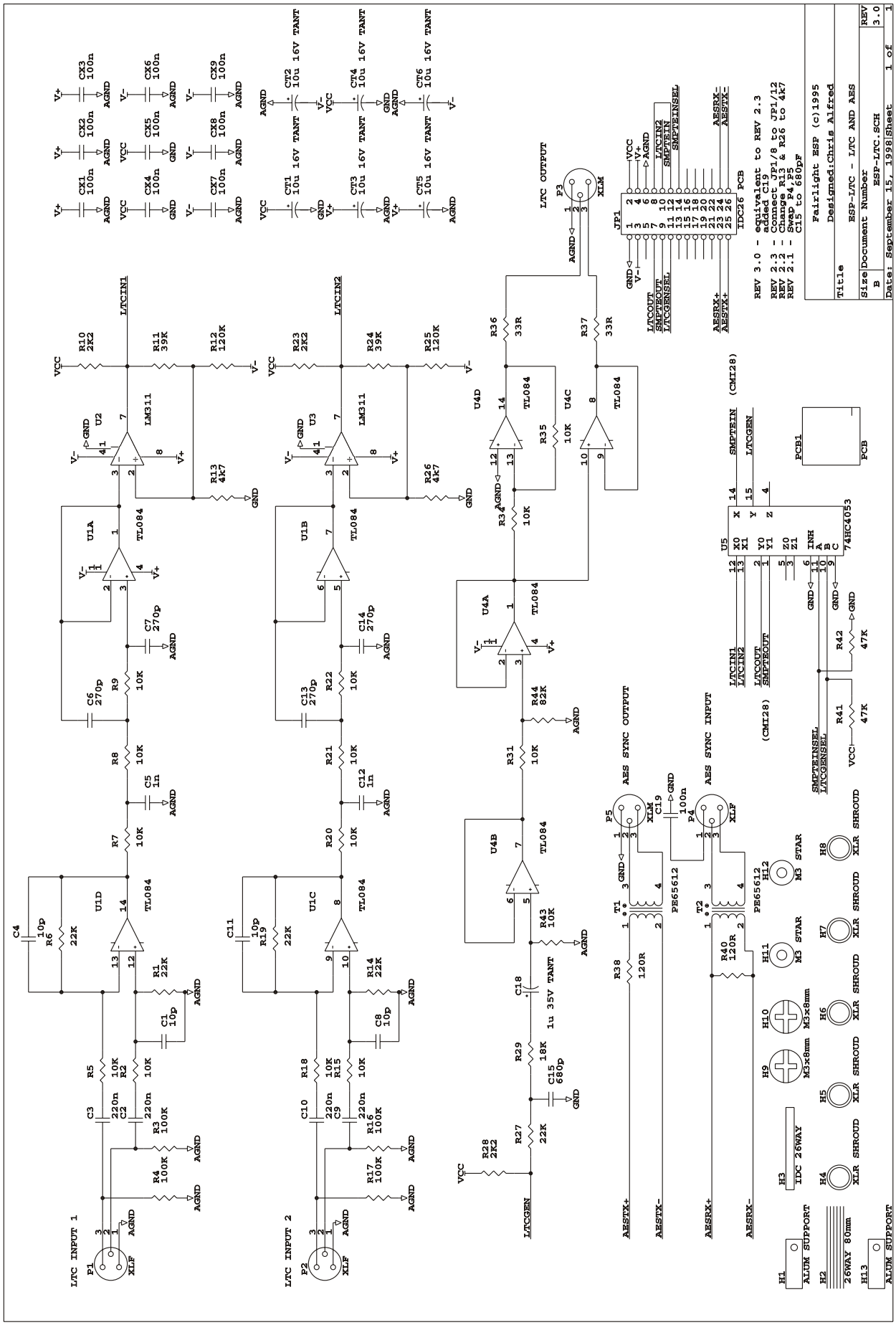
3. Press q to exit diagnostic.

20.2.8 Diagnostic Description

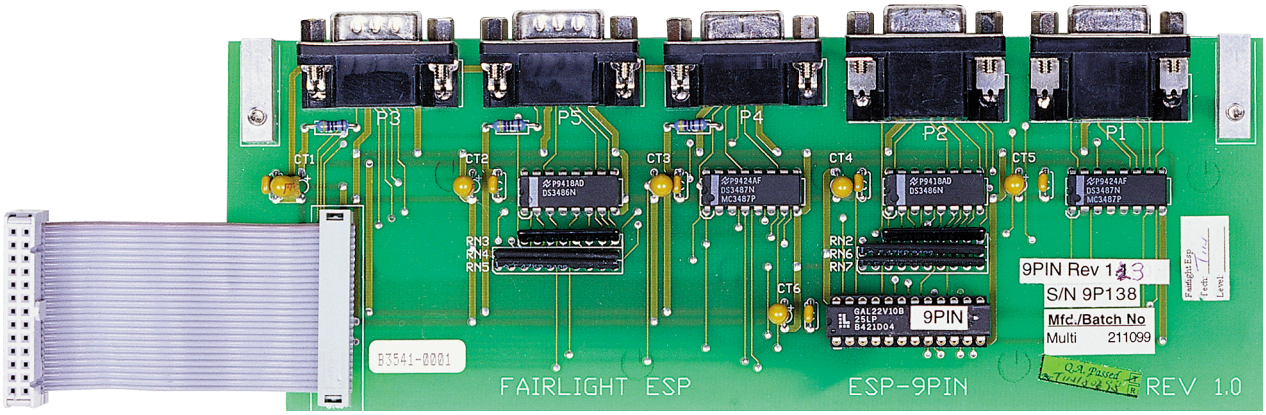
The diagnostic transmits AES data at 48kHz. The loop-back data is decoded by the AES receiver and its internal PLL generates AESWCLK. This PLL takes about 5 seconds to lock to a new input. Once locked, the display should show about 48kHz.

As the diagnostic measures the PLL of the receiver chip, if there is no AES input, the frequency displayed will be about 9kHz (rather than no signal) which is the lowest frequency the PLL can produce.

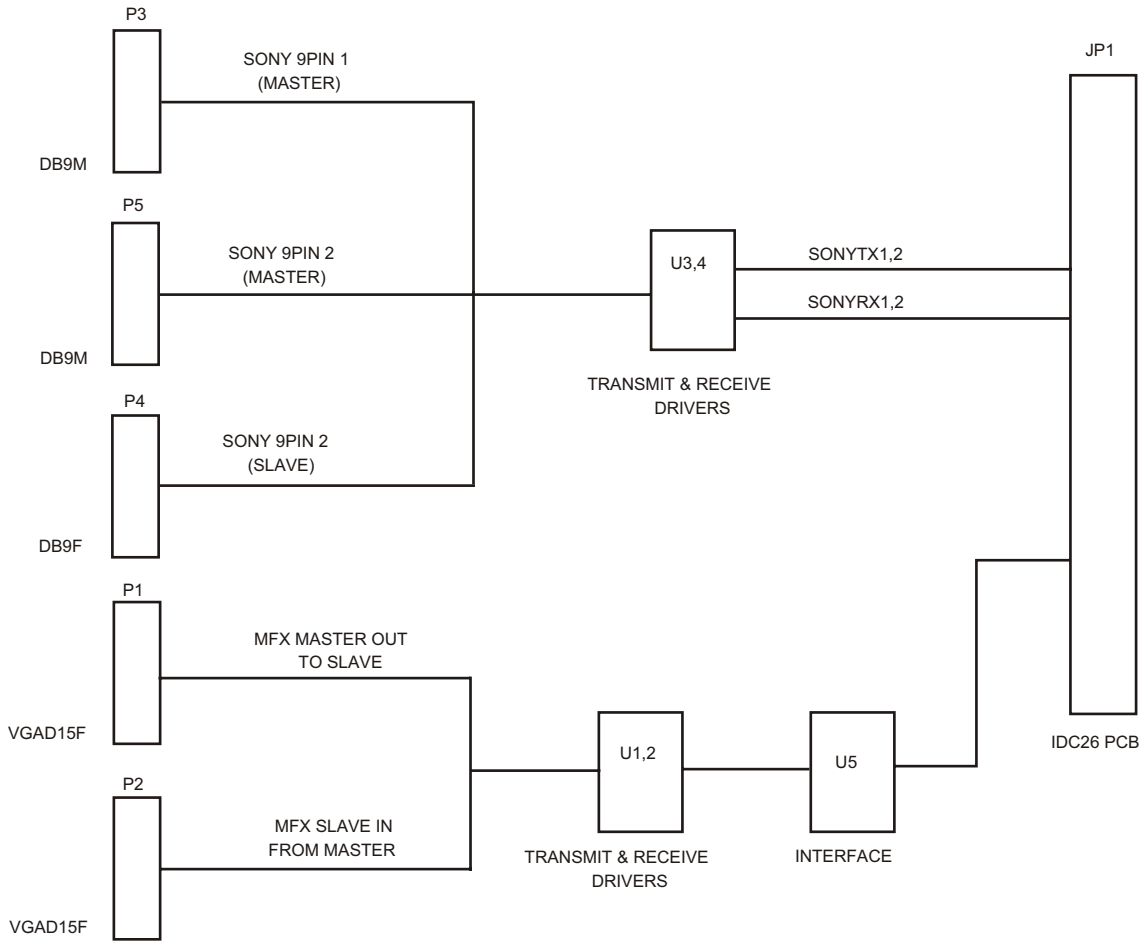
20.3 ESPLTC SCHEMATIC



21.0 ESP9PIN 9Pin Card



21.1 Block Diagram



21.2 Diagnostics

21.2.1 Running Diagnostics

System must have an ESP-SYN Sync Card and cable connecting it to the ESP-MIDI Card and the ESP-9PIN installed (other SIO modules need not be installed).

Type: osk30 enters OSK30 operating system

scdiag start Sync Card diagnostics

(should get SC> prompt)

A set of shorting plugs is required (connect pins joined by lines):

MACHINE A MACHINE B MACHINE SLAVE MFX IN MFX OUT

DB9 Female DB9 Female DB9 Male DB15MiniMale DB15MiniMale

2-8

3-7

2-8

3-7

2-8

3-7

2-3

7-8

2-3

7-8

5----------4

4----------5

10----------9

5----------5----------5----------9----------10

21.2.2 9PIN MASTER PORTS

(1) Setup: Connect shorting plug to MACHINE A

Connect shorting plug to MACHINE B

Connect shorting plug to MACHINE SLAVE

Type: s

(2) Press q to exit test.

The diagnostic shows the status of transmission and reception of each byte sent (value shown in Send field). The OUT and IN columns show report status as:

PASS	successful transmission/reception
FAIL	unsuccessful transmission/reception
....	no bytes received
I:nn	Extra interrupt, received nn.
L:nn	Lost interrupt, received nn.
[nn]	Incorrect data received

Upon success, the screen should show:

MASTER	OUT		IN		SLAVE	OUT	IN
Send	A	B	A	B	Send	B	SLAVE
nn	PASS	PASS	PASS	PASS	nn	PASS	PASS

Description of columns:

MASTER Send	value sent to master ports
MASTER OUT A	transmission result for Port A
MASTER OUT B	transmission result for Port B
MASTER IN A	reception result for port A
MASTER IN B	reception result for port B
SLAVE Send	value sent to slave port (Port B)
SLAVE OUT B	transmission result for port B
SLAVE IN SLAVE	reception result for port B

Note that port B is switched between driving MACHINE SLAVE and MACHINE B.

Diagnostic Description

The diagnostic sets SONYSEL low to select reception on SONYRX2 to be from MACHINE B port. Transmitter interrupts for U24 (68681 duart) are enabled for both serial ports which immediately generates an interrupt on *SERINT as the ports are ready to transmit. The value in the Send field is written to the duart for both ports and the byte is transmitted. A wait for 20mS ensures adequate time for the byte to be received then the receive interrupt on both ports is enabled which immediately causes and interrupt as the byte has been received. The byte is then checked against the value transmitted.

The second phase involves setting SONYSEL high to select reception on SONYRX2 from MACHINE SLAVE port, and the above sequence is repeated just for the second duart serial port.

21.2.3 FSYNC 1..3 Frame sync

(1) Setup: Connect all shorting plugs.

This connects WCLKS+ from MFX OUT to

FSYNC1, FSYNC2, FSYNC3.

Type: ep xtal 48k

fs

(2) Press q to exit test.

If successful, display should show:

/ FSYNC1:48000Hz FSYNC2:48000Hz FSYNC3:48000Hz

The actual frequencies displayed may be slightly different and may jitter as the frequency detection is sampling the input rate.

Diagnostic Description

The diagnostic sends 48kHz via WCLKS+ on pin 10 of the MFX OUT connector by setting WCLKSEL high selecting WCLKS+ to come from XWCLKO.

WCLKS+ is looped to FSYNC 1,2,3 via the test connector. The returned FSYNC signals are frequency measured and displayed. Frequency measurement is achieved inside the XILINX on the ESP-SYN by counting the number of 12.288MHz clocks for 200 received FSYNC rising edges.

21.2.4 MULTI MFX PORTS (SERIAL INTERFACE)

(1) Setup: Connect shorting plug to MFX IN

Connect shorting plug to MFX OUT

Type: u

(3) Press q to exit test.

Upon success, the display will show:

TEST 1 TEST 2

Send	OUT	IN	OUT	IN
nn	Pass	Pass	Pass	Pass

Diganostic Description

The diagnostic has two phases TEST 1 and TEST 2, which test all states of the three control signals TXMSEL, TXSSEL, and RXSEL. In TEST 1, TXMSEL=0, TXSSEL=1, RXSEL=0; and in TEST 2, TXMSEL=1, TXSEL=0, RXSEL=1. These two configurations test all combinations of data routing provided bu the MULTI pal (U5 22V10) for the serial interface between MFX machines.

The three control signals are setup for TEST 1. Transmit interrupts are enabled causing an immediate interrupt on *SERINT as the transmitter is ready. Software then writes the value in the Send field to the duart (68681 at U10) and the byte is transmitted. A wait for 20mS ensures that adequate time has elapsed for the byte to be received and the receive interrupt is enabled. As the byte has already been received, *SERINT should be asserted immediately. This byte is the compared for success. This sequence is then repeated for TEST 2 setup.

MULTI pal is effectively a serial data multiplexor driven by the three control signals. During TEST 1 the data path is:

(TXSSEL=1) (cable) (TXMSEL=0) (cable) (RXSEL=0)

XTX -> TXS -> RXS -> TXM -> RXM -> XRX

During TEST 2 the data path is:

(TXMSEL=0) (cable) (TXSSEL=1) (cable) (RXSEL=1)

XTX -> TXM -> RXM -> TXS -> RXS -> XRX

21.2.5 MULTI MFX CONTROL SIGNALS

(1) Setup: Connect shorting plug to MFX IN

Connect shorting plug to MFX OUT

Type: uc

(2) Check that signals *ZTPS (U1/9), WCLKS (U1/15), *ZTPM (U2/5) and WCLKM (U2/11) are clocking and at the same rate. Press any key other than q to swap to fast clocking and recheck signals.

(3) Press q to exit test.

Diagnostic Description

This diagnostic tests the multiplexing of multi MFX port control signals selected via ZTPSEL and WCLKSEL. The *ZTPOUT signal is toggled at the slow rate, and XWCLKO is set to 48kHz (derived from 12.288MHz crystal on ESP-SYN card).

When clocking slowly, ZTPSEL=1 and WCLKSEL=0, and the source of the clock is *ZTPOUT. The path of the clocking is:

(ZTPSEL=1) (cable) (WCLKSEL=0) (cable)

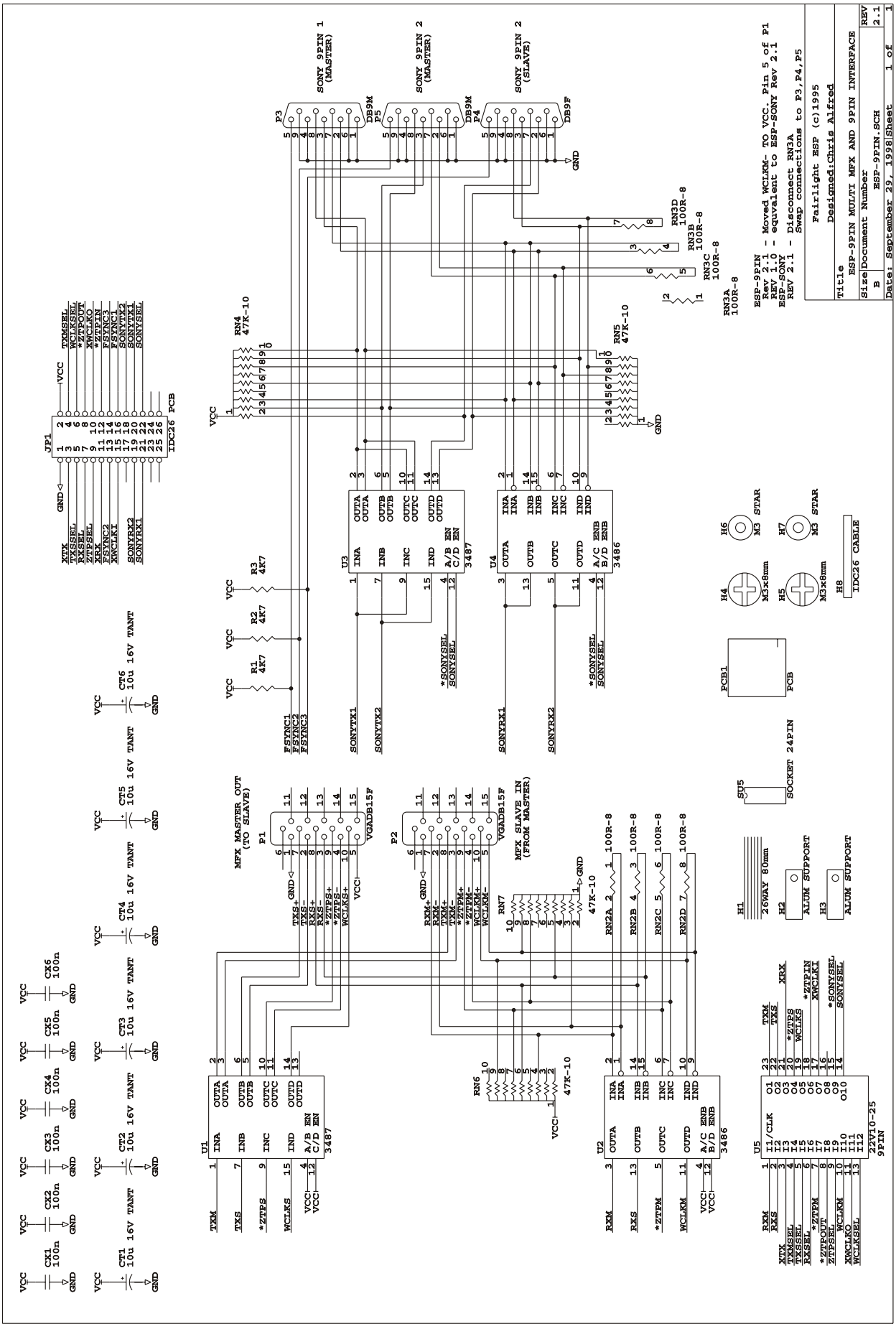
*ZTPOUT -> ZTPIN and ZTPS -> WCLKM -> XWCLKI and WCLKS -> ZTPM

When clocking quickly, ZTPSEL=0 and WCLKSEL=1, and the source of the clock is XWCLKO. The path of the clocking is:

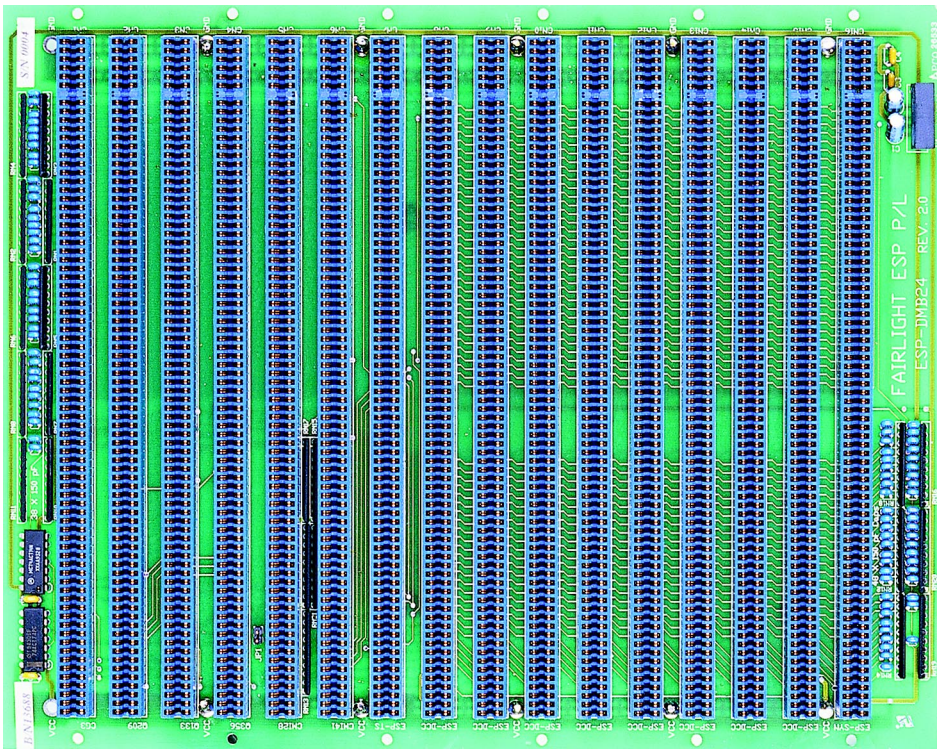
(WCLKSEL=1) (cable) (ZTPSEL=1) (cable)

XWCLKO -> WCLKI and WCLKS -> ZTPM -> ZTPIN and ZTPS -> WCLKM

21.3 ESP9PIN SCHEMATIC



22.0 ESPDMB Digital Mother Board



22.1ESPDMB Description

22.1.1 Introduction

The ESP-DMB8 is a non-expandable mother board with 2 slots for ESP-DCC Digital Channel Cards to provide 8 tracks of disk-recording. The ESP-DMB24 has 8 slots for ESP-DCCs; 6 are required for 24 tracks of disk-recording, and the other 2 are future expansion slots.

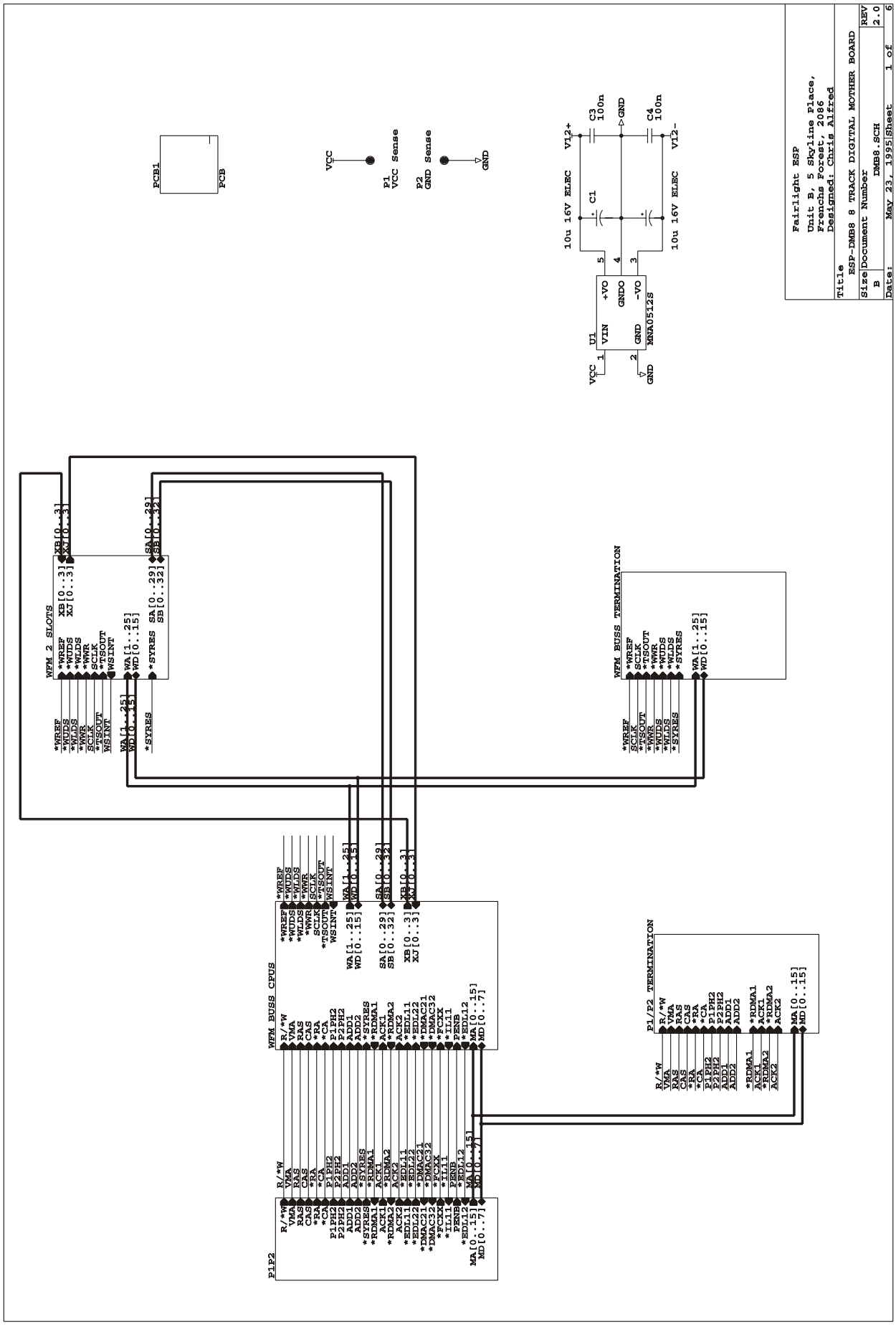
The ESP-DMB8 has 10 slots labelled 1 to 10 (connectors CN1 to 10 respectively) starting from the right hand side as viewed from the component side.

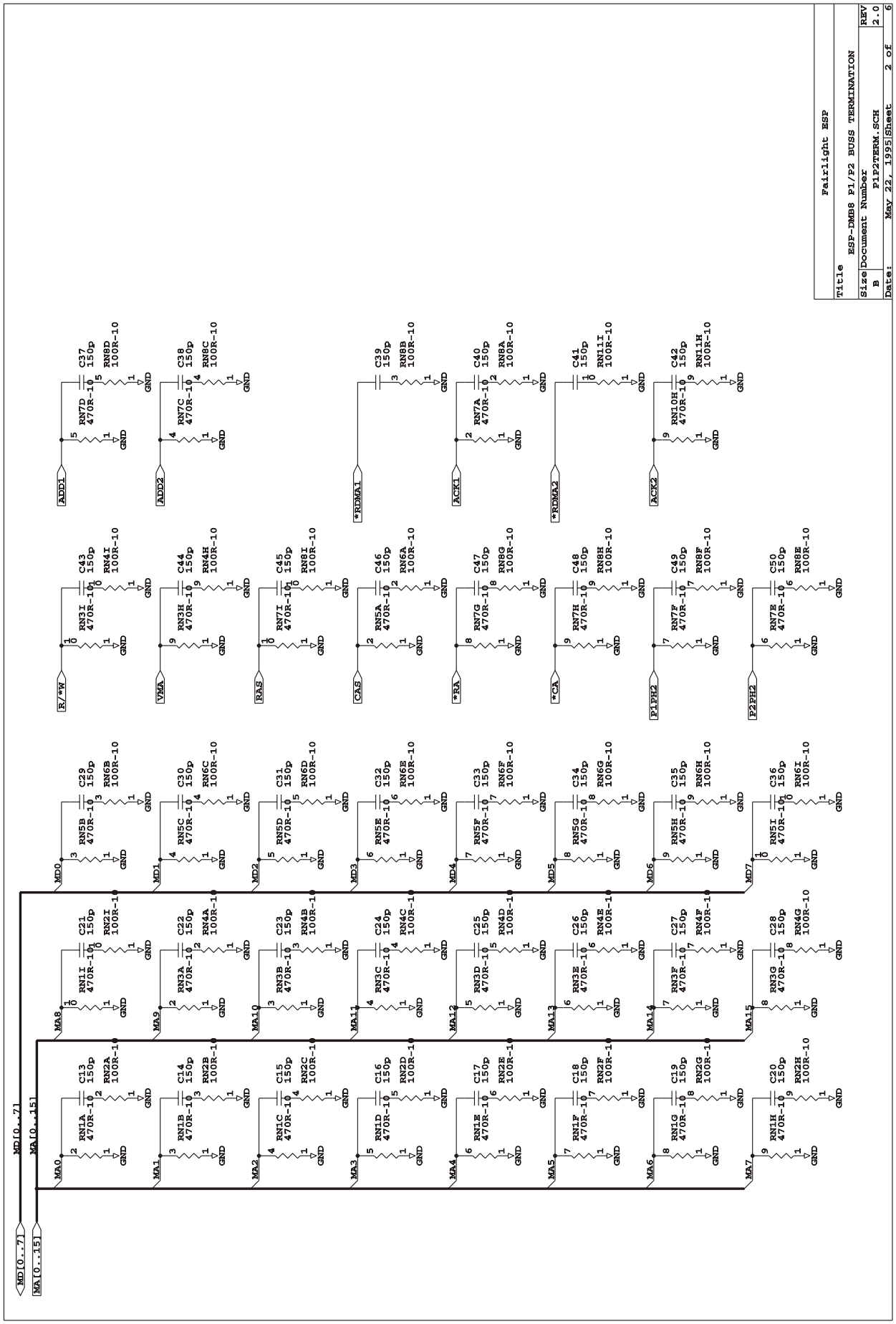
The ESP-DMB24 has 16 slots labelled 1 to 16 (connectors CN1 to 16 respectively) starting from the right hand side as viewed from the component side.

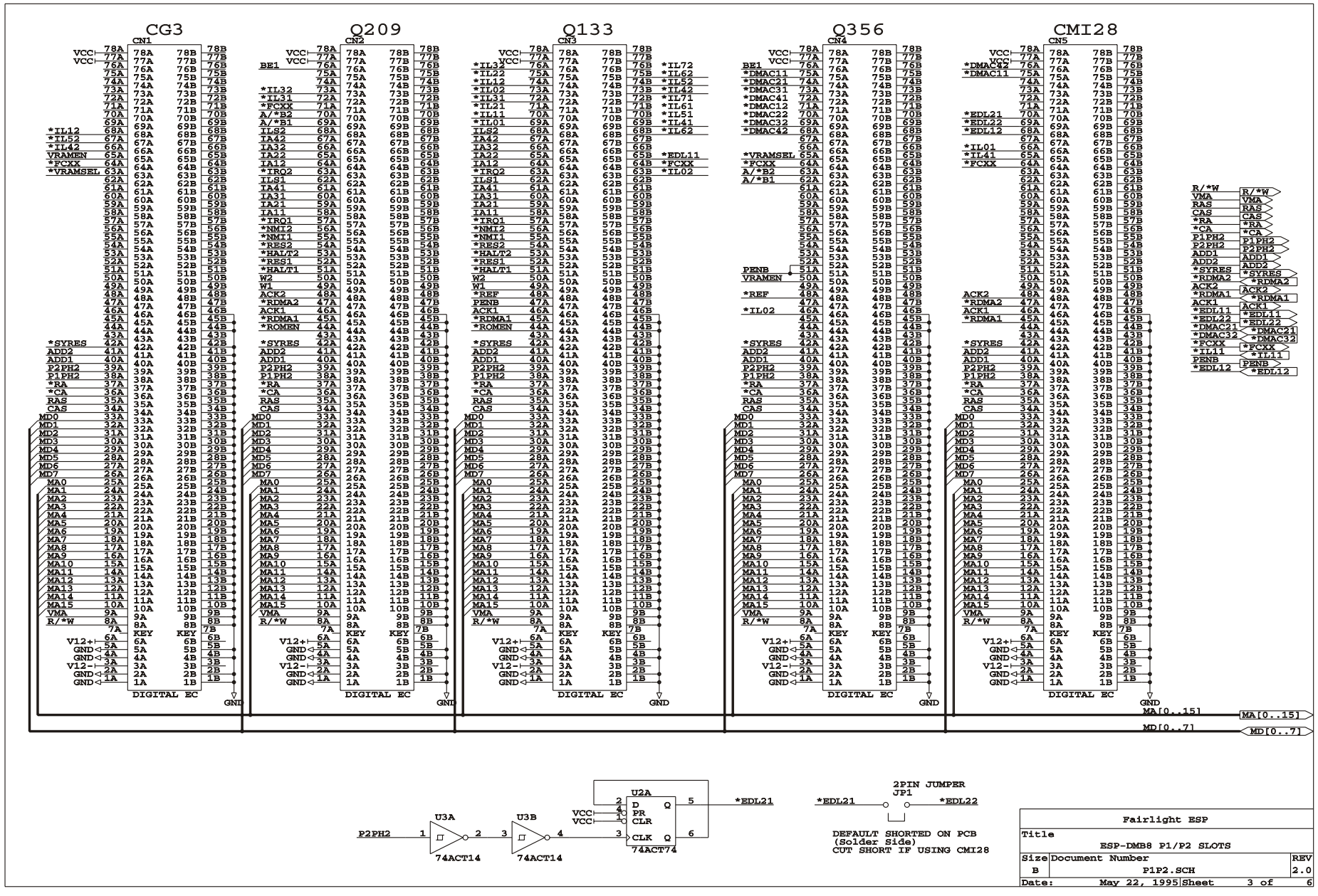
22.1.2 Power supply

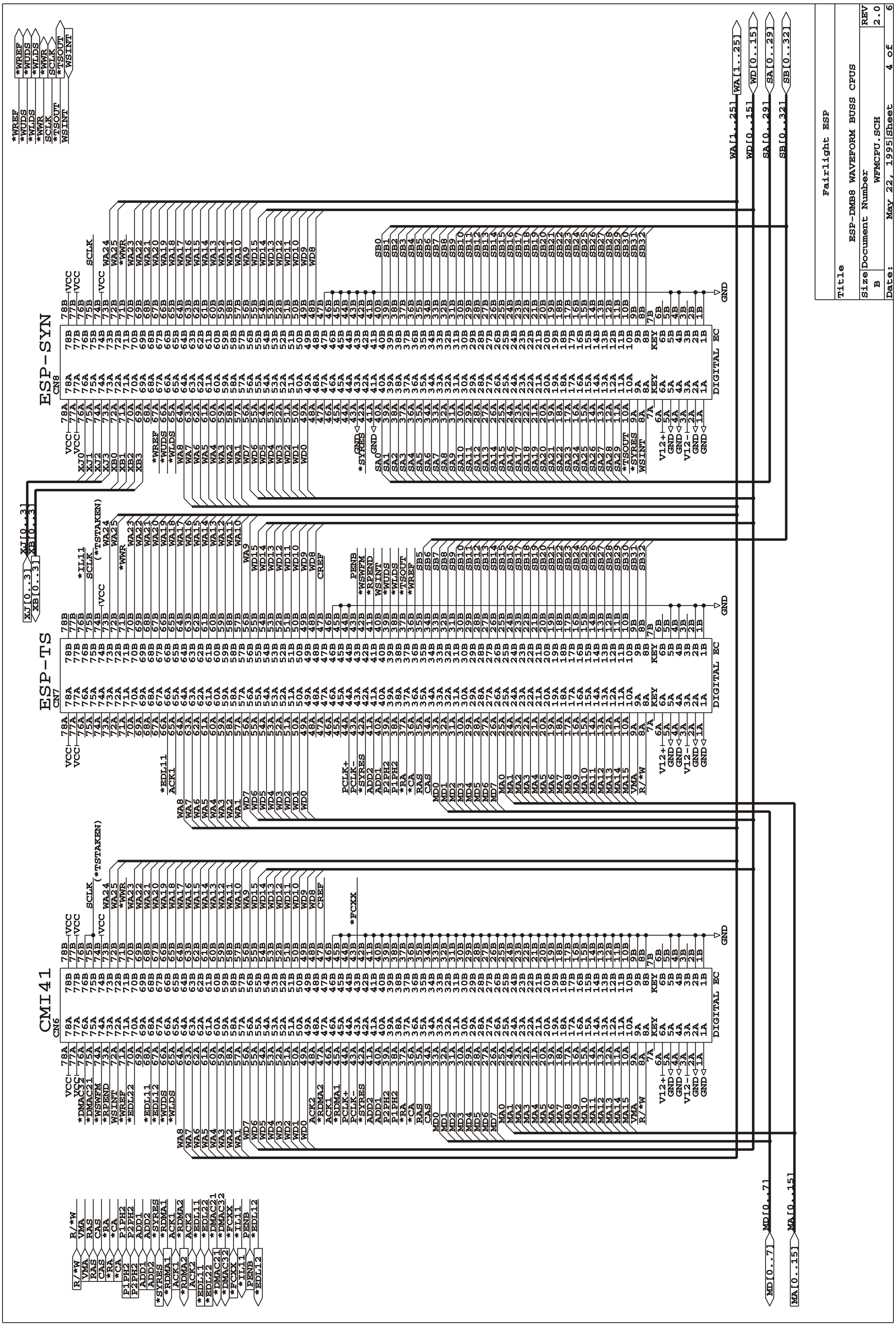
The ESP-DMB8 and ESP-DMB24 only require +5V, U1 is a DC-DC converted used to generate +12,-12.

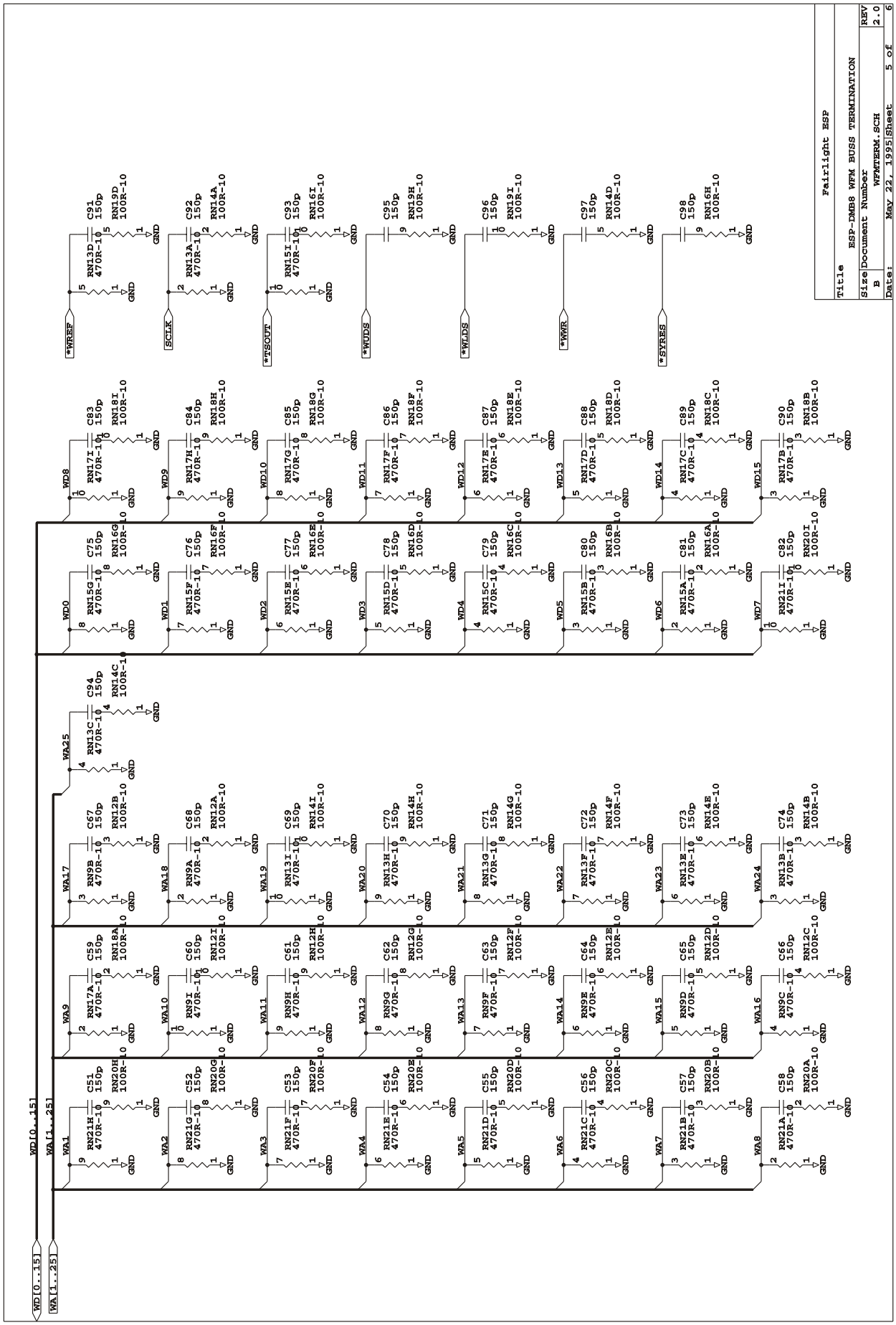
22.2 ESPDMB8 SCHEMATICS




Fairlight ESP
Title
ESP-DMB8 P1/P2 BUSS TERMINATION
Size B
Document Number P1P2TERM.SCH
REV 2.0
Date: May 22, 1995 Sheet 2 of 6
MD[0..7]
MA[0..15]
ADD1
ADD2
*RDMA1
ACK1
*RDMA2
ACK2
R/*W
VMA
RAS
CAS
*RA
*CA
P1PH2
P2PH2
GND


CG3
CN1
Q209
CN2
Q133
CN3
Q356
CN4
CMI28
CN5
DIGITAL EC
GND
*SYRES
ADD2
ADD1
P2PH2
P1PH2
*RA
*CA
RAS
CAS
MD0
MD1
MD2
MD3
MD4
MD5
MD6
MD7
MA0
MA1
MA2
MA3
MA4
MA5
MA6
MA7
MA8
MA9
MA10
MA11
MA12
MA13
MA14
MA15
VMA
R/*W
*IL12
*IL52
*IL42
VRAMEN
*FCXX
*VRAMSEL
*IL72
*IL62
*IL52
*IL42
*IL71
*IL61
*IL51
*IL41
*IL62
*EDL11
*FCXX
*IL02
*DMAC42
*DMAC11
*EDL22
*EDL12
*IL01
*IL41
*FCXX
MA[0..15]
MD[0..7]
U2A
U3A
U3B
74ACT14
74ACT74
P2PH2
*EDL21
*EDL22
2PIN JUMPER
JP1
DEFAULT SHORTED ON PCB
(Solder Side)
CUT SHORT IF USING CMI28
Fairlight ESP
ESP-DMB8 P1/P2 SLOTS
P1P2.SCH
May 22, 1995
Sheet 3 of 6


CMI41
CN6
ESP-TS
CN7
ESP-SYN
CN8
DIGITAL EC
Fairlight ESP
Title
ESP-DMB8 WAVEFORM BUSS CPUS
Size
Document Number
REV
B
WFMCPU.SCH
2.0
Date:
May 22, 1995
Sheet
4 of
6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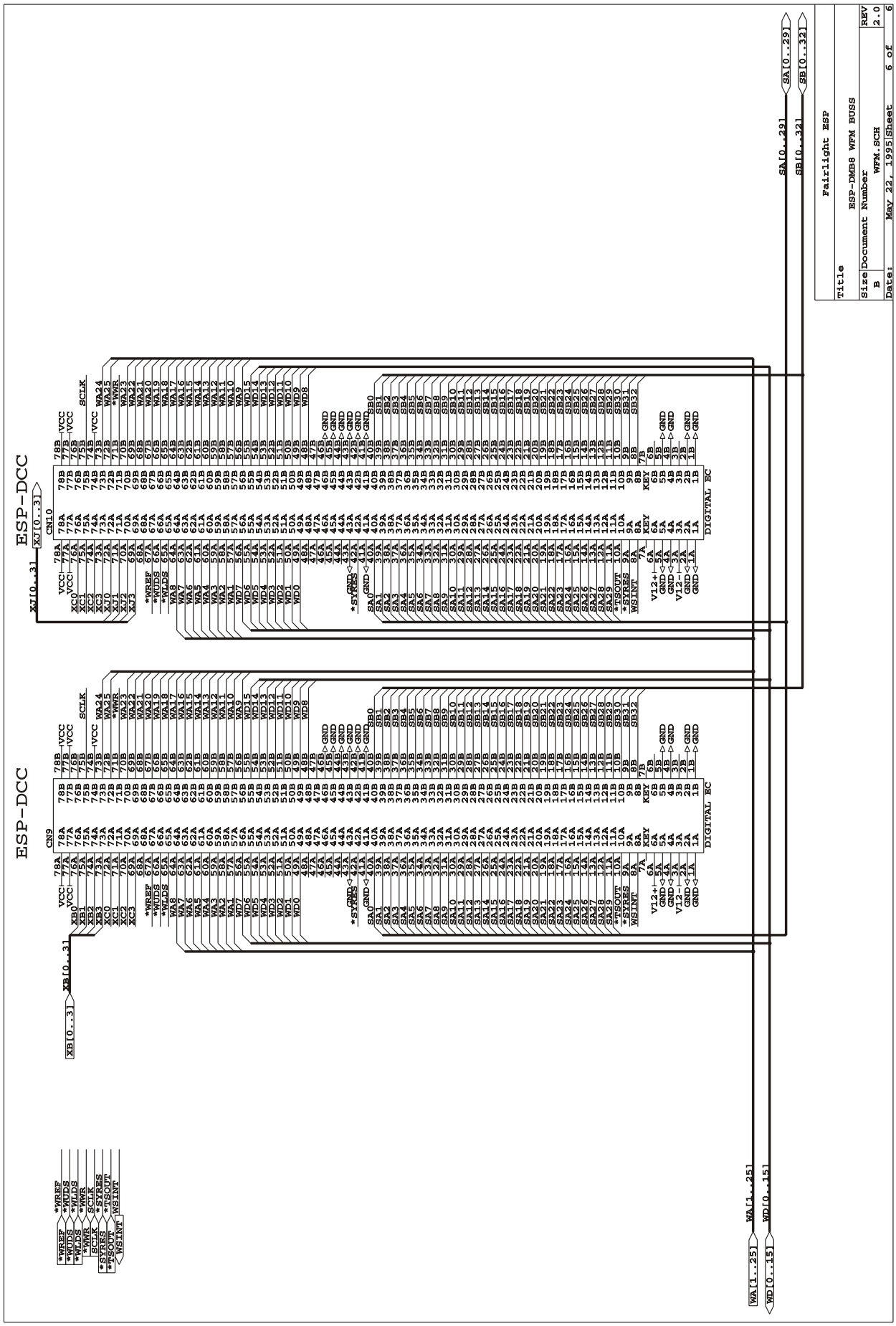
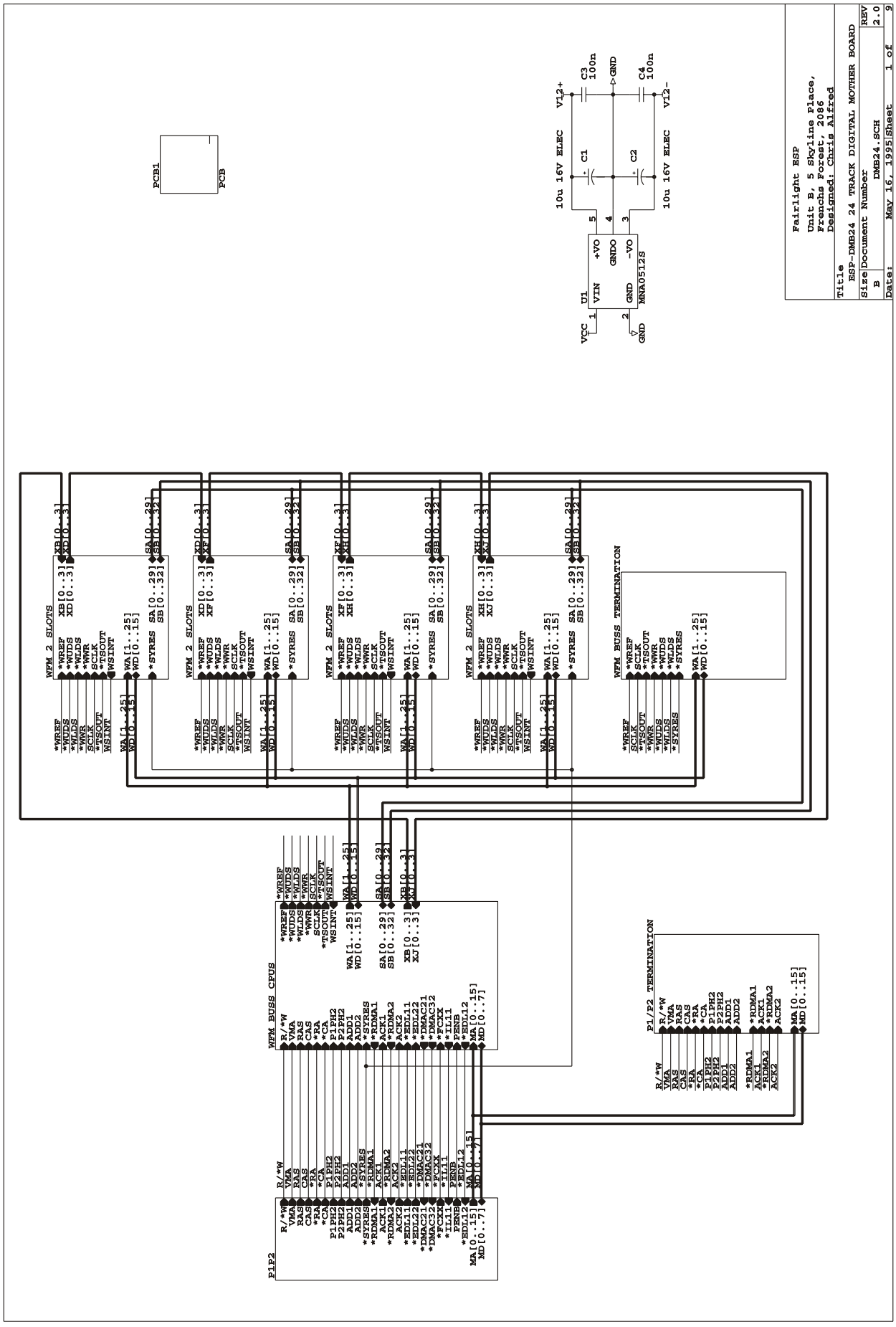
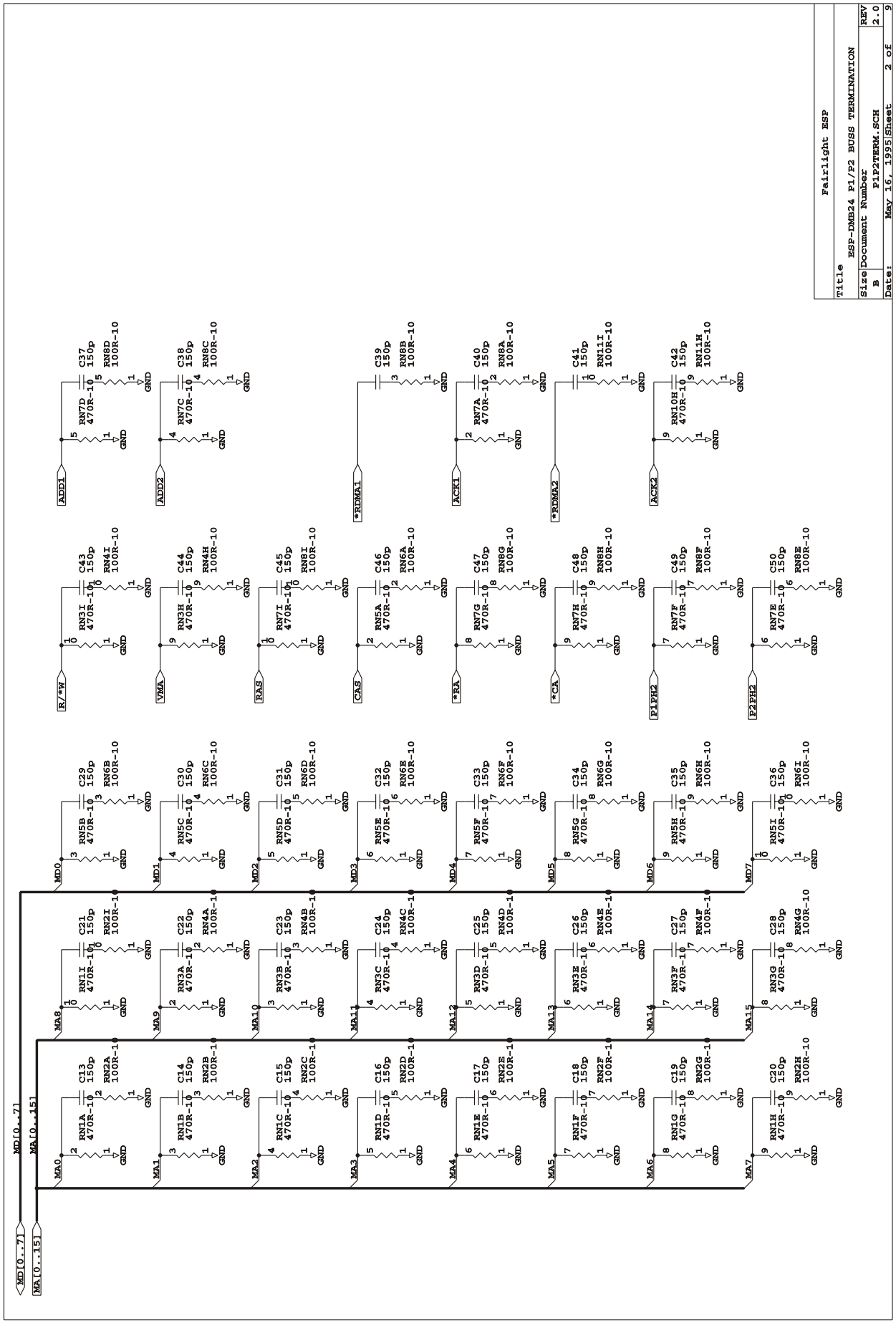
ESP-DMB8 WFM BUSS TERMINATION
Size Document Number REV
B WFMTERM.SCH 2.0
Date: May 22, 1995 Sheet 5 of 6
WD[0..15]
WA[1..25]
*WREF
SCLK
*TSOUT
*WUDS
*WLDS
*WWR
*SYRES
GND


ESP-DCC
ESP-DCC
Fairlight ESP
Title
ESP-DMB8 WFM BUSS
Size
B
Document Number
WFM.SCH
REV
2.0
Date:
May 22, 1995
Sheet
6 of
6
DIGITAL EC
XB[0..31]
XA[0..31]
SA[0..29]
SB[0..32]
WA[1..25]
WD[0..15]
*WREF
*WDDS
*WDS
*WWR
SCLK
*SYRES
*YSOUT
WSINT

22.3 ESPDMB24 SCHEMATICS

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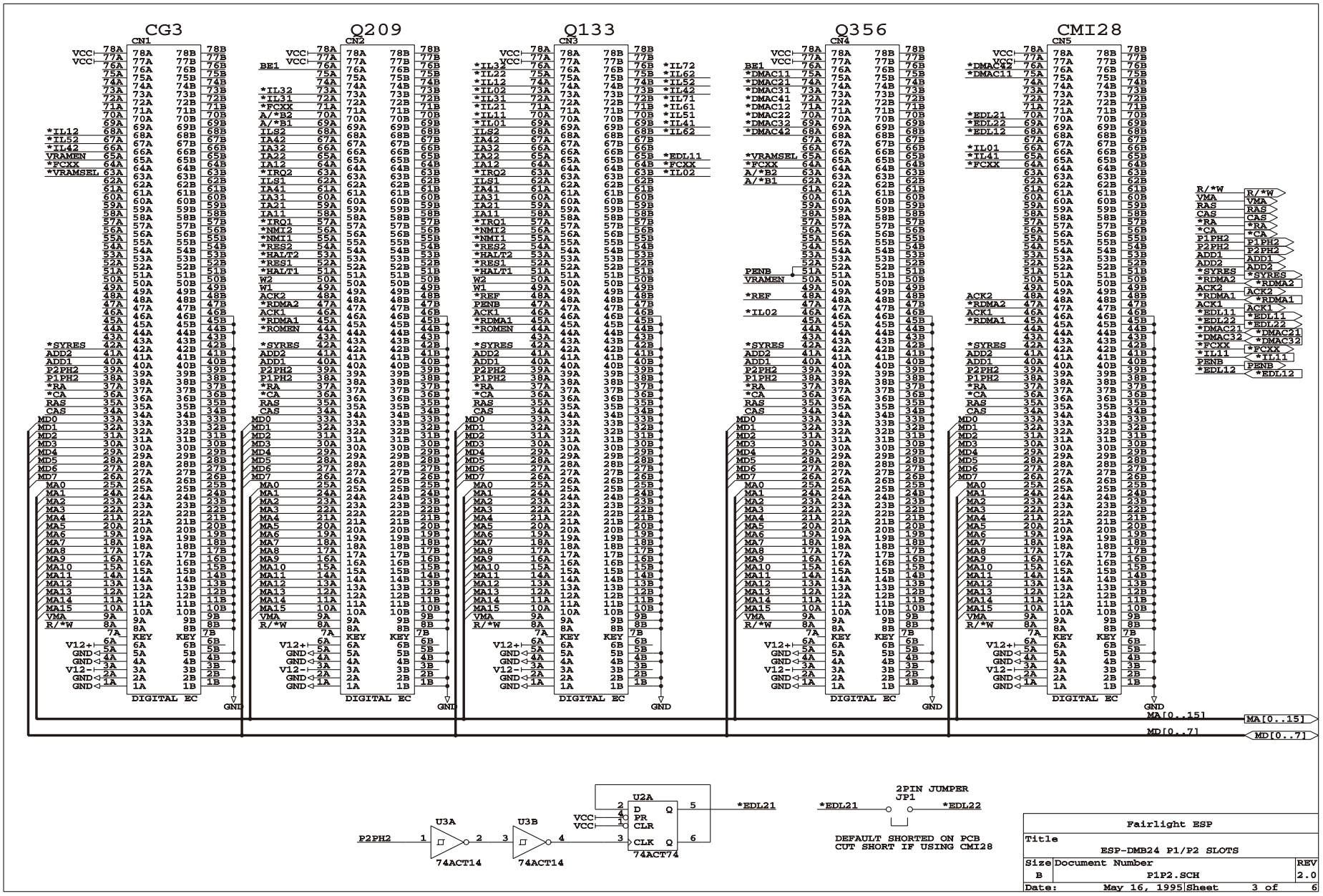
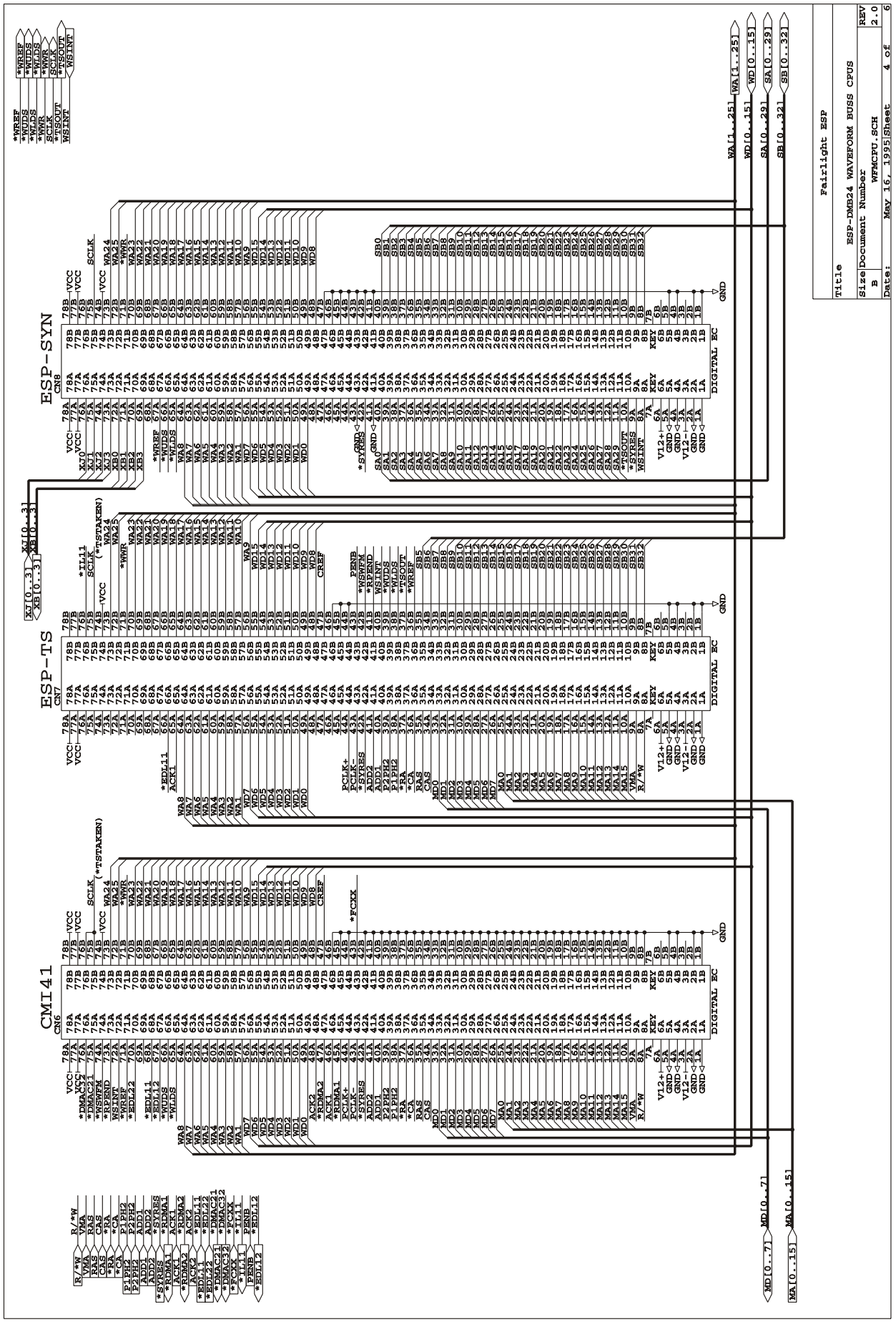
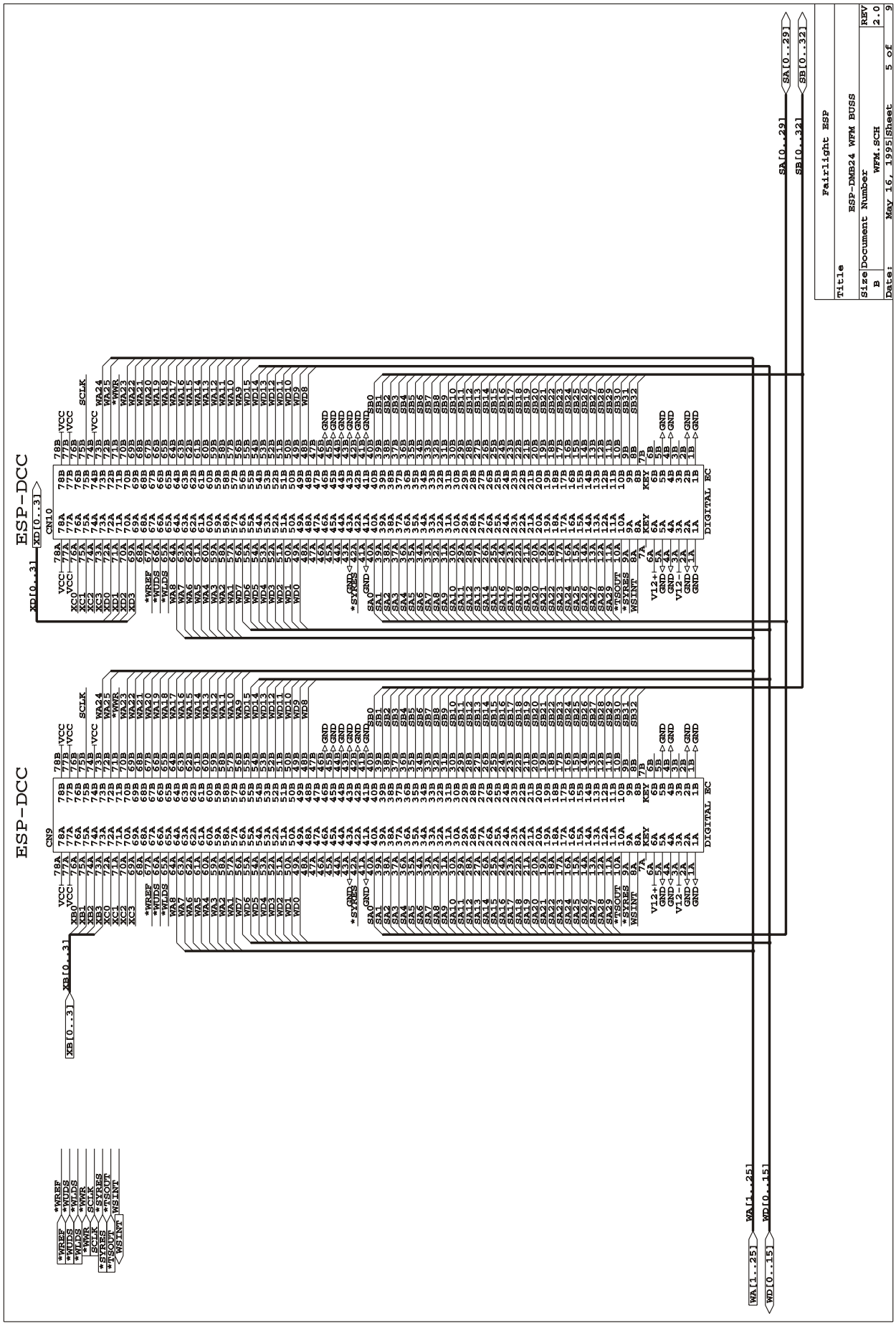
ESP-DMB24 P1/P2 BUSS TERMINATION
Size B
Document Number P1P2TERM.SCH
REV 2.0
Date: May 16, 1995 Sheet 2 of 9
MD[0..7]
MA[0..15]
ADD1
ADD2
*RDMA1
ACK1
*RDMA2
ACK2
R/*W
VMA
RAS
CAS
*RA
*CA
P1PH2
P2PH2
GND


CG3
CN1
Q209
CN2
Q133
CN3
Q356
CN4
CMI28
CN5
DIGITAL EC
GND
MA[0..15]
MD[0..7]
U2A
74ACT74
U3A
74ACT14
U3B
74ACT14
P2PH2
*EDL21
2PIN JUMPER
JP1
*EDL22
DEFAULT SHORTED ON PCB
CUT SHORT IF USING CMI28
Fairlight ESP
ESP-DMB24 P1/P2 SLOTS
P1P2.SCH
May 16, 1995
3 of 6


CMI41
ESP-TS
ESP-SYN
Fairlight ESP
Title
ESP-DMB24 WAVEFORM BUSS CPUS
Size
B
Document Number
WFMCPU_SCH
REV
2.0
Date:
May 16, 1995
Sheet
4 of 6


ESP-DCC
ESP-DCC
Fairlight ESP
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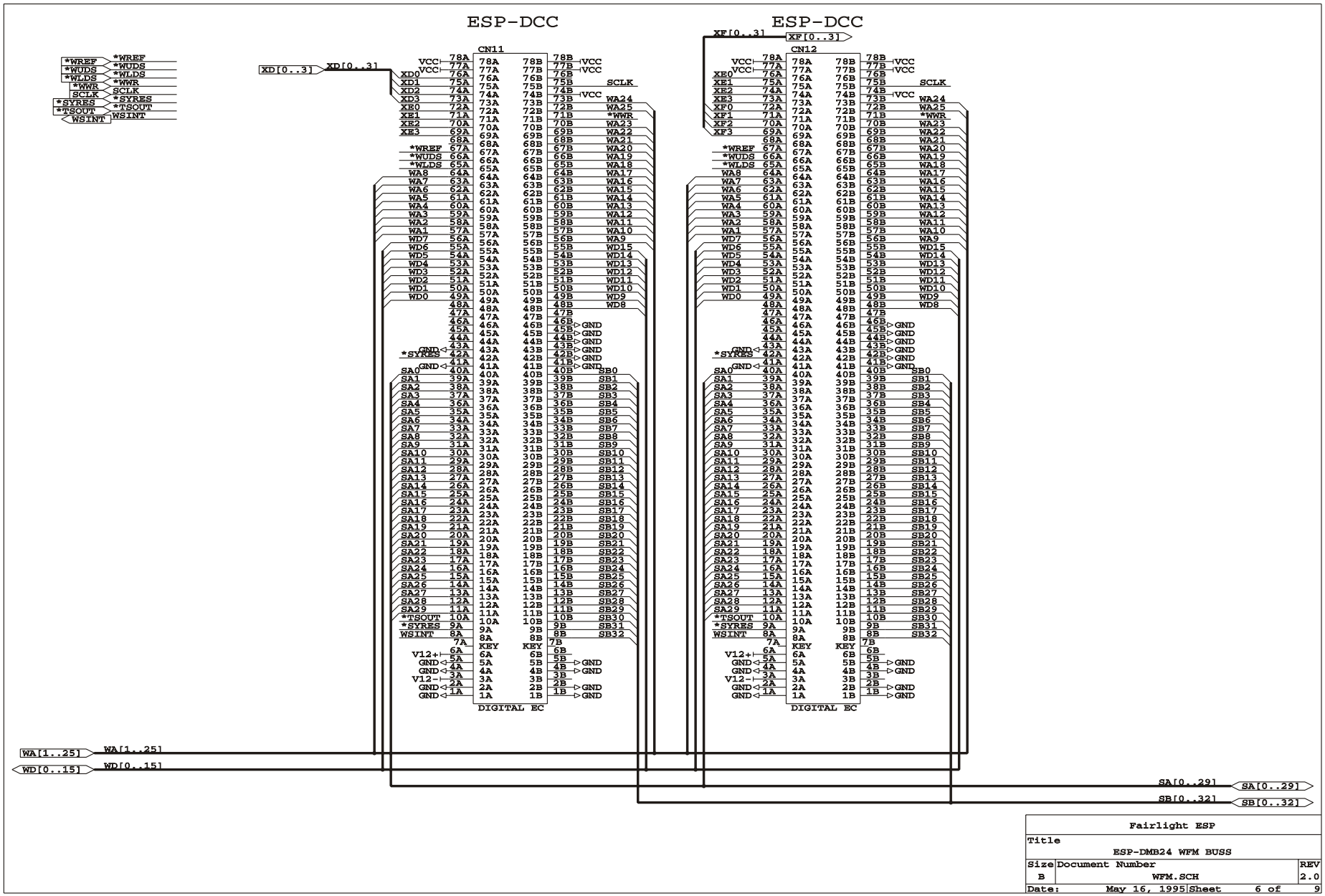
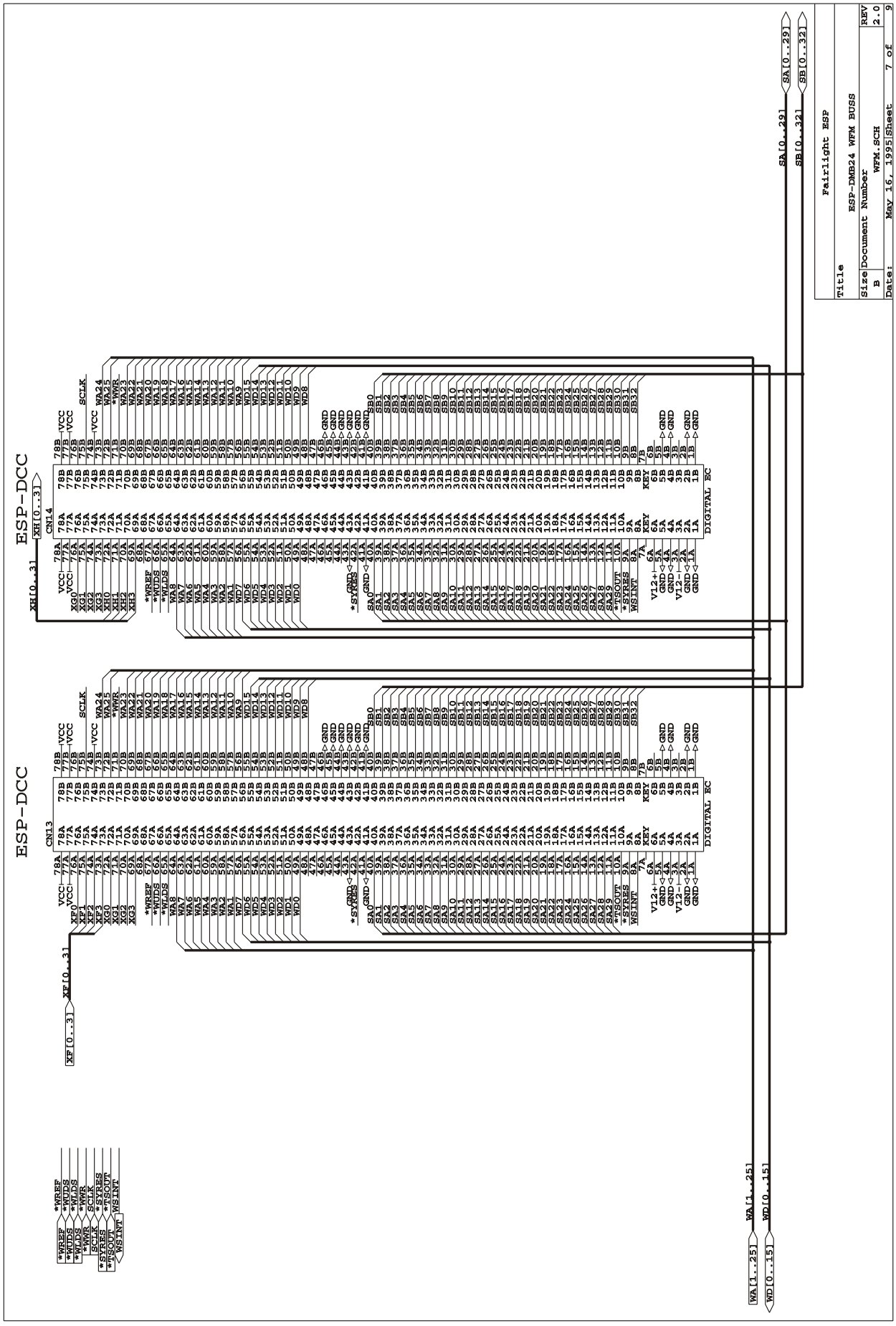
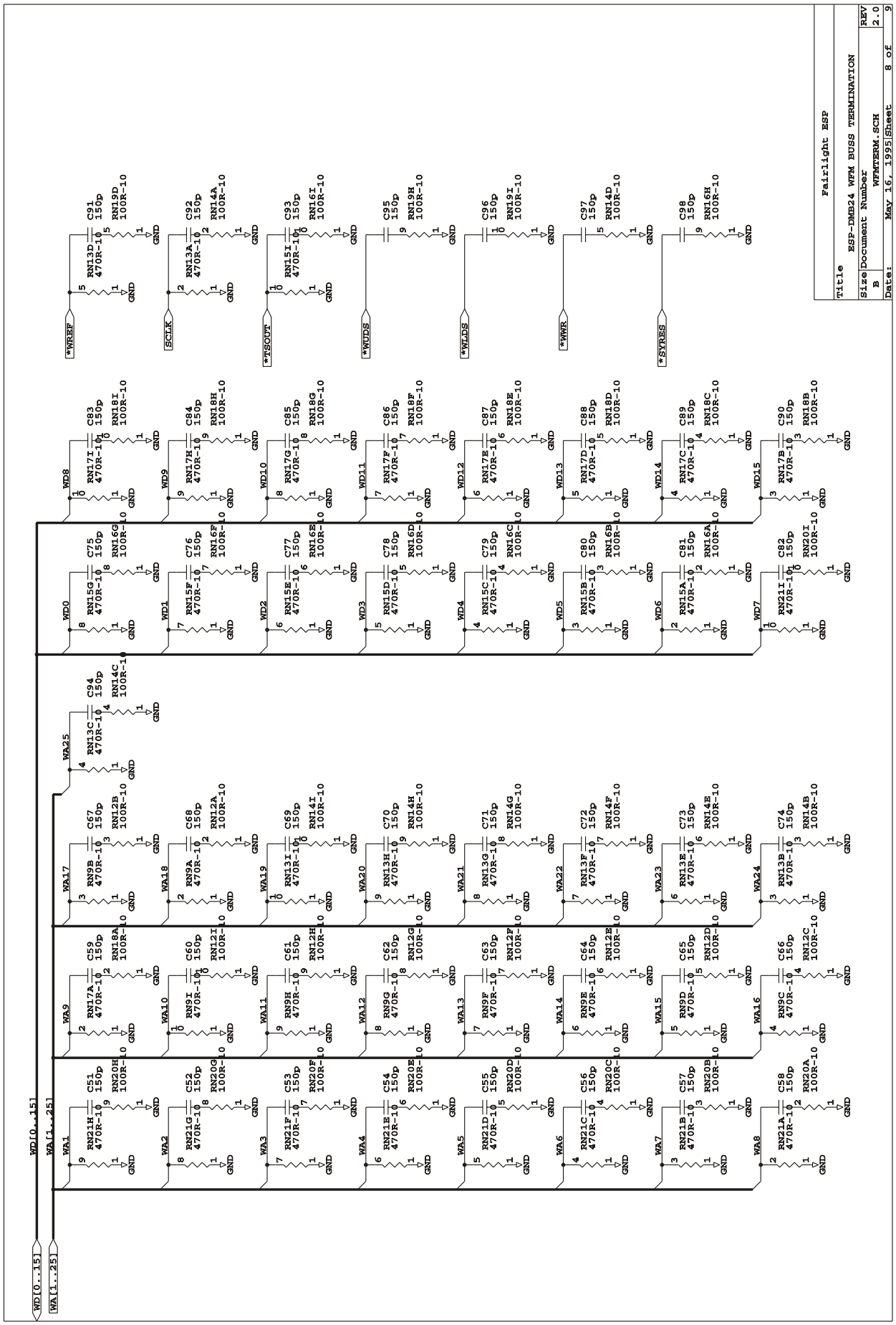
ESP-DMB24 WFM BUSS
Size Document Number REV
B WFM.SCH 2.0
Date: May 16, 1995 Sheet 5 of 9


ESP-DCC
CN11
DIGITAL EC
ESP-DCC
CN12
DIGITAL EC
*WREF
*WUDS
*WLDS
*WWR
SCLK
*SYRES
*TSOUT
WSINT
XD[0..3]
XF[0..3]
WA[1..25]
WD[0..15]
SA[0..29]
SB[0..32]
VCC
GND
V12+
V12-
KEY
Fairlight ESP
Title
ESP-DMB24 WFM BUSS
Size B
Document Number WFM.SCH
REV 2.0
Date: May 16, 1995 Sheet 6 of 9


ESP-DCC
ESP-DCC
Fairlight ESP
Title
ESP-DMB24 WFM BUSS
Size
B
Document Number
WFM.SCH
REV
2.0
Date:
May 16, 1995
Sheet
7 of
9
XF[0..31]
CN13
CN14
DIGITAL EC
SA[0..29]
SB[0..32]
WA[1..25]
WD[0..15]
*WREF
*WVDS
*WLDS
*WWR
SCLK
*SYRES
*MSOUT
WSINT


Fairlight ESP
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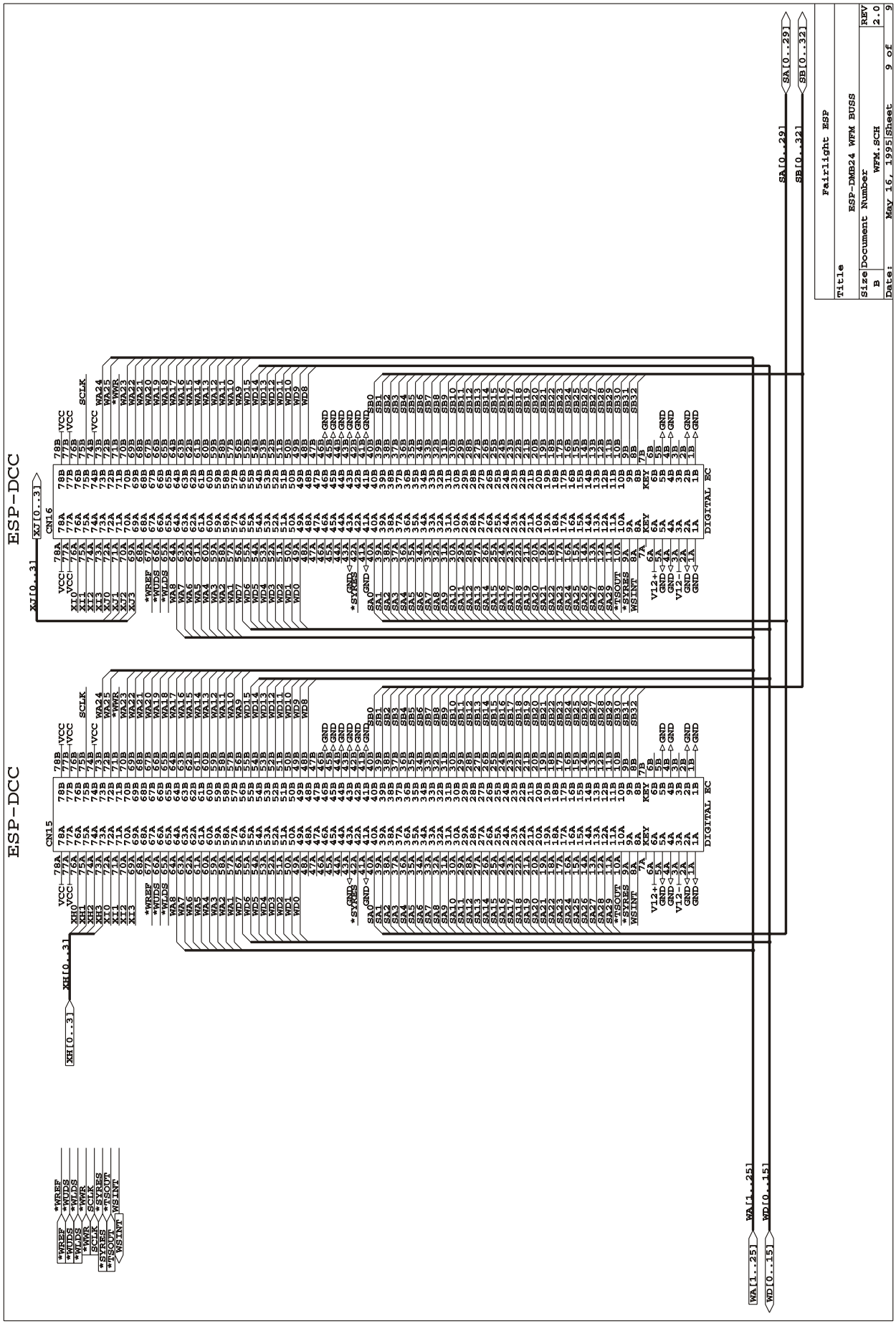
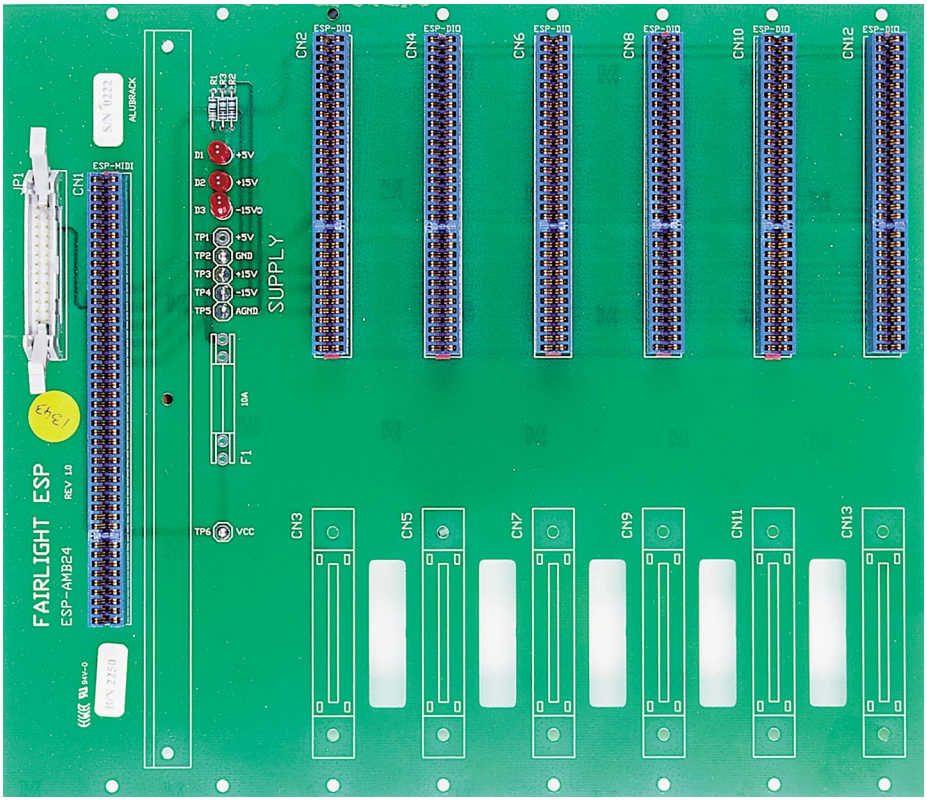
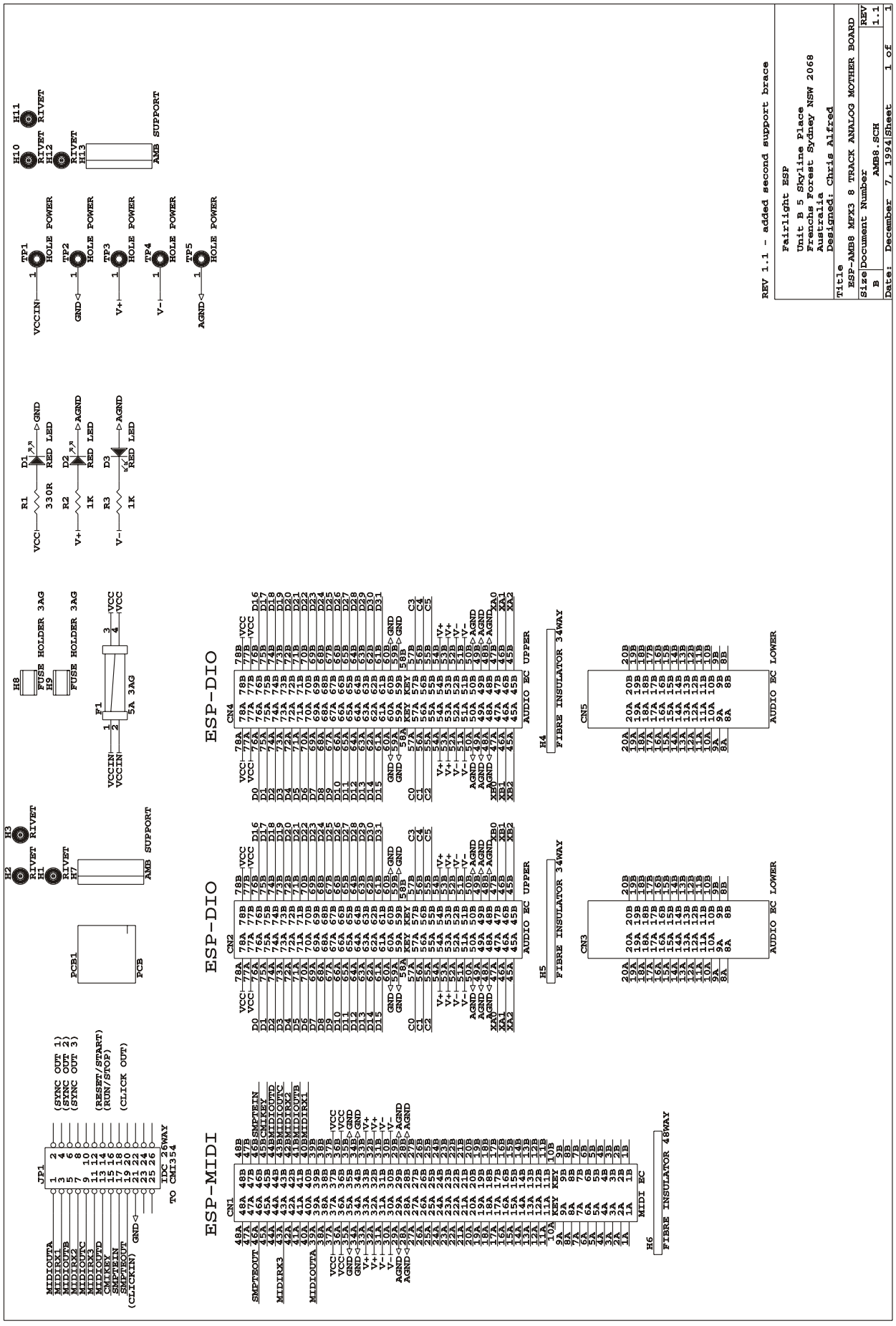
ESP-DMB24 WFM BUSS TERMINATION
Size B
Document Number WFMTERM.SCH
REV 2.0
Date: May 16, 1995 Sheet 8 of 9
WD[0..15]
WA[1..25]
*WRSF
SCLK
*TSOUT
*WUDS
*WLDS
*WWR
*SYRES
GND


ESP-DCC
ESP-DCC
Fairlight ESP
Title
ESP-DMB24 WFM BUSS
Size
B
Document Number
WFM.SCH
REV
2.0
Date:
May 16, 1995
Sheet
9 of
9
SA[0..29]
SB[0..32]
XH[0..31]
XF[0..31]
WA[1..25]
WD[0..15]
CN15
CN16
DIGITTAL EC
KEY
*WREF
*WDDS
*WLDS
*WWR
SCLK
*SYRES
*TSOUT
WSINT

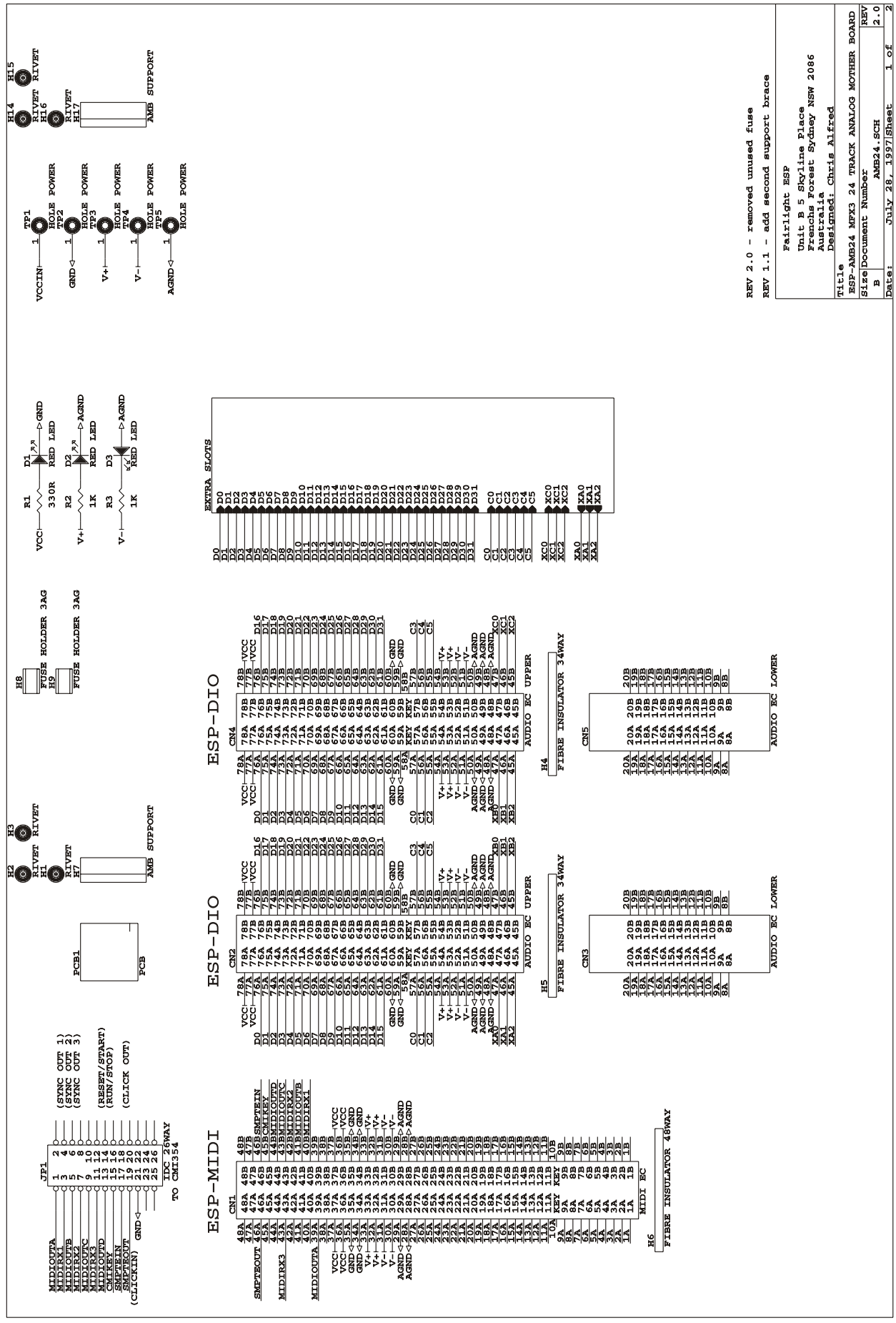
23.0 ESPAMB Analogue Mother Board



23.1 AMB8 SCHEMATICS

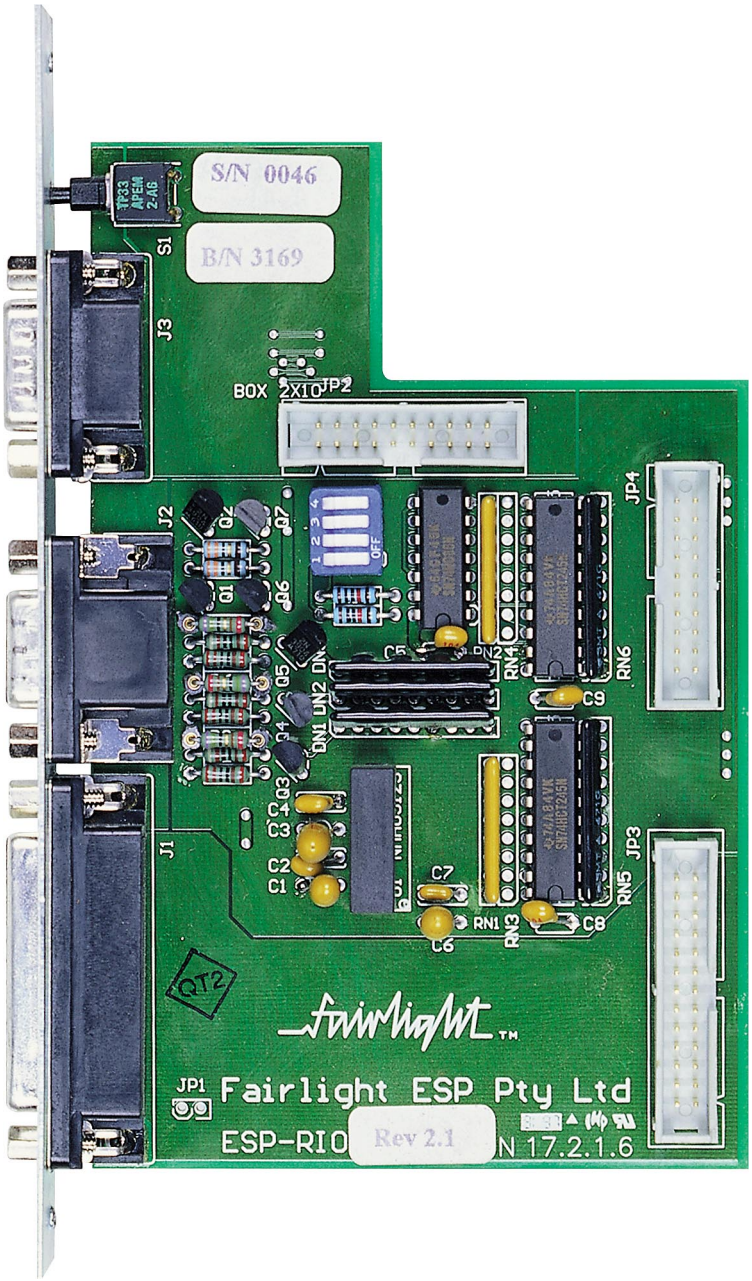


23.2 AMB24 SCHEMATICS

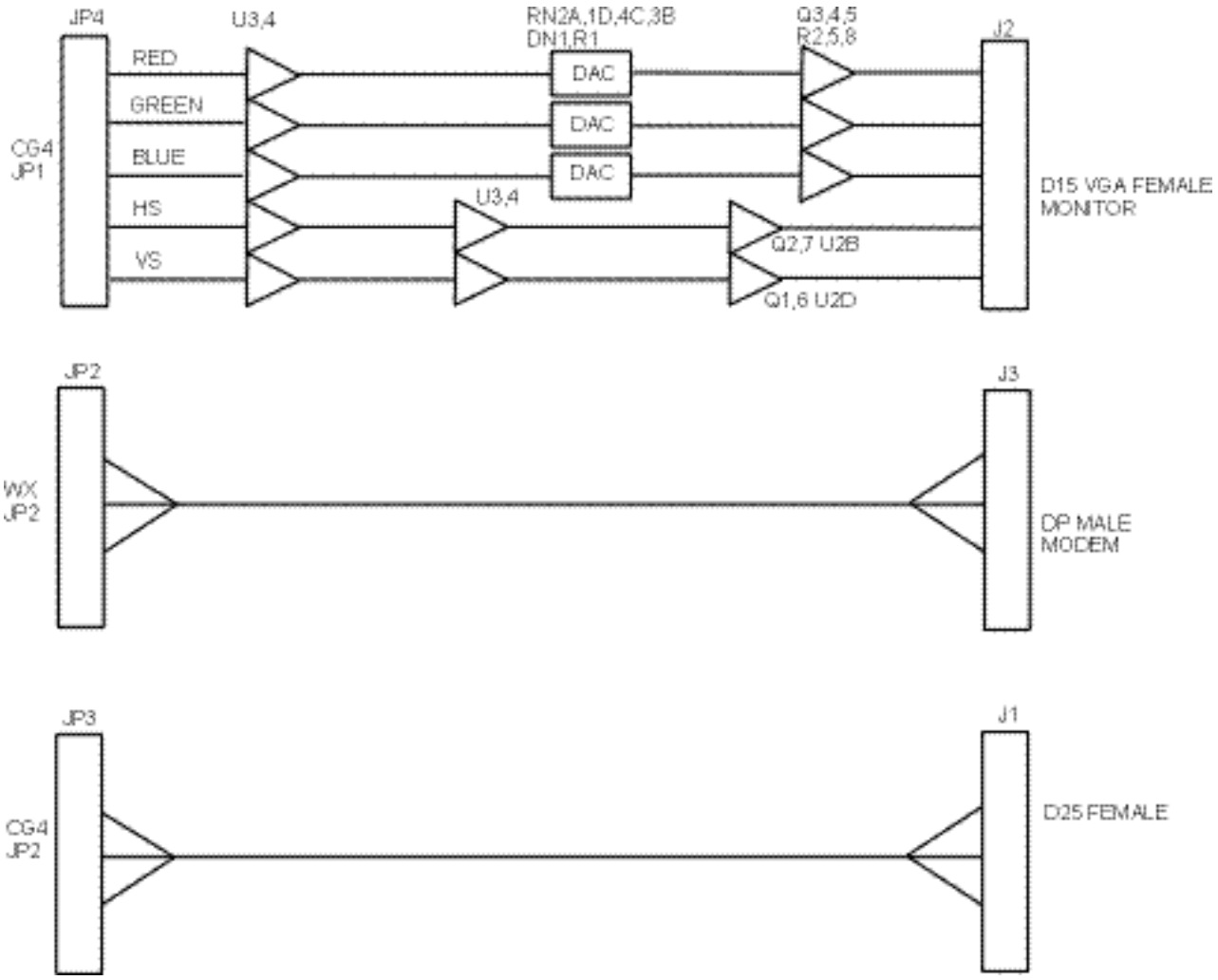


ESP-DIO
CN6
CN8
CN10
CN12
H11
H10
H13
H12
FIBRE INSULATOR 34WAY
AUDIO EC UPPER
AUDIO EC LOWER
CN7
CN9
CN11
CN13
Fairlight ESP
Designed: Chris Alfred
Title
ESP-AMB24 EXTRA SLOTS
Size
Document Number
REV
B
SLOTS.SCH
1.1
Date: October 17, 1995
Sheet 2 of 2

24.0 ESPRIO Rear I/O Card



24.1 ESPRIO Block Diagram



24.2 ESPRIO Description

The RIO rear I/O card provides a mounting system for the I/O ports of the WX and CG4. It also incorporates the circuitry and functionality of the ESP-RGB board (which is no longer required). The I/O devices on the RIO are; the WX reset switch, the WX modem port, the CG4 RGB output and the CG4 HSSL port.

24.2.1 Installation

The RIO is mounted at the rear of the machine on the Rear Plug Assembly. Three cables connect the ESP-RIO to ESP-WX and ESP-CG4; a 20 way IDC cable from JP1 on CG4 to JP4 of ESP-RIO, a 26 way IDC cable from JP2 of CG4 to JP2 of RIO and another 20 way IDC cable from JP2 of ESP-WX to JP2 of RIO.

24.2.2 Operation

The RIO board consists of three main sections which handle the HSSL, the serial port and reset switch and graphics driver section.

The HSSL subsection consists of a 26 way IDC connector, JP3, and the HSSL output connector J1. In a similar manner, the serial port/reset switch subsection consists of the 20 way IDC connector JP4, switch S1 and connector J3.

24.2.3 Graphics Driver Section

The graphics driver section obtains +5 volts and GND supply from the CG4 via connector JP4. In addition it uses the DC-DC converter U1 to generate the +/-12 volts required for the analogue line driver circuitry.

For each colour of red, green and blue, RIO receives a three bit binary code for the colour intensity RED[0..3], GRN [0..3] and BLU[0..3]. These signals are buffered by U3 and U4, with the buffered versions of the red, green and blue binary code bits being fed directly into the DAC (digital to analogue converter) for each colour. The DAC for the colour red consists of RN2A, RN1D, RN4C, RN3B, the diode array DN1 and the resistor R1. As can be seen from the schematic, similar circuitry exists for the colours green and blue. Transistors Q3, Q4 and Q5 in conjunction with R2, R5 and R8 provide line buffers for the analogue voltages appearing across R1, R4 and R7.

The vertical and horizontal sync signals HS and VS from the CG4 are also buffered by U3 and U4 before being fed into switchable inverters (U2A and U2C) and finally into the totem pole drivers consisting of Q2, Q7 and U2B for the horizontal sync pulse and Q1, Q6 and U2D for the vertical sync pulse.

24.2.4 Testing and Diagnostics

The ESP-RIO should have all three cables connected between it and the WX and CG4 for proper testing. The HSSL portion of the RIO card should be tested using an external D25 way loopback plug (described below) using the HSSLTEST Serial port test program.

The RGB DAC portion of RIO should be tested using the CG4TEST program with the output being displayed on a monitor. CG4TEST has recently been updated with a display screen which shows the sixteen possible shades of red, green and blue.

24.2.5 HSSL External Loopback plug

An external loopback plug can be made using a male solder bucket 25 way D connector (ie Farnell 150-810). The following connections should then be made on this connector :

Pin 2 <—> Pin 8

Pin 3 <—> Pin 9

Pin 4 <—> Pin 10

Pin 5 <—> Pin 11

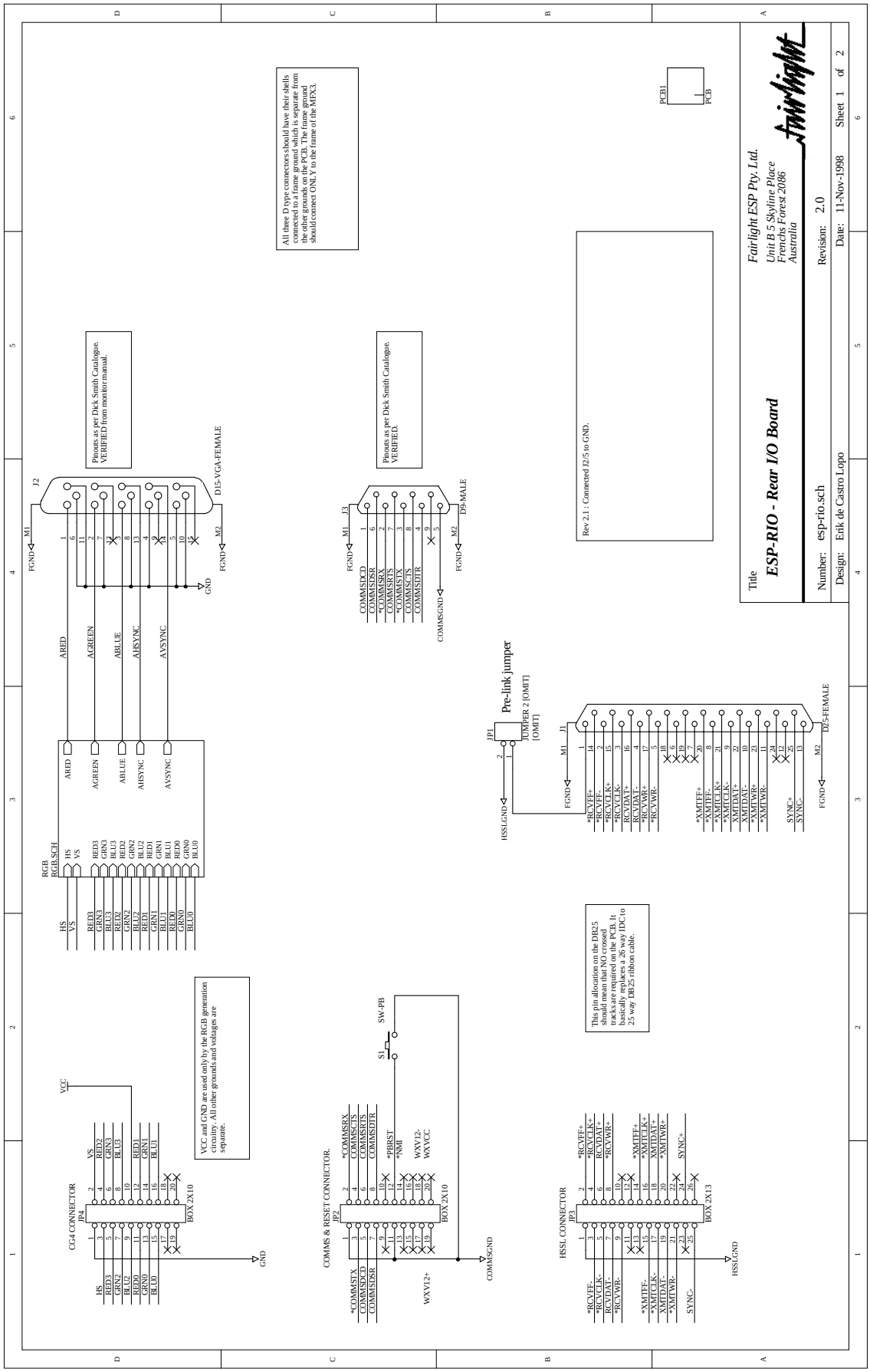
Pin 14 <—> Pin 20

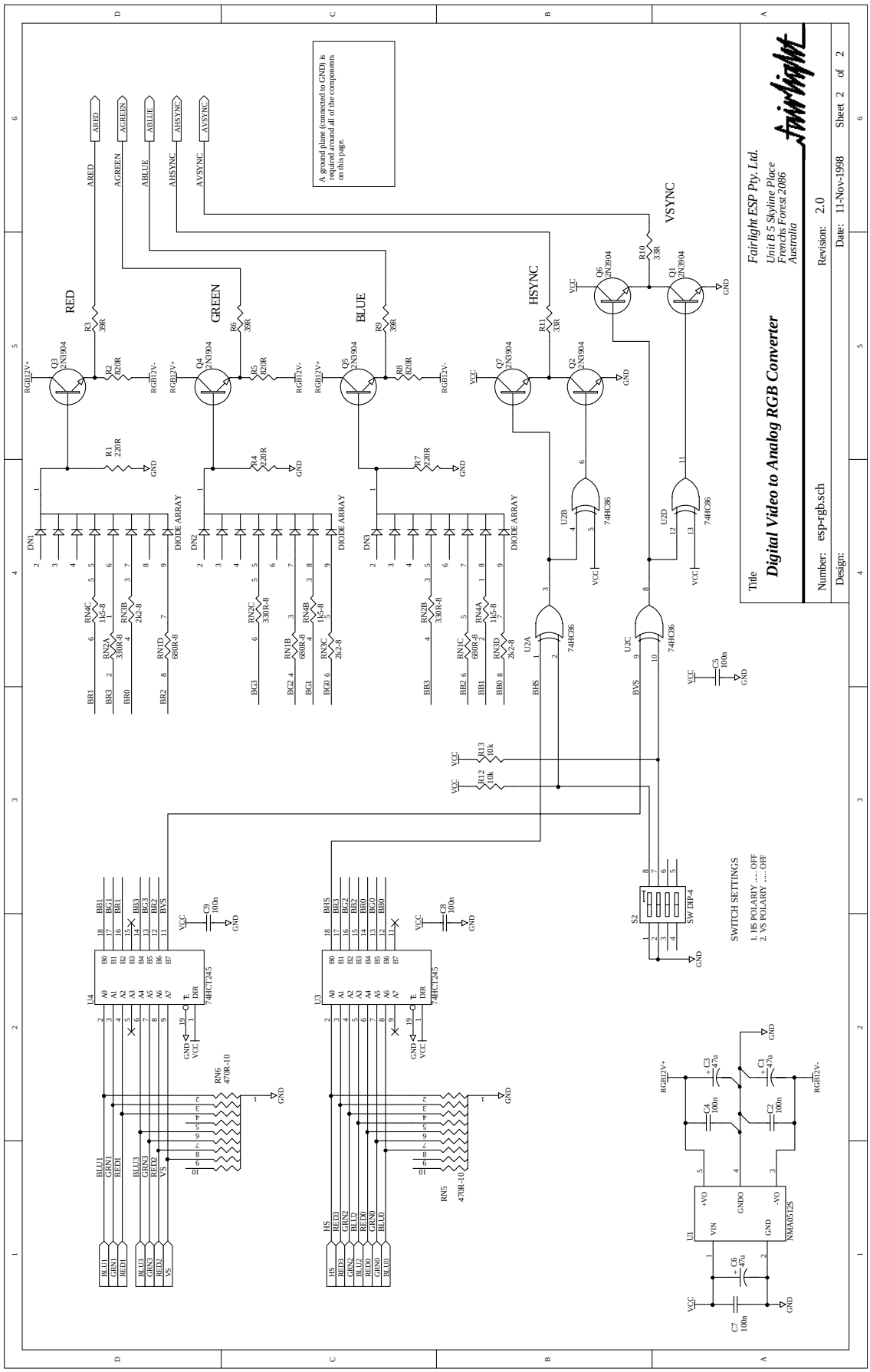
Pin 15 <—> Pin 21

Pin 16 <—> Pin 22

Pin 17 <—> Pin 23

24.3 ESPRIO SCHEMATICS




Title
Digital Video to Analog RGB Converter
Fairlight ESP Pty. Ltd.
Unit B 5 Skyline Place
French's Forest 2086
Australia
Number: esp-rgb.sch
Revision: 2.0
Design:
Date: 11-Nov-1998
Sheet 2 of 2
A ground plane (connected to GND) is required around all of the components on this page.
RED
GREEN
BLUE
HSYNC
VSYNC
SWITCH SETTINGS
1. HS POLARITY ..... OFF
2. VS POLARITY ..... OFF
74HC86
74HCT245
SW DIP-4
DIODE ARRAY
NMA0505DS

25.0 MFX Console

25.1 MFX010 Conroller Card Description

The MFX keyboard is a console designed to facilitate the use of post-production software on the MFX.

The MFX keyboard contains two circuit boards. MFX010 is the controller board for the MFX console, containing the Microprocessor. The other board, MFK, is used to decode the switches and trigger keys.

25.1.1 68000 Master Processor

(refer schematic MFX010-CPU (page 2 of 8))

The 68000 is responsible for the processing tasks in the MFX as it handles every task including scanning the 24 trigger keys. It has ROM, RAM and non-volatile RAM to store and execute programs and data.

The peripherals of the 68000 are memory mapped in the usual way with the high bits of the address buss determining the active peripheral. Each peripheral capable of generating interrupts is assigned to a different interrupt level.

25.1.2 ROM's

(refer schematic MFX010-MEMORY (page 3 of 8))

Two 8 bit EPROM's are used in parallel to provide the 16-bit boot code required by the 68000. These EPROM's are 27256 varieties with access times of 170ns or better. When accessing these EPROM's, no wait states are required by the 68000 allowing full-speed operation.

On power-up or after a reset, the EPROM's are mapped at location 0, as this is where the 68000 loads its initial stack pointer and program counter. The EPROM's can also be accessed at location $100000H. By setting the signal OVLY low (U9 pin 17) the EPROM is mapped out of location 0 and replaced by static RAM. This allows the exception vector locations to be modified by software. The OVLY signal is set high by reset. Regardless of the state of OVLY, the EPROM's may be accessed starting at $100000H.

The first instruction of the EPROM is to set OVLY low. If this does not occur then the processor is probably not able to execute any instructions. If the processor does not even load the stack pointer and program counter then the problem is very fundamental, and is not simply problems with the address or data lines.

25.1.3 RAM

(refer schematic MFX010-MEMORY (page 3 of 8))

Four 8-bit static RAM's are used in parallel to provide the 16-bit wide memory space in which to execute code. Normally 256K-bit RAM's are installed giving 64K words of memory. The memory is mapped starting at location 0. This allows direct access to the 68000 exception vectors, which occupy the first $200H words.

On power-up or reset, the signal OVLY is high, mapping the EPROM's to location 0 and preventing access to the RAM's. Normally, the first instruction executed is sets OVLY low, mapping the RAM to location 0. OVLY should remain low until power is removed or the

processor is reset.

The MFX keyboard has been designed to allow downloading of software from the Series III CMI, eliminating the need for costly EPROM updates. The task of the boot code in the EPROM's is to move the application code from the non-volatile memory to the RAM for execution.

25.1.4 Non-volatile RAM

(refer schematic MFX010-MEMORY (page 3 of 8))

Three 8K by 8-bit static RAM with battery-backup is provided to store programs configuration setups and data. This RAM is protected by a DS1234 non-volatile controller (U38), which controls write-protection and battery usage. The memory may be configured to be read-only or read-write and volatile or non-volatile. Normally the memory is kept as ready-only non- volatile memory, and changed to- read-write memory only when the data is being changed.

As this memory space is only 8 bits wide, it is not possible to execute programs directly from this RAM. At a temperature of 25'C, the BR2325 battery should provide a life of 8 years. Care should be taken to avoid exposing the MFX to extremes of temperature for long periods of time, as elevated temperature decreases the battery life rapidly.

At the time of writing this document, 100% CMOS RAM's are only made by Toshiba and are proving difficult to obtain. However they offer such low stand-by currents that they would offer non-volatility for the shelf life of the battery (> 10 years).

There is a jumper block provided which allows selection of a variable number of wait states for the non-volatile RAM - either 0, 2, 4 or 6 wait states. This may be necessary as the DS1234 shortens the access times of- the RAM by around 30ns. The actual setting used depends on the speed of the installed static RAM.

25.1.5 Address Decoding

(refer schematic MFX010-CPU (page 2 of 8))

The address decoding is performed by two 74ACT138 demultiplexers (U21 and U26) and half of a 74HCT138 demultiplexer (U27). The 16 megabyte memory space of the 68000 is divided up into sixteen 1 megabyte areas by the two 74ACT138, with each register or peripheral given ifs own area. All the peripherals decoded by U26 are no wait-state devices, whilst those decoded by U21 must supply an open collector /DTACK signal.

The second last address space is supplied to the 74HCT138, which subdivides this space into four areas for use by peripherals which require synchronization to the 1MHz E clock of the 68000. The /CS6800 signal tells the 68000 to synchronise to the E clock by, asserting VPA low whenever this address range is selected. The highest 1 megabyte address space should be left vacant, as this space is selected whenever an interrupt acknowledge cycle is commenced.

/DTACK is generated by all four DUARTs (U7, U8, U9 and U10) and by the 74HC175 (U33). Whenever the demultiplexer U26 is selected, U33 is reset causing /DTACK to be asserted low. Whenever the non-volatile RAM is selected, the select signal is shifted through the flip-flops of U33 on the rising edge of PCLK (10MHz) until is appears at the link block (W4) causing /DTACK to be asserted low.

25.1.6 LED Circuitry

(refer schematic MFX010-DISPLAY (page 6 of 8))

The LED's controlled by the MFX are arranged into rows and columns, and lit using a multiplexed scheme. Under this scheme each LED is pulsed on for 1ms with a high current, and then turned off for 7ms. By pulsing the LED its efficiency is improved and the drive circuitry is simplified.

The 16 columns are controlled by two 74HC273 latches (U37and U38). If a bit is set to high, then the corresponding column is active. The columns are driven by two UDN2981A high-current source drivers (U29 and U30) and the current set by the 100R 1W resistors. The outputs of the source drivers are either VLED (+12V) if they are driven or floating if they are off.

The 8 rows are controlled by a 74HC164 shift-register (U19). This register is arranged as a circulating buffer with one bit high (the active row) and the other bits low. Every time an access is made to the column register, the active row is incremented. Two ULN2803A Darlington drivers (U15 and U12) drive the rows in parallel. The outputs of the drivers are either around 1 volt if driven or floating if they are off.

The circuitry has been designed to work optimally if the LED column register is accessed every 1ms. This speed ensures that the blinking of the LED's (125Hz) is faster than the human eye. If a Led were to be driven by this circuitry continuously then it would burnout because the driving currents are greater than the maximum allowable average current through the LED's. To prevent this undesirable event, protection circuitry has been installed to turn off the LED's if the column register is not accessed for 3ms. This protection circuitry consists of a 74HC123 dual monostables (U44 and U50) and a flip-flop (U31B). If a fault condition is detected then U37, U38 and U19 are reset, and the signal START goes high. When the LED register is next accessed, START supplies the initial conditions to drive output QH of U19 high. If the next row to become active will be ROWO then the signal CHECK will be high. This signal is available at ACIA2 (U10), input port signal IP4 (pin 43). The software should check this signal to determine if it agrees with what software expects. If a disagreement is detected, the software should immediately write a 0 to the LED column register and wait 10ms. If the signal CHECK is now high, the LED scanning may resume; otherwise the software should disable LED scanning and inform the user.

25.1.7 Clocks

(refer schematic MFX010-CPU (page 2 of 8))

A 10MHz oscillator (OSC1) supplies the main system clock, PCLK. The 68000 divides this signal by 10 to give the 1MHz E clock (6:4 duty cycle) used by slow synchronous peripherals (displays). The E clock is divided by a flip-flop (U31) to give a 1/2 MHz square wave. The 1/2 MHz clock is used by DUART U7 as the 16 x MIDI clock. A 3.6864MHz clock is generated by DUART U8 for use in generating RS232 baud rates. See the section on the DUARTS for more information.

25.1.8 Watchdog

(refer schematic *MFX010-CPU (page 2 of 8))*

A DS1232 watchdog (U45) is used to supervise the operation of the MFX keyboard. It drives the open collector /RESET and /HALT signals low whenever the +5V power supply is out of

range (4.76V to 5.25V), if the optional reset button has been pressed (connector J11), or if, the watchdog has not been accessed by the 68000 for 100ms. The 68000 requires both /RESET and /HALT to cause it to reset. If the 68000 does a double buss fault (e.g. loading an odd address pointer during an exception vector fetch) then it will drive /HALT low. If the 68000 executes a reset instruction, then it will drive /RESET only low. Both /RESET and /HALT also drive low-current red LED's (LD6 and LD8). If both LED's light simultaneously, then it is likely that the watchdog is driving these lines. However if the /HALT LED lights marginally before the /RESET LED then it is likely that the 68000 has had a double buss fault. This would occur if the ROM's were corrupt or if there was a serious problem with the address or data buss. If the green LED (LD7) remains lit, then the 68000 is executing code and keeping the watchdog at bay. If the green and red LED's light alternately, then the 68000 is not executing correct code.

25.1.9 Displays

(refer schematic MFX010-DISPLAY (page 6 of 8))

The MFX keyboard supports the attachment of two LM402B01 displays. These displays each offer 40 columns by 2 rows with up to 8 custom characters. The display is backlit by yellow LED's, which shine through the characters (clear characters on a black background). The data buss, address buss and R/W are buffered (74HCT245 at U36 and elsewhere) before driving the display signal cables (J8 and J9). The backlight is driven from 12V, as very little other use is made of the negative supply capacity of the MFX. A contrast adjustment pot is accessible from the top right hand corner of the MFX keyboard. Before concluding that a display is faulty because nothing is visible, you should check the contrast adjustment.

25.1.10 DUARTs

(refer schematic MFX010-DUARTS & DRIVERS (page 4&5 of 8))

The MFX supports serial communications with the following devices:

1. MIDI to MIDI D on the MFX
2. MIDI from MIDI D on the MFX
3. Midi from the Fairlight music keyboard
4. RS422 to and from a LYNX synchroniser or other synchroniser supporting the ES Bus
5. RS232 to and from an MFX expansion device
6. RS232 to the MFX keyboard input
7. RS232 from printer port 2 on the MFX (this port is no longer an external connector)
8. RS232 from the music keyboard
9. RS232 to and from a mouse

Four 68C681 DUARTs (U7, U8, U9 and U10) support these communication channels.

U8 drives a 3.6864Mhz crystal, which when buffered by a 74HC240 (U6H) is supplied to the other DUARTs. This clock is divided by the 68C681s to give the RS232 baud rates. A 1/2MHz

clock is used as the MIDI 16 times clocks.

The 68C681 DUART has two transmit channels, and two receive channels. All channels have independent baud rates. An internal, 16-bit counter can be programmed in a variety of ways to act as a timer, counter or frequency generator. An 8-bit output port is provided, with some of the bits being able to provide status information. A 6 bit input port can be read directly, or programmed to generate interrupts on either or both edges of a signal.

The 68C681 implements the full 68000 interrupt vectoring scheme, by providing the contents of an interrupt vector register to the 68OOO during the interrupt acknowledge cycle.

25.1.11 AC1A1

(refer schematic MFX010-DUARTS (page 4 of 8))

AClA1 (U7) handles MIDI communications. MIDI to and from the MFX (port D) is handled by the “A” side, whilst MIDI from the music keyboard is received by side “B”. The 1/2MHz clock is supplied to input pins IP2 to IP5, and the software configures these inputs to be the 16 times clock inputs. This DUART can generate level 5 interrupts, enabling quick response to MIDI data.

25.1.12 ACIA2

(refer schematic MFX010-DRIVERS (page 5 of 8))

AClA2 (U10) handles RS422 communications at 38k4 baud to Lynx synchronisers, or other synchronisers supporting the ES-buss. The Lynx Synchroniser generates a square Wave synchronised to the field edges of a video signal (SYSC on pin3 of U10), which can be programmed to cause an interrupt in the MFX. It also handles the RS232 bi-directional channel available on the MFX expansion port. This DUART can generate level 4 interrupts.

25.1.13 ACIA3

(refer schematic MFX010-DUARTS (page 4 of 8))

ACIA3 (U8) handles RS232 communication to and from the MFX. Side “A” transmit drives the alphanumeric keyboard input signal on the MFX. The RS232 keyboard output from the MFX appears at the receive input, side “B”. This DUART can generate level 2 interrupts.

25.1.14 ACIA4

(refer schematic MFX010-DUARTS (page 4 of 8))

ACIA4 (U9) handles RS232 communications to and from a mouse using side “A”. This mouse should be a serial mouse with a DB9 connector for attachment to the serial port of an IBM PC-AT. There are numerous software protocols possible. Side “B” is unused, This DUART can generate level 2 interrupts.

Interface drivers

(refer schematic MFX010-DRIVERS (page 5 of 8))

MIDI is received using PC900 opto-couplers (U1, U2). This circuit is the circuit

recommended by the MIDI specifications. The MlDI transmitter is a BC549 transistor (Q7), which makes this circuit more rugged than the usual 7407 open-collector transmitter circuit. The tape synchroniser is interfaced using a DS8921 RS422 transmit receiver pair (U3), The driver has a source impedance of 110ohm and a low-pass filter. The receiver has termination impedance of 110ohm at high frequency, increasing to high impedance at DC. Pull-up resistors cause the +ve input to see a higher voltage than the -ve input if the inputs are not being driven. RS232 is driven by a 14C88-driver (U4), with all outputs filtered and output impedance's of 110 ohm. The voltage swing is +11V to -11V typically. A 14C89-receiver (U5) has termination impedances of 120 ohm at high frequency, increasing to high-impedance at DC.

25.1.15 Speaker

(refer schematic MFX010-DRIVERS (page 5 of 8))

Five of the output pins of AClA2 (U10) are used to produce tones through the speaker of the MFX. Each output is connected to a different resistor and summed at a common node. The signal is then AC-coupled and low-pass filtered before reaching the non-inverting input of a power op-amp (U14). By turning a pot accessible from the top right hand corner of the MFX, the gain of the op-amp may be varied. The op-amp directly drives an 8ohm speaker. Each output can produce an independent tone, with a volume level that depends upon the Output Used. The Signal SL1 produced by OP3 (pin 15 of ACIA2 (U10)) can be programmed to be a free running square-wave derived from the internal counter. The other four outputs require that the processor toggle each bit directly.

25.1.16 Key scanning

(refer schematic MFX010.004 and 009)

The switches are arranged into banks, with each bank containing 8 switches. The bank address is written to the output register of ACIA1 (U7), and the state of the 8 switches can then be read from the 74HC244 buffer (U11). A 1 in a switches bit position indicates that the switch is open (up), whilst a 0 indicates that the switch is closed (depressed). The bank address consists of a 4-bit diode network number, and a 4-bit circuit board selection number.

7		unused (future expansion)
6		unused (future expansion)
5	ENPANEL	0 panel key (MFK panel keys) enabled 1 panel key disabled
4	ENQWERTY	0- qwerty key (MFK qwerty keys) enabled 1= qwerty key disabled
3	SWI3	number of the active
2	SWI2	diode-network on
1	SWI1	each circuit board
0	SWI0	(MFX030 and MFX040)

Fig 1. Switch bank address register (output port of U7)

25.1.17 Jogger wheel

(refer schematic MFX010-DRIVERS (page 5 of 8))

The MFX supports the decoding of an optical shaft encoder. The quadrature output of the encoder is pulled up and low-pass filtered before being buffered by a 74HC132-schmitt-trigger (U18). The outputs of the Schmidt trigger are fed to ACIA2 (U10), input port bits IPO and lP1. The DUART can be configured to cause an interrupt on the edge of the quadrature signal.

25.1.18 MFK Qwerty board.

(Refer schematic MFK)

The MFK board supports and decodes the QWERTY keyboard, the function keys and the panel trigger keys. It receives power from MFX010 through a 10-way Molex connector, and communicates with, MFX010 through a 50-way lDC connector. The panel trigger keys and all other switches are scanned by the 68000 processor.

25.1.19 Qwerty, Panel trigger switches and function keys.

(refer schematic MFK-MFX console key panel)

The QWERTY, function and panel keys are decoded using a diode matrix, with an active row/column scheme. This allows infinite key roll-over to be implemented. The diodes are contained in 25 common cathode diode networks (DN1 through DN25).

25.1.20 Qwerty

(refer schematic MFK-qwerty keys 1 to 4)

The QWERTY keys are arranged into 4 banks (qwerty1, qwerty2, qwerty3, and qwerty4). The address of the active QWERTY key is set up by the 12-bit code SWQ0 through SWQ12. SWQ0-3 selects qwerty1, SWQ4-7 selects qwerty2, SWQ8-11 selects qwerty3, and SWQ12 selects qwerty4.

The anodes of the QWERTY diode networks are connected to the outputs of two 74HC138 8-channel multiplexors (U3 and U4). If the signal ENQWERTY is low, then the signals SWI0 through SWI3 set which of the 12 (plus 4 unused) outputs SWQ0 through SWQ15 will be low.

25.1.21Panel

(refer schematic MFK-panel keys 1 to 4)

The PANEL keys are arranged into 4 banks (panel1, panel2, panel3, and panel4). The address of the active PANEL key is set up by the 14-bit code SWP0 through SWP13. SWP0-3 selects panel1, SWP4-7 selects panel2, SWP8-11 selects panel3, and SWP12-13 selects panel4.

The anodes of the PANEL diode networks are connected to the outputs of two 74HC138 8-channel multiplexors (U2 and U1). If the signal ENPANEL is low, then the signals SWI0 through SWI3 set which of the 14 (plus 2 unused) outputs SWP0 through SWP15 will be low.

The signals SWOO0 through SWO7 are pulled up to +5V by resistors on MFX010. Thus only

one diode network will have its cathode near GND, allowing its diodes to conduct if the attached switches are closed.

25.2 MFX CONSOLE DIAGNOSTICS

1. To reset the non-volatile RAM in the MFX console switch OFF power and hold down numeric keypad keys 1:2:3. Switch on power while keys are depressed. Go to the shell from MFX project screen by typing “SHIFT” $ <ret>. At the # type “mfxload” ret>. The system will load the non-volatile RAM. When operation is complete depress “ESC” key.

2. To enter diagnostics on the MFX console hold down numeric keypad keys 4:5:6. Switch on power while keys are depressed. Release keys when you are ready to enter diagnostics. Depress Fl:F3:F5:F7 to exit test.

TEST NUMBER	TEST DESCRIPTION
0	LCD, 68000 RAM, LED circuits
1	Raw Keyboard Test
2	ASCII keyboard Test, depress ‘keys and Check LCD display
3	Jogger and mouse X axis / Y axis
4	N/A
5	N/A
6	NIA
7	Speaker level test. Adjustment on top right corner of console
8	RS422 / N/A
9	Return MFX console to MFX operation

To set LCD contrast, adjust preset on top right corner of console.

3. Depressing keys -:+:BLUE will set console for software up load. This does not reset the non-volatile RAM as in point 1.

CABG8529 - MFX Plus Cable Assembly

REV.	DATE	DESIGNED BY	DESCRIPTION	PCO	ZONE
1.0	5/8/96	L.Stewart	RELEASE		
1.1	16/1/97	L.Stewart	Cable spec and connections		
1.2	7/12/98	N.Plummer	Rotated drawing to match connection drawing. Corrected title name.		

NOTE :

1. Cable to be to the following specification;
   12 Pair + Drain Twisted Pair
   7/0.02mm Stranded Cores
   RS422 Hi Speed Data (50pF/m)
   Low Impedance & Braided Screen
   e.g. MCP-12S/BS (supplier A.G.Garland)
2. Refer to Dwg # CABC8529.DW2 for connections
3. Refer to supplied documentation for additional information regarding termination of cable screens
4. Ferrites to be FairRite P/N 2643626402 Fairlight P/N FERB0110)
5. Cover ferrites with heatshrink

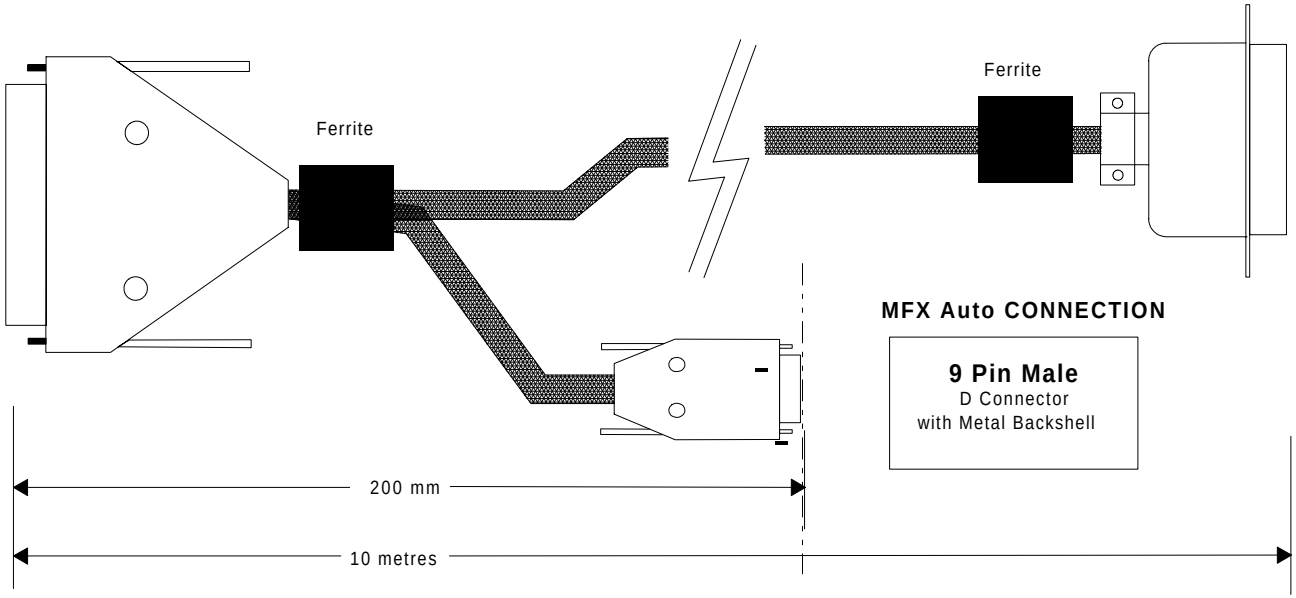
See also related connection drawing
Cabg8529 MFXP 1 of 2 Connect rev 1-3.dc

MAINFRAME CONNECTION

24 Pin Male
Centronics Connector
with Metal Backshell

CONSOLE CONNECTION

37 Pin Male
D Connector
with Metal Backshell



MFX Auto CONNECTION

9 Pin Male
D Connector
with Metal Backshell

DIMENSION UNITS: mm	DESIGNED BY ENGINEERING: L.Stewart	TITLE: CABG8529 - MFX Plus Cable Assembly	REV. 1.2
TOLERENCE: ± 3%	APPROVED BY ENGINEERING		
FILE NAME: CABG8529.DW2	APPROVED BY PRODUCTION	FILE NAME: Cabg8529 MFXP 1 of 2 Assy rev 1-2.dc	
	APPROVED BY QUALITY CONTROL	SCALE N.T.S. / SHEET 1 OF 1 / COMPANY CONFIDENTIAL	

CABG8529 - MFX Plus Cable Connection Diagram

REV.	DATE	DESIGNED BY	DESCRIPTION	PCO	ZONE
1.0	16/12/96	L.Stewart	RELEASE		
1.1	16/1/96	L.Stewart	Cable Spec & Connections		
1.2	27/8/98	M.Paolino	Signal names corrected (Midin / out)		
1.3	7/12/98	N.Plummer	Previous change reversed. Signal names changed to PCB name at each end. Corrected part number in title.		

NOTES :

** Assumes this signal when appropriate jumper is in place

1. Cable is to be to the following specification;
   14 Pair + Drain Twisted Pair
   7/0.02 Stranded cores
   RS422 HI SPEED Data (50pF/m)
   LOW IMPEDANCE
   Braided screen
   e.g. MCP-12S/BS (Supplier: A.G. Garland)

See also related assembly drawing
Cabg8529 MFXP 2 of 2 Assy rev 1-2.dc

Console Connection

37 Pin Male
D Connector
with Metal Backshell
UL Recognised
(Connects to J2 on MFX010)

Signal Name (MFX010 PCB)	Connector Pin No.	Colour	Mandatory	Connector Pin No.	Signal Name (ESP-MIDI PCB)	
FS+	13	Brown	Yes	5	X422+	Pair
FS-	31	Brown/White	Yes	17	X422-	
TS+	12	Grey	Yes	6	R422+	Pair
TS-	30	Grey/White	Yes	18	R422-	
MO1+	8	Green		10	Mid+	Pair
MO1-	26	Green/White		22	Mid-	
MI1+	9	Blue		9	MOut+	Pair
MI1-	27	Blue/White		21	MOut-	
MI2+	11	Orange		7	n/c	Pair
MI2-	29	Orange/White		19	n/c	
RSI1	6	Brown	Yes	12	Data2	Pair
Gnd	21	Brown/Black	Yes	14	Gnd **	
RSI2	7	Grey		11	Data1 **	Pair
Gnd	20	Grey/Black	Yes	13	Gnd **	
RSO2 **	25	Green		23	KEYBDOUT**	Pair
n/c	16	Green/Black		15	n/c	
Gnd	10	Green	Yes	8	*MFXPresent	Pair
SYSC	28	Green/Yellow		20	n/c	
RSO1	24	Orange	Yes	24	Datain	Pair
Gnd	23	Orange/Black	Yes	16	Gnd **	
n/c	2	Grey		2	n/c	Pair
n/c	4	Grey/Red		3	n/c	
Gnd	1	Green	Yes	1	Gnd **	Pair
n/c	14	Green/Red		4	n/c	
MRXD	36	(any)	Yes	2	(MRXD)	
MTXD	37	(any)	Yes	3	(MTXD)	
Gnd	33	(any)	Yes	5	Gnd	

Mainframe Connection

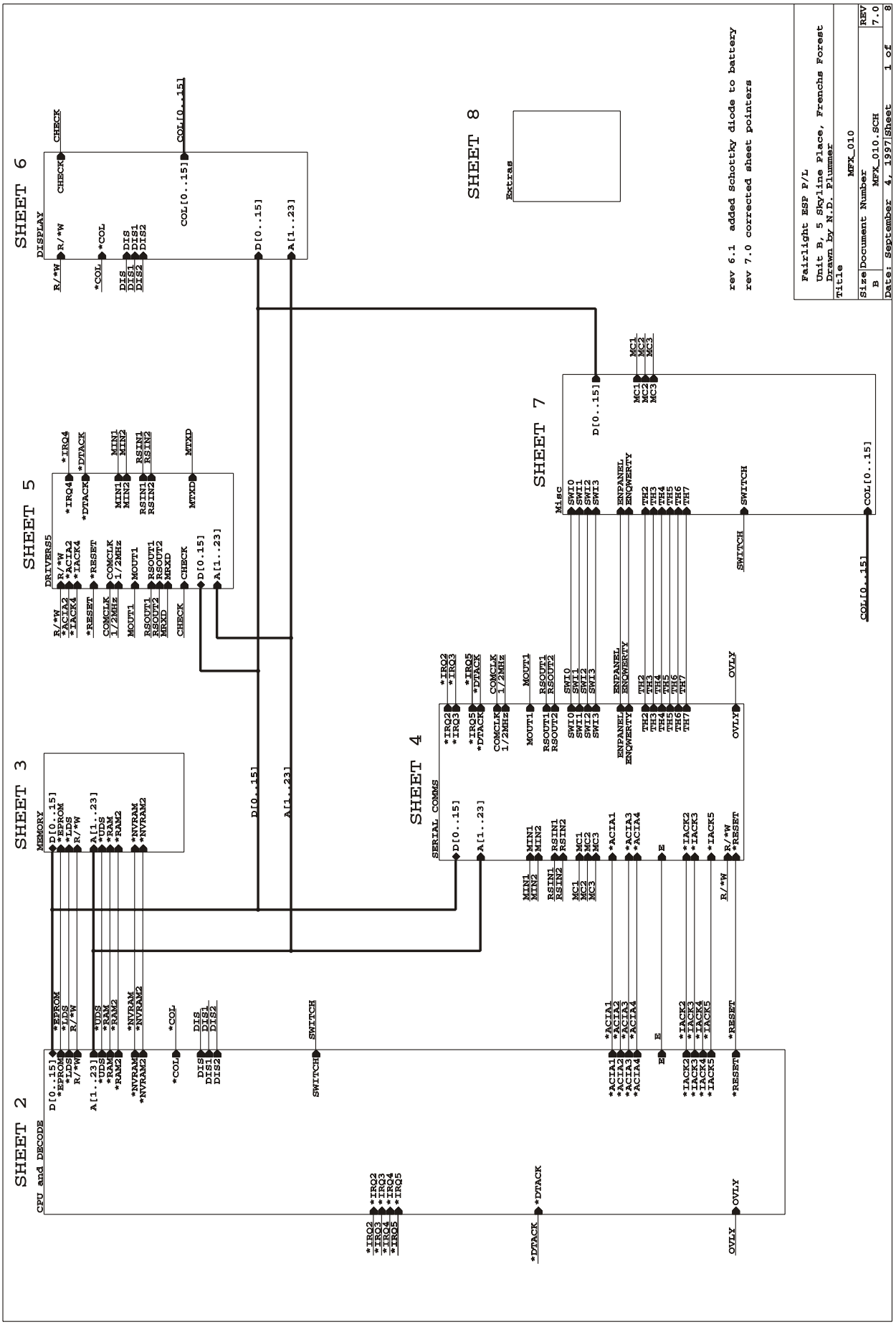
24 Pin Male
Centronics Connector
with Metal Backshell
UL Recognised
(Connects to P5 on ESP-MIDI)

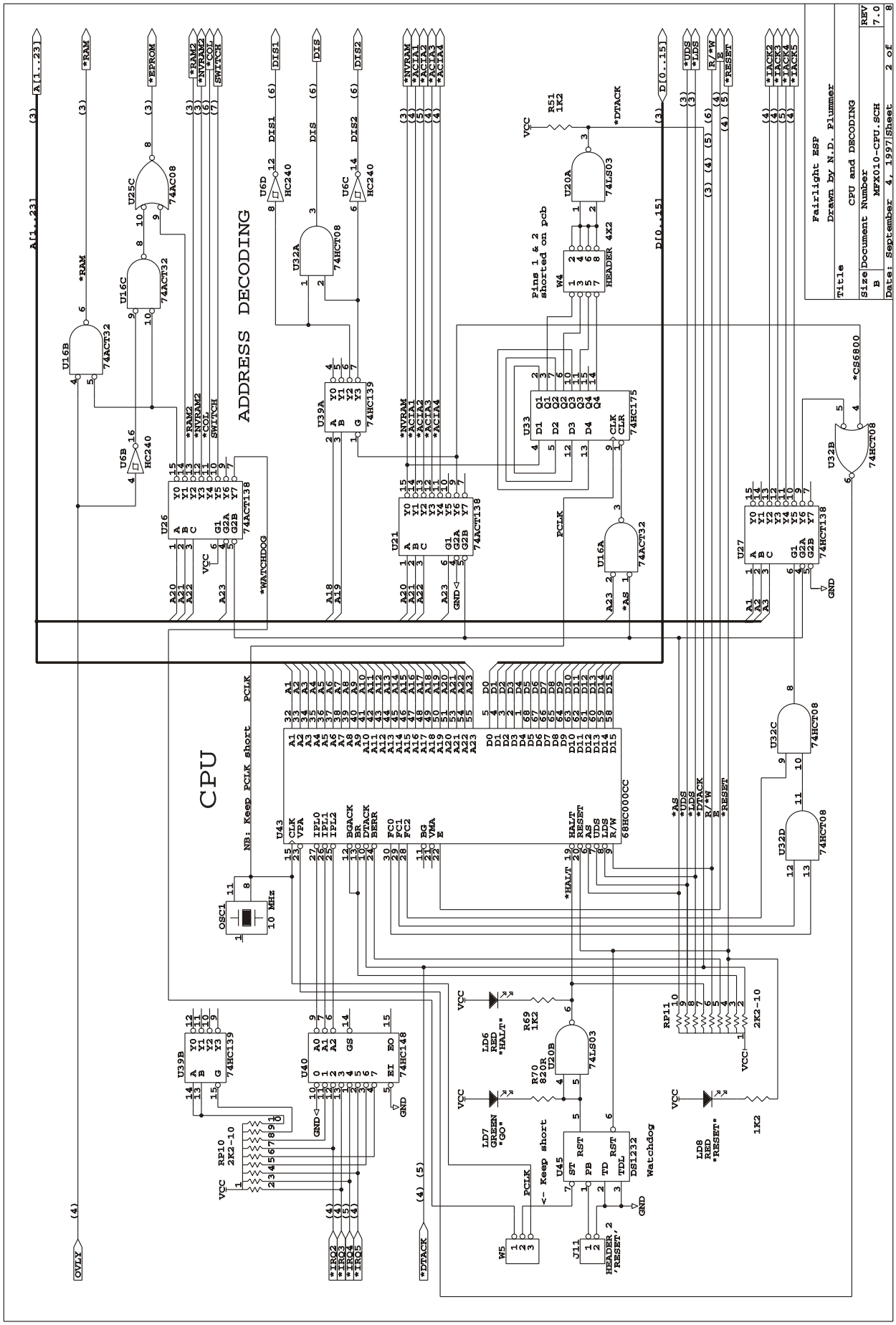
MFX Auto Connection

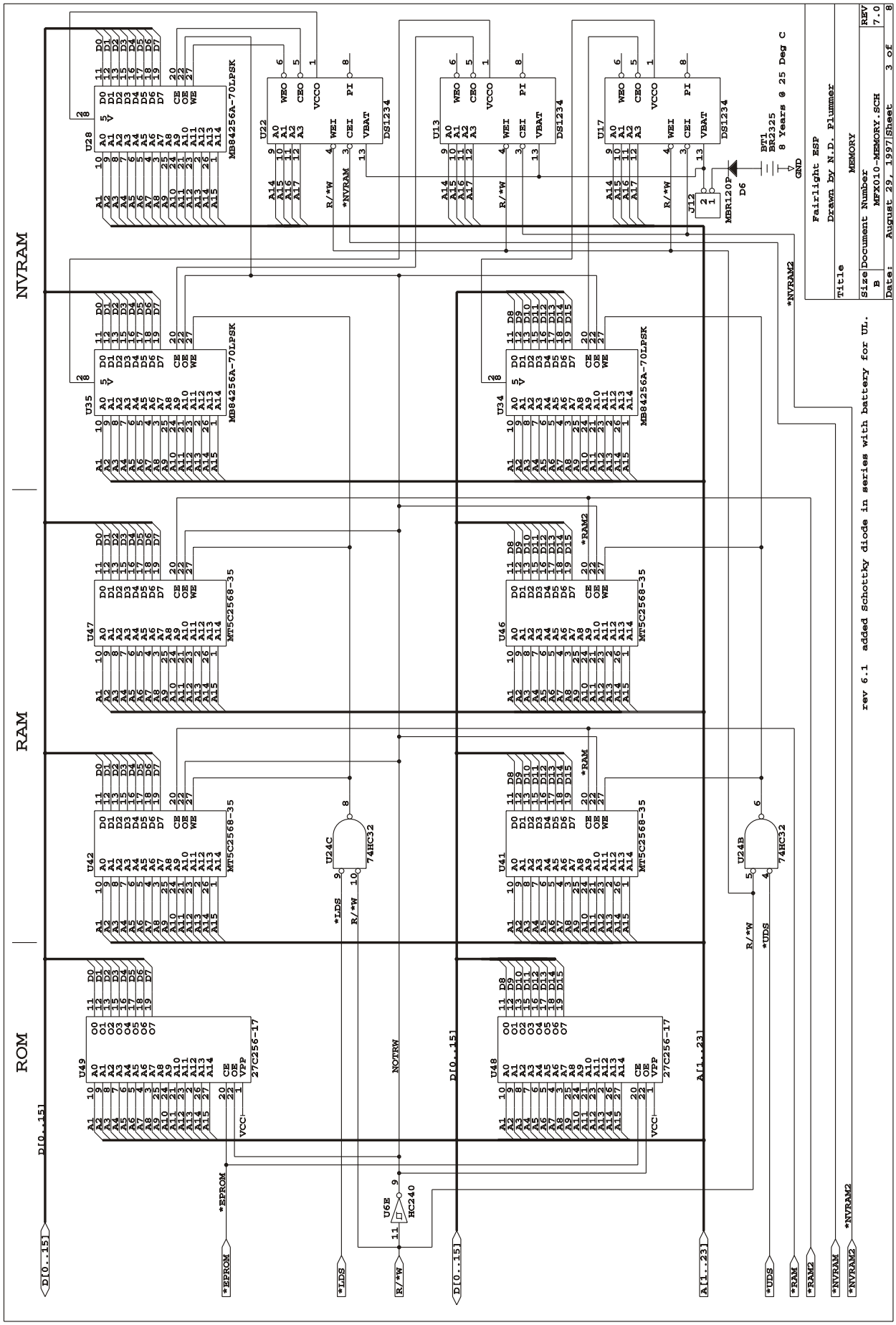
9 Pin Male
D Connector
with Metal Backshell
UL Recognised
(Connects to Serial Port on PC)

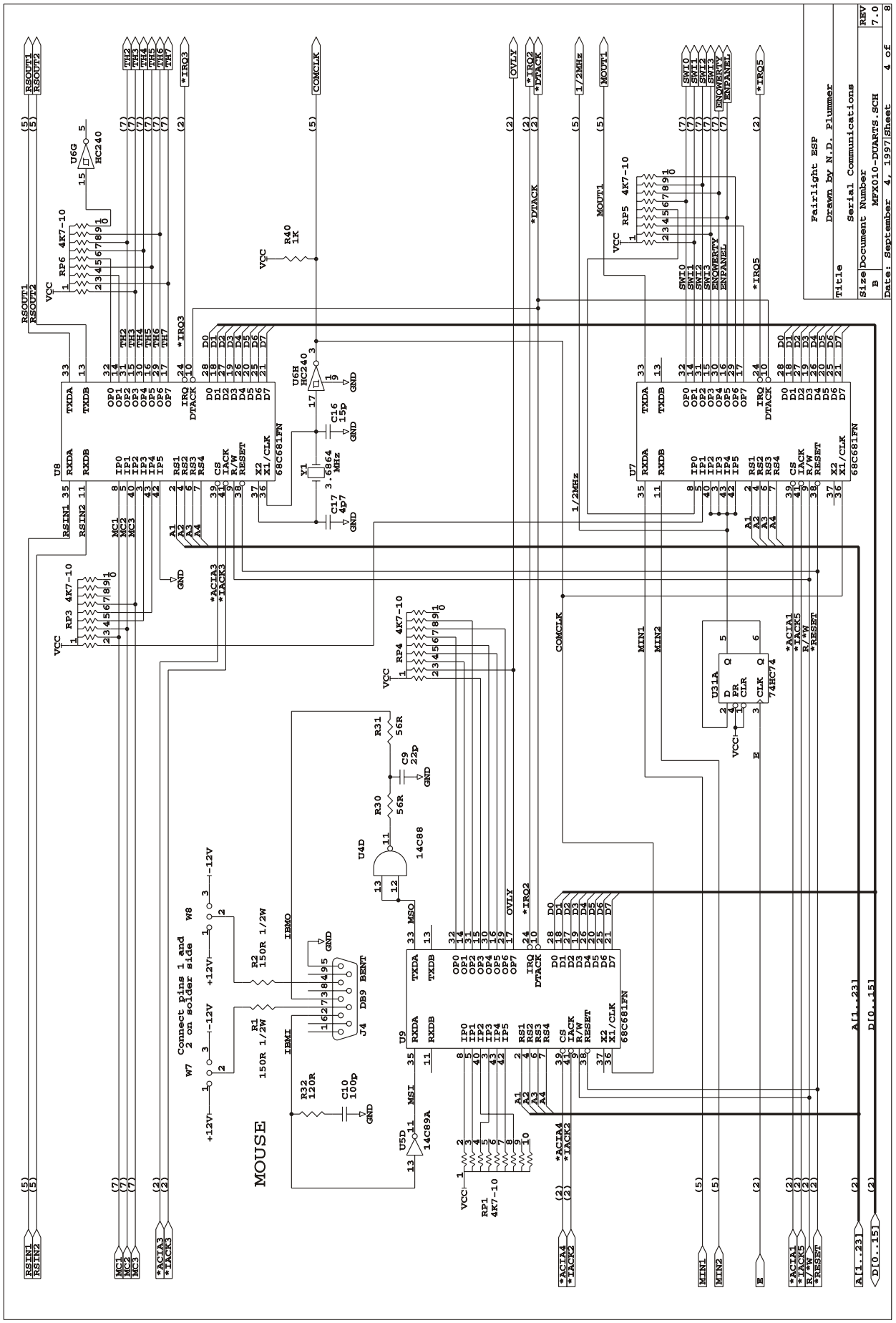
DIMENSION UNITS: mm	DESIGNED BY ENGINEERING: L.Stewart	TITLE: CABG8529 - MFXP Cable Connection Diagram	REV. 1.3
TOLERENCE: ± 3%	APPROVED BY ENGINEERING	FILE NAME: Cabg8529 MFXP 2 of 2 Connect rev 1-3.dc	
FILE NAME: CABC8529.DW2	APPROVED BY PRODUCTION	SCALE N.T.S. / SHEET 1 OF 1	COMPANY CONFIDENTIAL
	APPROVED BY QUALITY CONTROL		

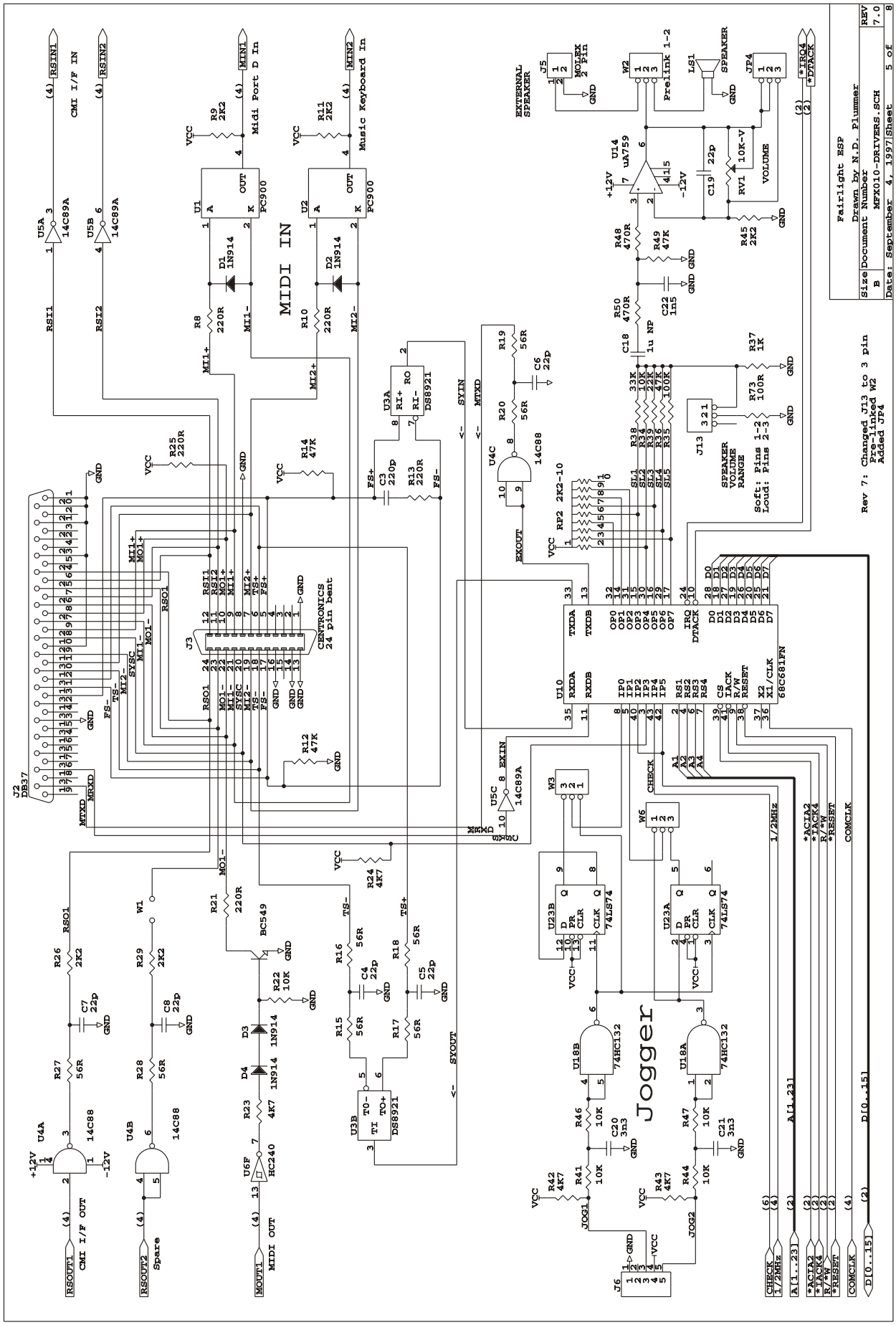
25.4 MFX010 Controller Card Schematics

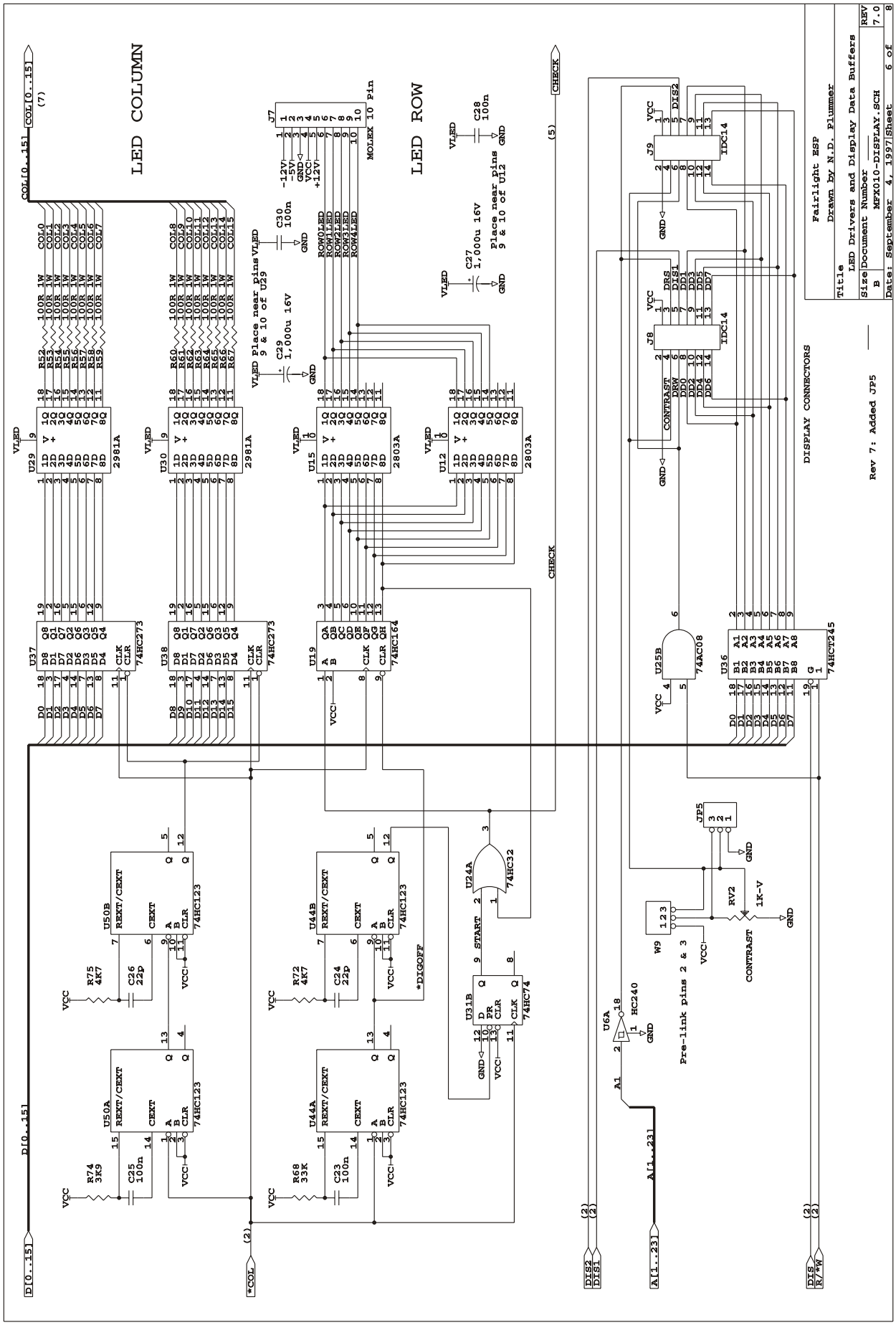


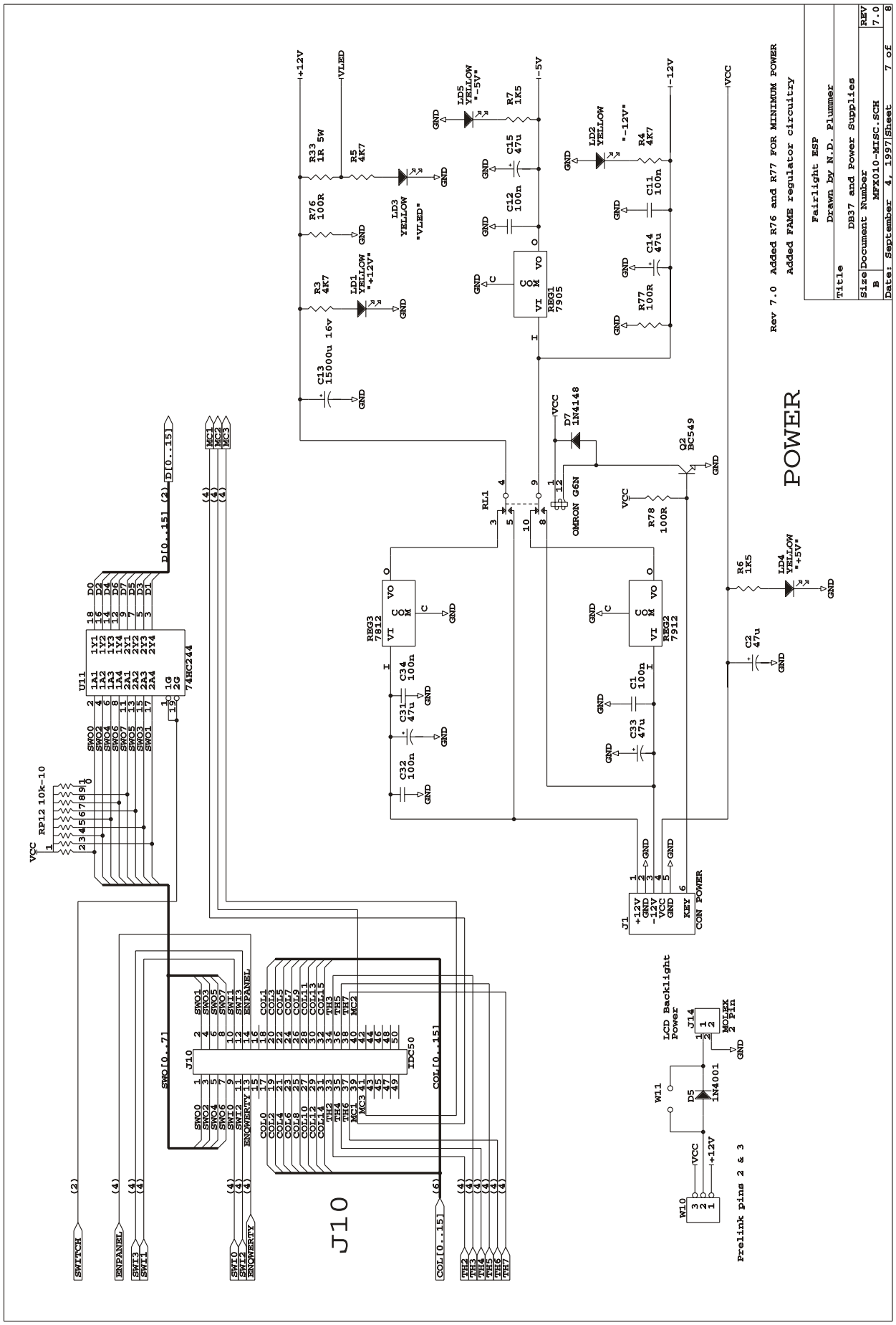

ADDRESS DECODING
CPU
Fairlight ESP
Drawn by N.D. Plummer
Title CPU and DECODING
Size B Document Number MFX010-CPU.SCH REV 7.0
Date: September 4, 1997 Sheet 2 of 8
NB: Keep PCLK short
<- Keep short
Watchdog
Pins 1 & 2 shorted on pcb
*WATCHDOG
*DTACK
*CS6800
*RESET
*HALT
*AS
*UDS
*LDS
R/*W
*IRQ2
*IRQ3
*IRQ4
*IRQ5
*TACK2
*TACK3
*TACK4
*TACK5
LD6 RED "HALT"
LD7 GREEN "GO"
LD8 RED "RESET"
HEADER 'RESET'
HEADER 4X2
10 MHz
1K2
2K2-10
820R

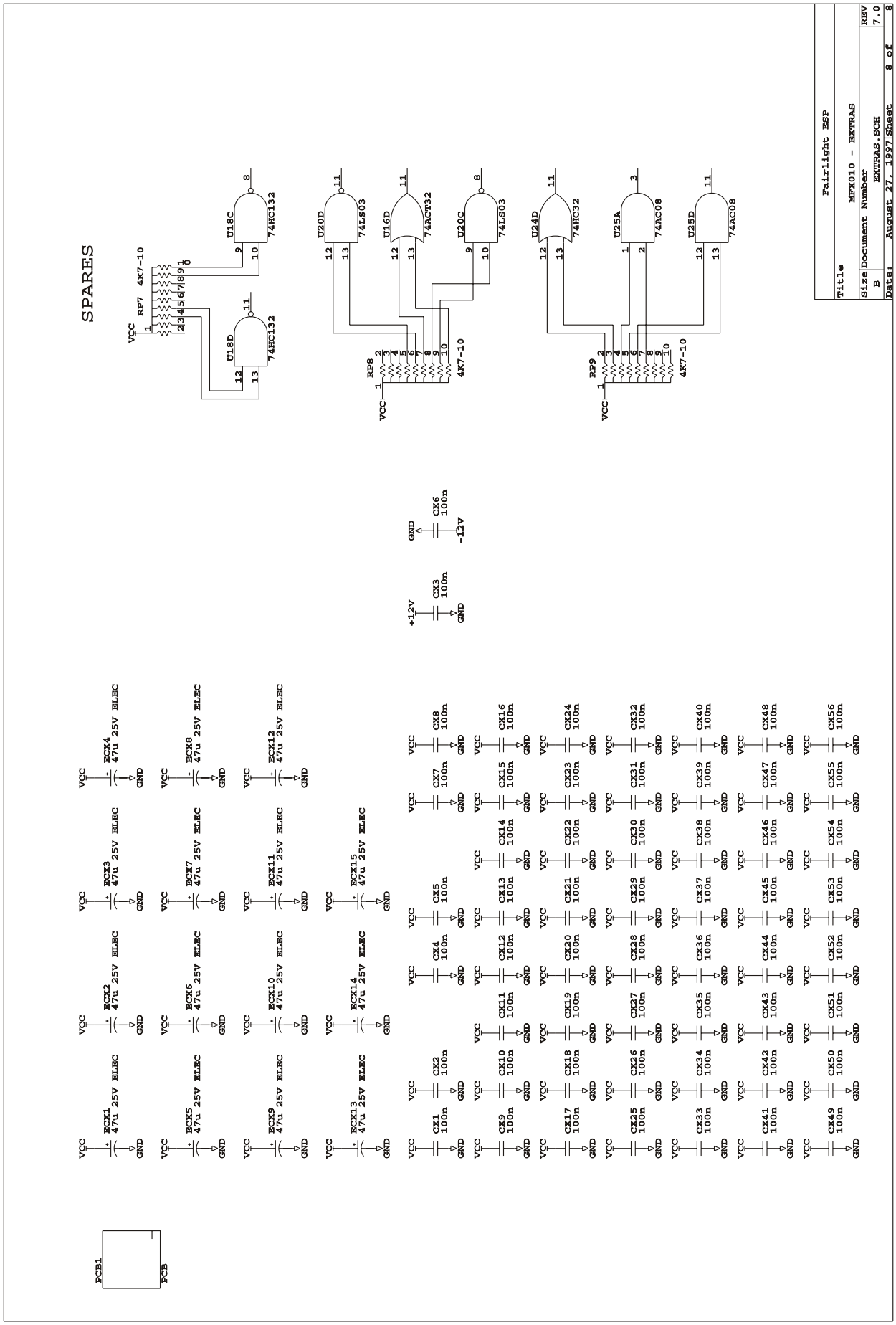

NVRAM
RAM
ROM
Fairlight ESP
Drawn by N.D. Plummer
Title
MEMORY
Size
Document Number
MFX010-MEMORY.SCH
REV
7.0
Date: August 29, 1997
Sheet 3 of 8
rev 6.1 added Schottky diode in series with battery for U1.
MB84256A-70LPSK
MT5C2568-35
27C256-17
74HC32
HC240
DS1234
MBR120P
BR2325
8 Years @ 25 Deg C
D[0..15]
A[1..23]
*EPROM
*LDS
*UDS
*RAM
*RAM2
*NVRAM
*NVRAM2
R/*W
NOTRW
*NVRAM
*RAM
*RAM2


Fairlight ESP
Drawn by N.D. Plummer
Title Serial Communications
Size B Document Number MFX010-DUARTS.SCH REV 7.0
Date: September 4, 1997 Sheet 4 of 8
MOUSE
Connect pins 1 and 2 on solder side
U8
U9
U7
U6H HC240
U6G HC240
U31A 74HC74
U4D 14C88
U5D 14C89A
RP3 4K7-10
RP4 4K7-10
RP5 4K7-10
RP6 4K7-10
RP1 4K7-10
R40 1K
R1 150R 1/2W
R2 150R 1/2W
R30 56R
R31 56R
R32 120R
C10 100p
C9 22p
C16 15p
C17 4p7
Y1 3.6864 MHz
J4 DB9 BENT
68C681FN
RSOUT1
RSOUT2
RSIN1
RSIN2
MC1
MC2
MC3
*ACIA3
*TACK3
*IRQ3
COMCLK
OVLY
*IRQ2
*DTACK
1/2MHz
MOUT1
SWI0
SWI1
SWI2
SWI3
ENOWERTY
ENPANEL
*IRQ5
*ACIA4
*TACK4
*ACIA1
*TACK5
R/*W
*RESET
MIN1
MIN2
E
A[1..23]
D[0..15]

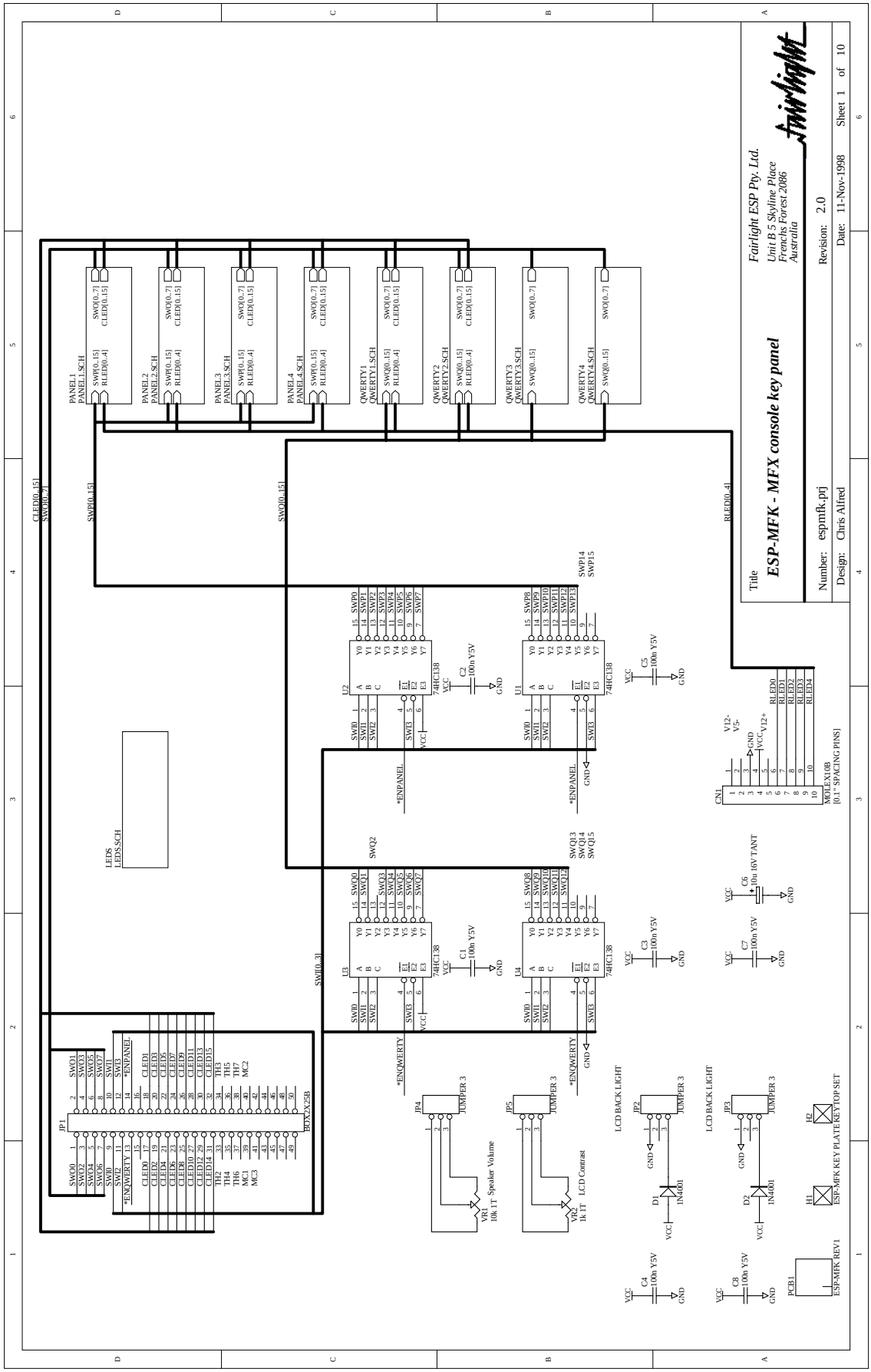

MIDI IN
Joggger
CMI I/F IN
Midi Port D In
Music Keyboard In
CMI I/F OUT
Spare
MIDI OUT
CENTRONICS
24 pin Dent
SPEAKER
VOLUME
RANGE
Soft: Pins 1-2
Loud: Pins 2-3
Prelink 1-2
SPEAKER
VOLUME
EXTERNAL
SPEAKER
Rev 7: Changed J13 to 3 pin
Pre-linked W2
Added JP4
Fairlight BSP
Drawn by N.D. Plummer
Size Document Number REV
B MFX010-DRIVERS.SCH 7.0
Date: September 4, 1997 Sheet 5 of 8

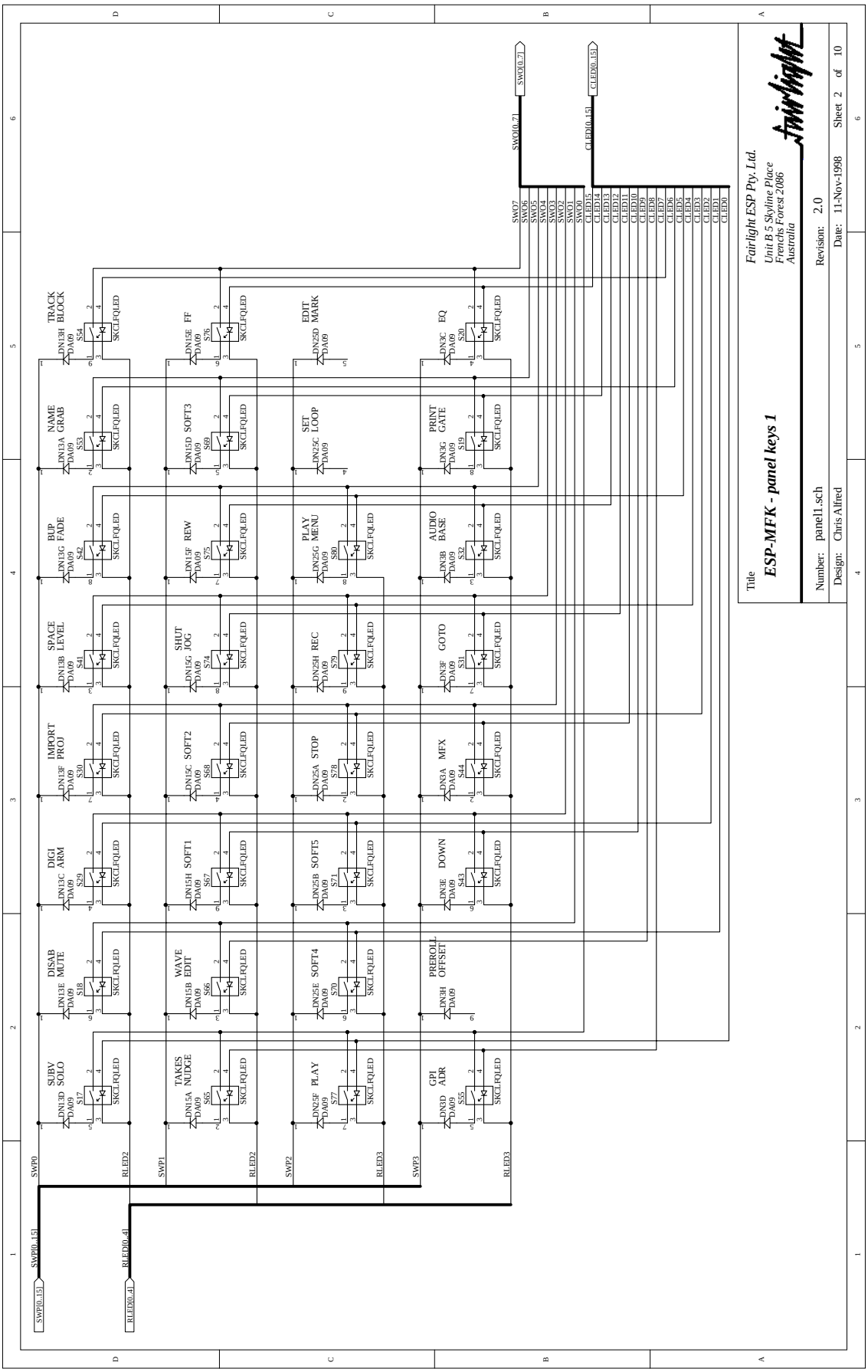

LED COLUMN
LED ROW
DISPLAY CONNECTORS
Fairlight ESP
Drawn by N.D. Plummer
Title
LED Drivers and Display Data Buffers
Size|Document Number
B
MFX010-DISPLAY.SCH
REV
7.0
Date: September 4, 1997|Sheet 6 of 8
Rev 7: Added JP5
Pre-link pins 2 & 3
CONTRAST
*DIGOFF
*COL
CHECK
D[0..15]
A[1..23]
COL[0..15]
MOLEX 10 Pin
IDC14
74HC273
74HC164
74HC123
74HC32
74HC74
74HC240
74HCT245
74AC08
2981A
2803A

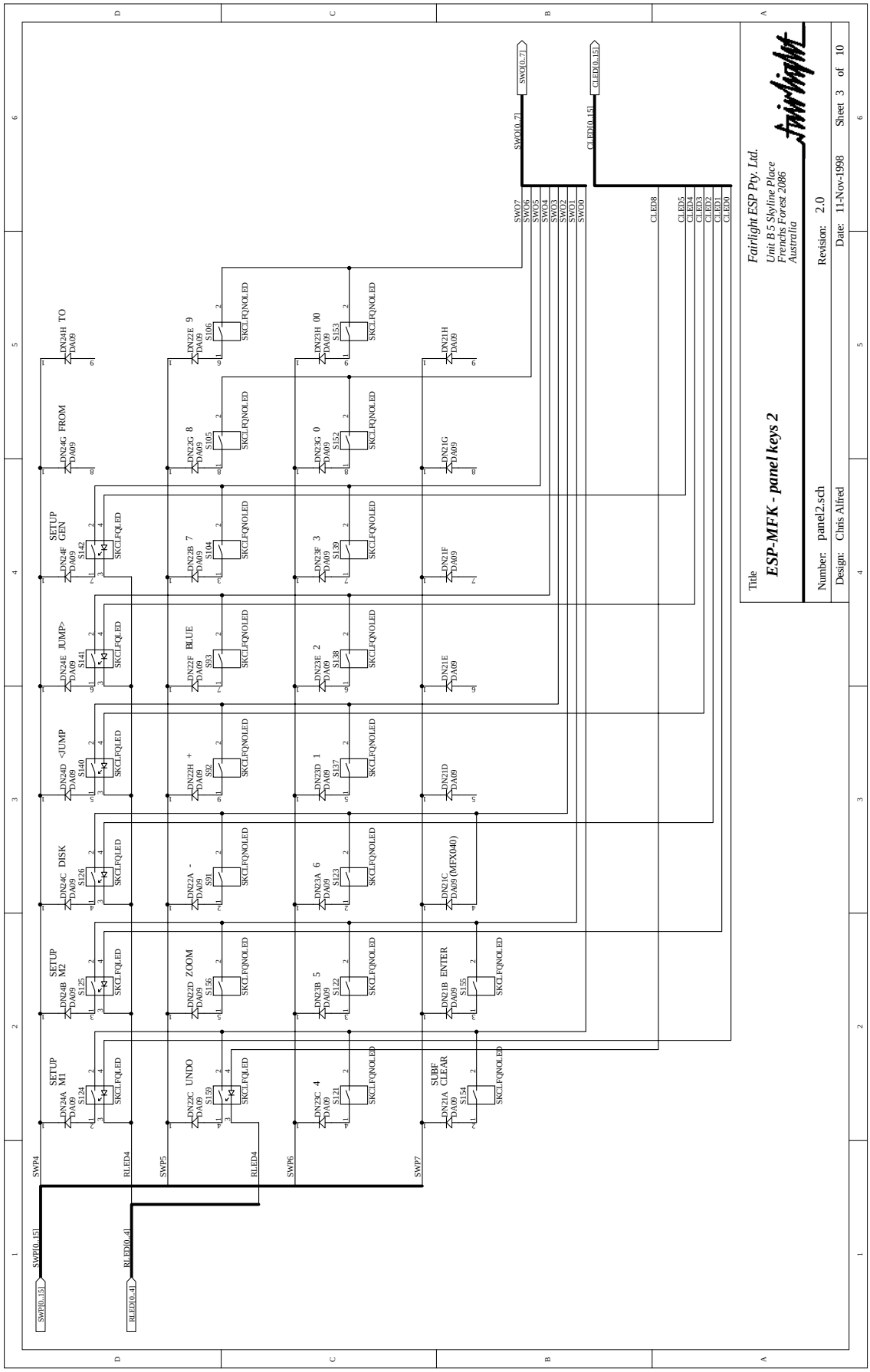

POWER
J10
Rev 7.0 Added R76 and R77 FOR MINIMUM POWER
Added FAME regulator circuitry
Fairlight ESP
Drawn by N.D. Plummer
DB37 and Power Supplies
MFX010-MISC.SCH
Date: September 4, 1997 Sheet 7 of 8
Prelink pins 2 & 3
LCD Backlight Power
CON POWER
OMRON G6N
74HC244
IDC50
MOLEX 2 Pin

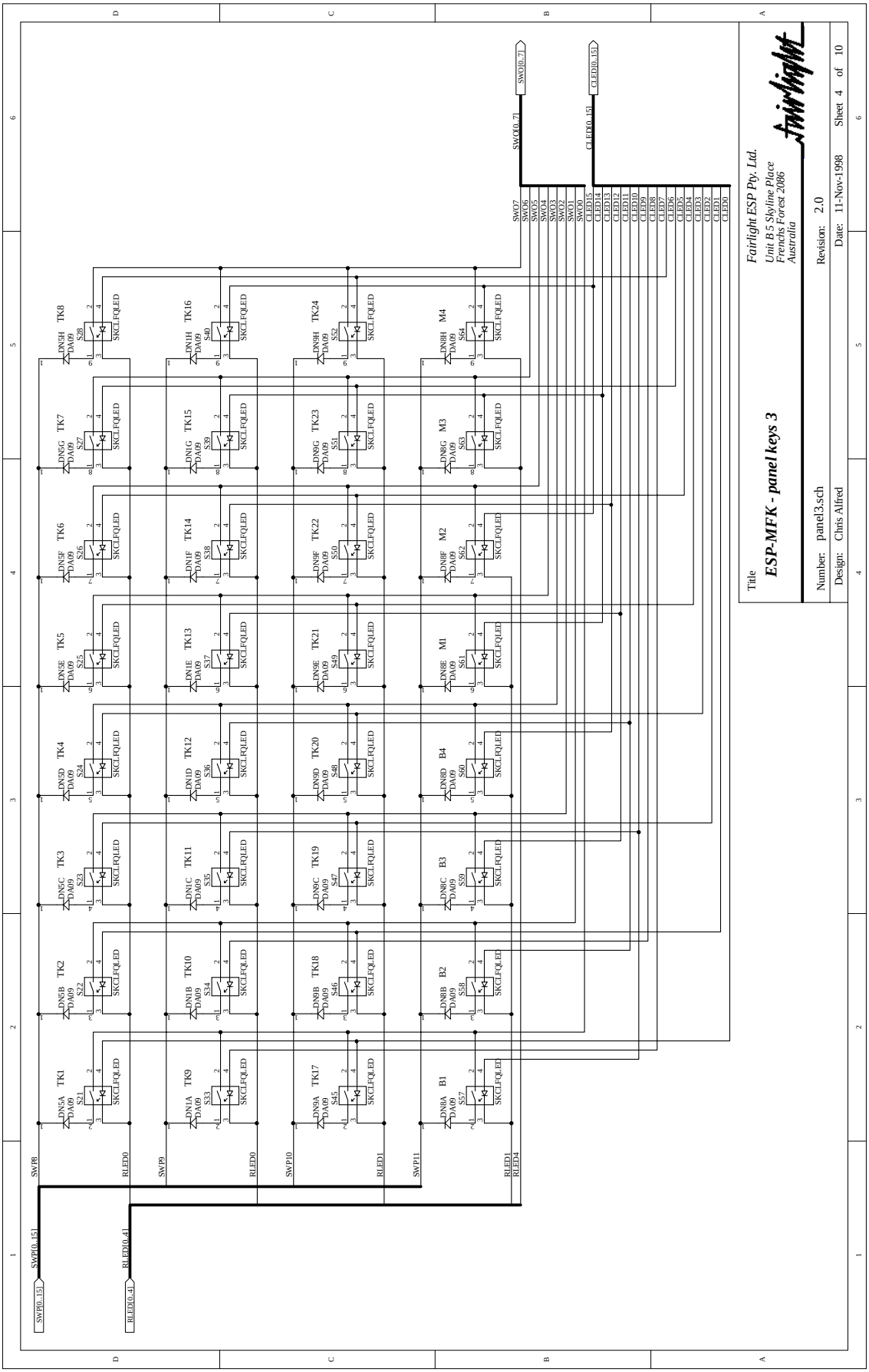

SPARES
Fairlight ESP
Title
MFX010 - EXTRAS
Size
B
Document Number
EXTRAS.SCH
REV
7.0
Date: August 27, 1997
Sheet 8 of 8

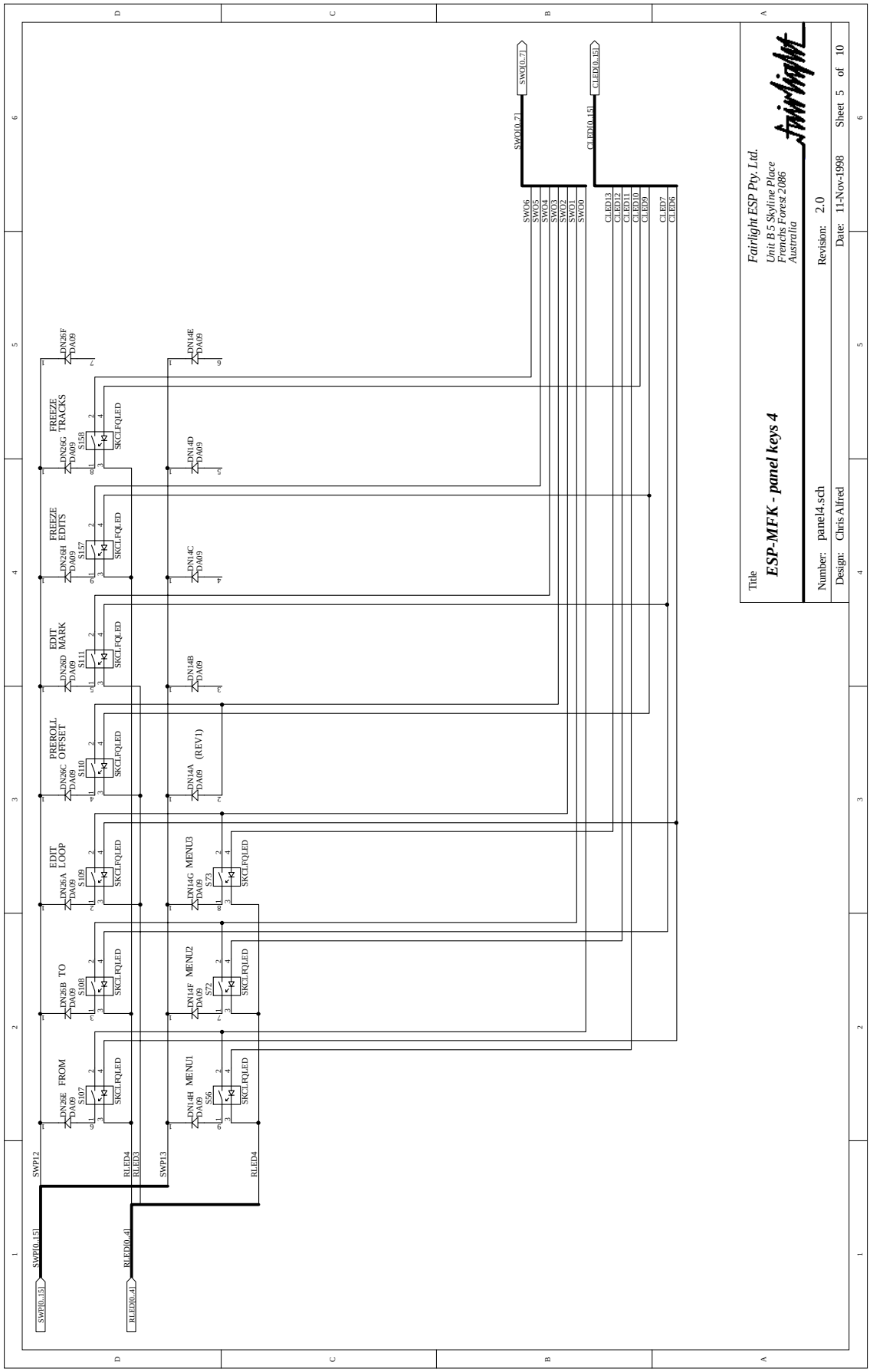
25.5 MFK Schematics

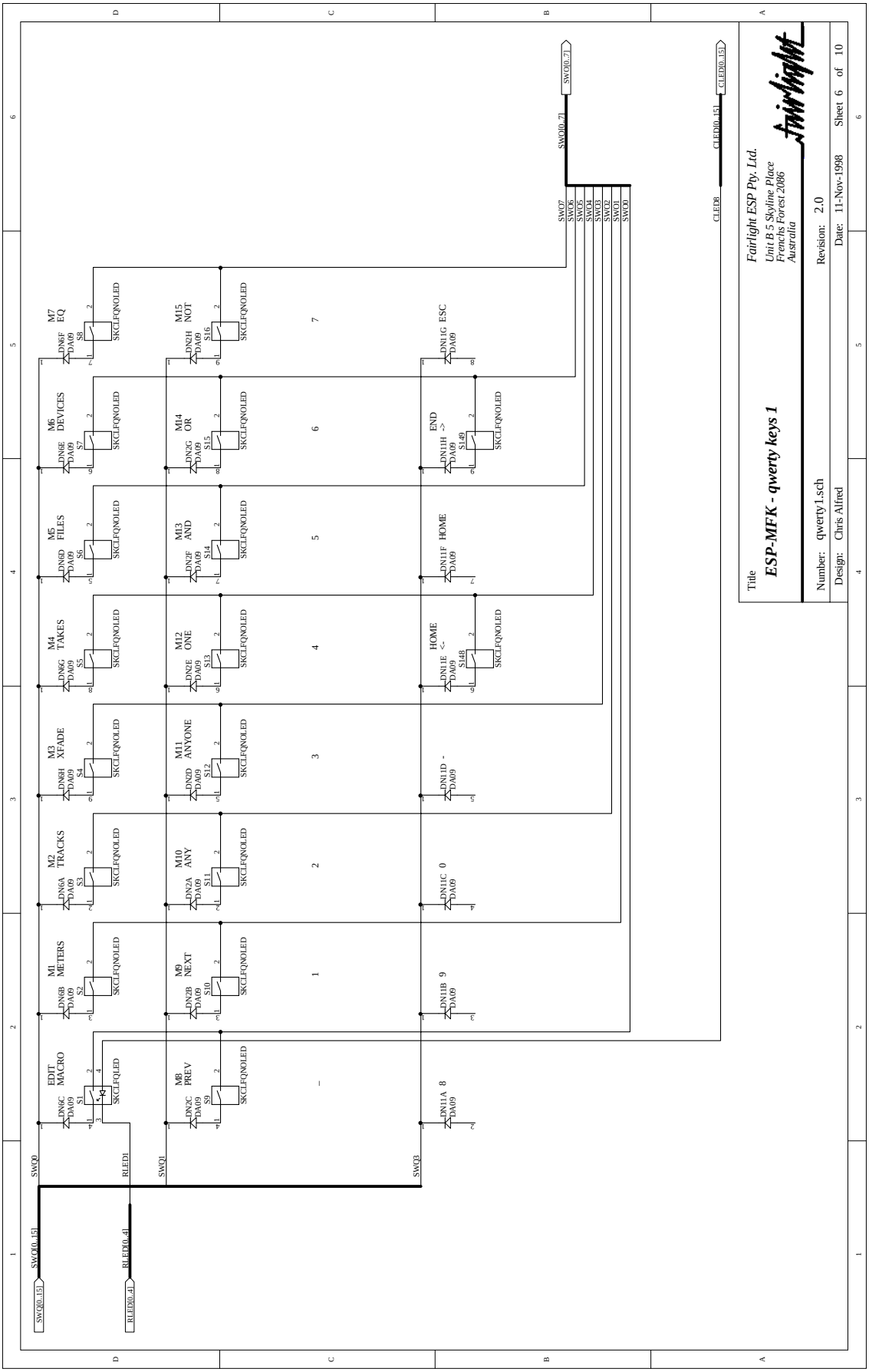


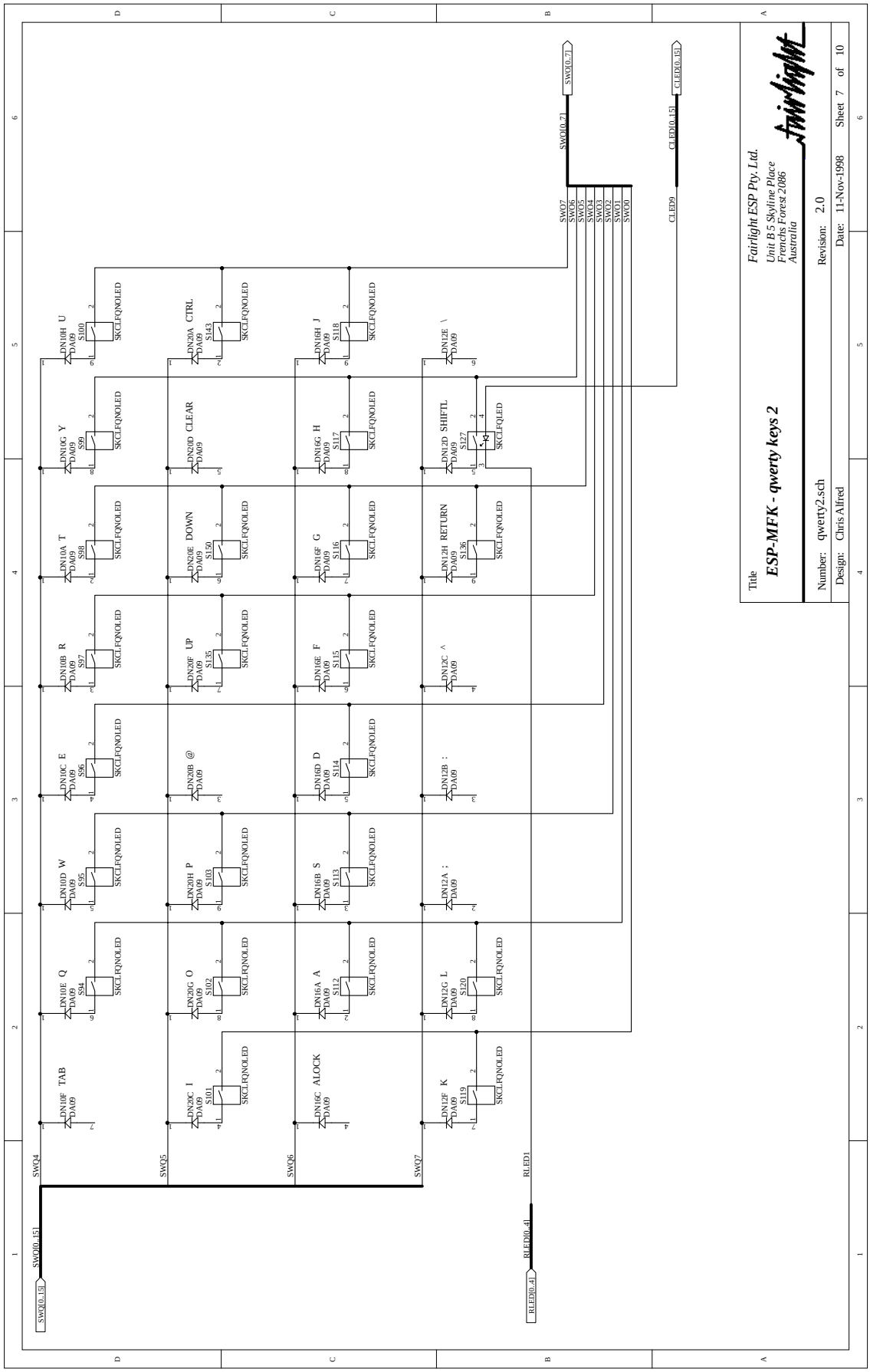

Fairlight ESP Pty. Ltd.
Unit B 5 Skyline Place
Frenchs Forest 2086
Australia
Title
ESP-MFK - panel keys 1
Number: panel1.sch
Revision: 2.0
Design: Chris Alfred
Date: 11-Nov-1998
Sheet 2 of 10
SWP[0..15]
RLED[0..4]
SW0[0..7]
CLED[0..15]
SUBV SOLO
DISAB MUTE
DIGI ARM
IMPORT PROJ
SPACE LEVEL
BUP FADE
NAME GRAB
TRACK BLOCK
TAKES NUDGE
WAVE EDIT
SOFT1
SOFT2
SHUT JOG
REW
SOFT3
FF
GPI ADR
PREROLL OFFSET
DOWN
MFX
GOTO
AUDIO BASE
PRINT GATE
EQ
PLAY
SOFT4
SOFT5
STOP
REC
PLAY MENU
SET LOOP
EDIT MARK

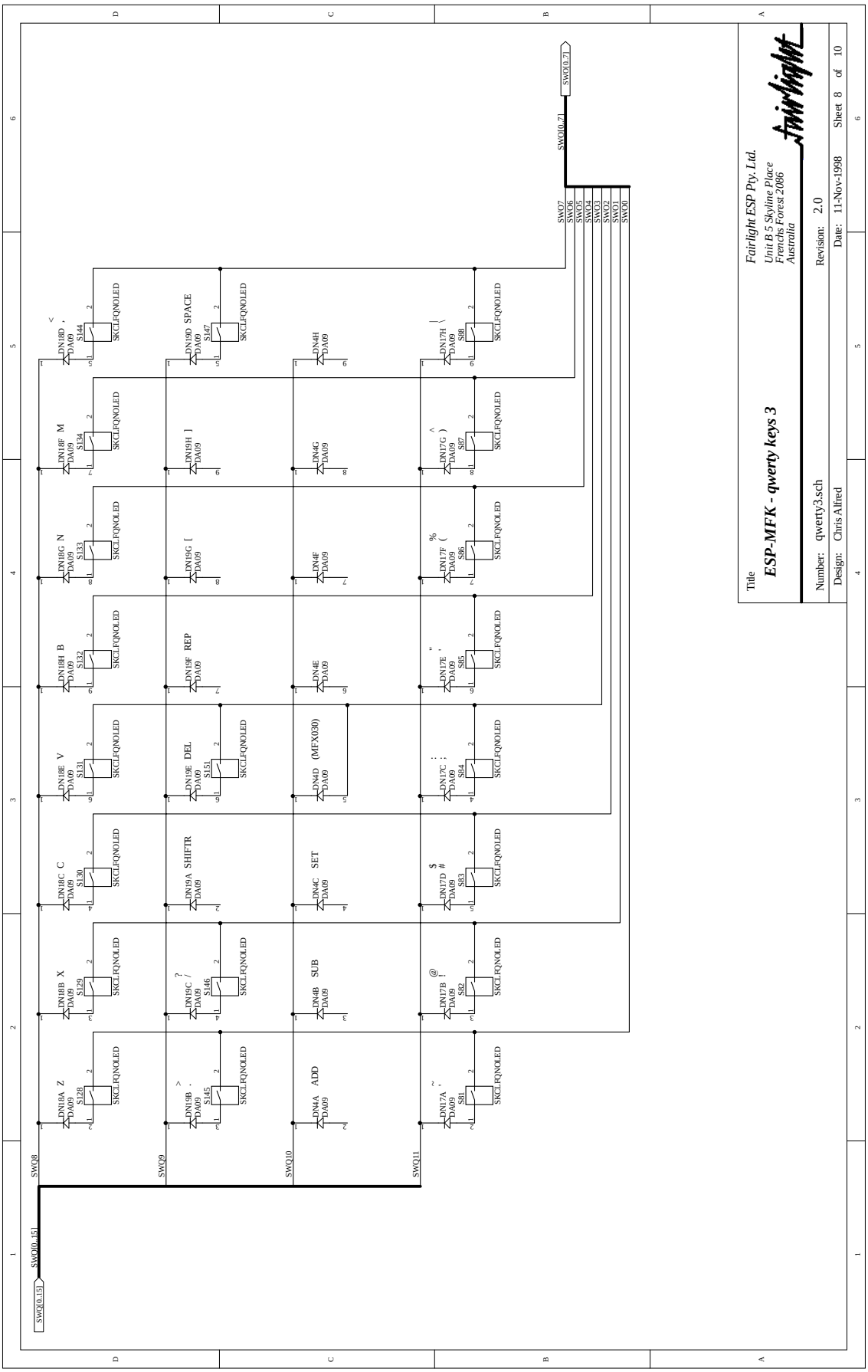

Title
ESP-MFK - panel keys 2
Fairlight ESP Pty. Ltd.
Unit B 5 Skyline Place
French's Forest 2086
Australia
Number: panel2.sch
Revision: 2.0
Design: Chris Alfred
Date: 11-Nov-1998
Sheet 3 of 10
SWP[0..15]
RLED[0..4]
SW0[0..7]
CLED[0..15]
SETUP M1
SETUP M2
SETUP GEN
DISK
UNDO
ZOOM
CLEAR
ENTER
<JUMP
JUMP>
FROM
TO
BLUE
SKCLFQLED
SKCLFQNOLED

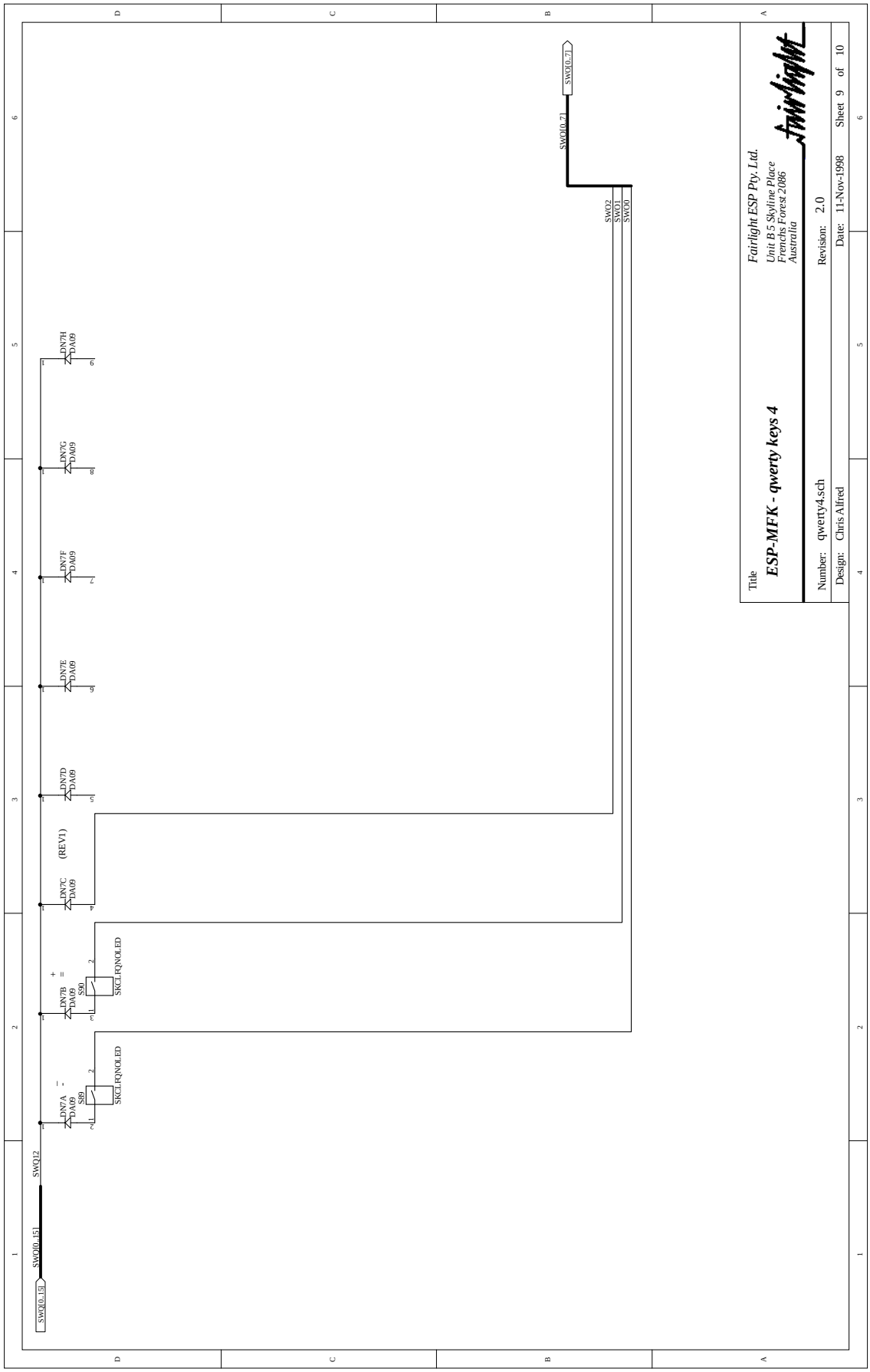

Fairlight ESP Pty. Ltd.
Unit B 5 Skyline Place
Frenchs Forest 2086
Australia
Title
ESP-MFK - panel keys 3
Number: panel3.sch
Revision: 2.0
Design: Chris Alfred
Date: 11-Nov-1998
Sheet 4 of 10
SWP0..15
RLED0..4
SWP8
SWP9
SWP10
SWP11
RLED0
RLED1
RLED4
SWO0..7
CLED0..15
TK1
TK2
TK3
TK4
TK5
TK6
TK7
TK8
TK9
TK10
TK11
TK12
TK13
TK14
TK15
TK16
TK17
TK18
TK19
TK20
TK21
TK22
TK23
TK24
B1
B2
B3
B4
M1
M2
M3
M4
SKCLFQLED

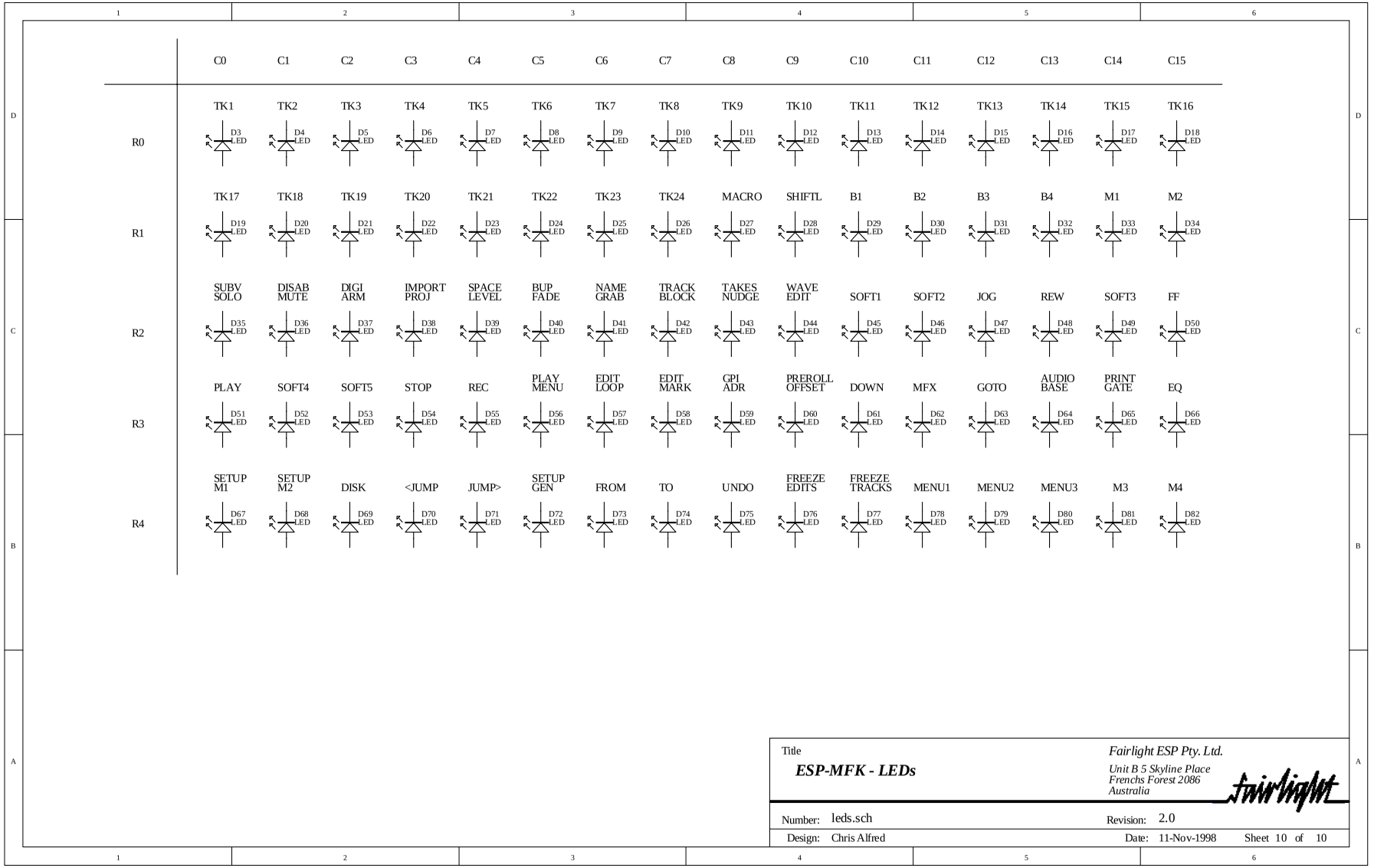

SWP[0..15]
RLED[0..4]
SWP12
SWP13
RLED4
RLED3
RLED4
SW0[0..7]
CLED[0..15]
SW06
SW05
SW04
SW03
SW02
SW01
SW00
CLED13
CLED12
CLED11
CLED10
CLED9
CLED7
CLED6
DN26E FROM S107
DN26B TO S108
DN26A EDIT LOOP S109
DN26C PREROLL OFFSET S110
DN26D EDIT MARK S111
DN26H FREEZE EDITS S157
DN26G FREEZE TRACKS S158
DN26F
DN14H MENU1 S56
DN14F MENU2 S72
DN14G MENU3 S73
DN14A (REV1)
DN14B
DN14C
DN14D
DN14E
SKCLFQLED
Fairlight ESP Pty. Ltd.
Unit B 5 Skyline Place
French's Forest 2086
Australia
Title
ESP-MFK - panel keys 4
Number: panel4.sch
Revision: 2.0
Design: Chris Alfred
Date: 11-Nov-1998
Sheet 5 of 10


Fairlight ESP Pty. Ltd.
Unit B 5 Skyline Place
Frenchs Forest 2086
Australia
Title
ESP-MFK - qwerty keys 1
Number: qwerty1.sch
Revision: 2.0
Design: Chris Alfred
Date: 11-Nov-1998
Sheet 6 of 10
SW[0..15]
RLED[0..4]
CLED[0..15]
M1 METERS
M2 TRACKS
M3 XFADE
M4 TAKES
M5 FILES
M6 DEVICES
M7 EQ
M8 PREV
M9 NEXT
M10 ANY
M11 ANYONE
M12 ONE
M13 AND
M14 OR
M15 NOT
EDIT MACRO
HOME
END
ESC
SKCLFQNOLED
SKCLFQLED


Fairlight ESP Pty. Ltd.
Unit B 5 Skyline Place
French's Forest 2086
Australia
Title
ESP-MFK - qwerty keys 2
Number: qwerty2.sch
Revision: 2.0
Design: Chris Alfred
Date: 11-Nov-1998
Sheet 7 of 10
SWQ[0..15]
SWQ04
SWQ05
SWQ06
SWQ07
SW0[0..15]
RLED[0..4]
RLED1
SW0[0..7]
CLED[0..15]
CLED9
SW07
SW06
SW05
SW04
SW03
SW02
SW01
SW00
DN10F TAB
DN10E Q
DN10D W
DN10C E
DN10B R
DN10A T
DN10G Y
DN10H U
DN20C I
DN20G O
DN20H P
DN20B @
DN20E UP
DN20D CLEAR
DN20A CTRL
DN16G ALOCK
DN16A A
DN16B S
DN16D D
DN16F F
DN16G G
DN16H H
DN16H J
DN12F K
DN12G L
DN12A ;
DN12B :
DN12C ^
DN12H RETURN
DN12D SHIFTL
DN12E \
SKCLFQNOLED
SKCLFQLED


SW[0..15]
SW[0..7]
SW08
SW09
SW10
SW11
SW07
SW06
SW05
SW04
SW03
SW02
SW01
SW00
Fairlight ESP Pty. Ltd.
Unit B 5 Skyline Place
Frenchs Forest 2086
Australia
Title
ESP-MFK - qwerty keys 3
Number: qwerty3.sch
Revision: 2.0
Design: Chris Alfred
Date: 11-Nov-1998
Sheet 8 of 10


SWO[0..7]
SWO[0..15]
SWO12
SWO[0..15]
SWO2
SW01
SW00
DN7A DA09
DN7B DA09
DN7C DA09
DN7D DA09
DN7E DA09
DN7F DA09
DN7G DA09
DN7H DA09
S89
S90
SKGLRQNOLED
SKGLRQNOLED
(REV1)
Title
ESP-MFK - qwerty keys 4
Number: qwerty4.sch
Revision: 2.0
Design: Chris Alfred
Date: 11-Nov-1998
Sheet 9 of 10
Fairlight ESP Pty. Ltd.
Unit B 5 Skyline Place
Frenchs Forest 2086
Australia


C0 C1 C2 C3 C4 C5 C6 C7 C8 C9 C10 C11 C12 C13 C14 C15
R0
TK1 TK2 TK3 TK4 TK5 TK6 TK7 TK8 TK9 TK10 TK11 TK12 TK13 TK14 TK15 TK16
D3 LED D4 LED D5 LED D6 LED D7 LED D8 LED D9 LED D10 LED D11 LED D12 LED D13 LED D14 LED D15 LED D16 LED D17 LED D18 LED
R1
TK17 TK18 TK19 TK20 TK21 TK22 TK23 TK24 MACRO SHIFTL B1 B2 B3 B4 M1 M2
D19 LED D20 LED D21 LED D22 LED D23 LED D24 LED D25 LED D26 LED D27 LED D28 LED D29 LED D30 LED D31 LED D32 LED D33 LED D34 LED
R2
SUBV SOLO DISAB MUTE DIGI ARM IMPORT PROJ SPACE LEVEL BUP FADE NAME GRAB TRACK BLOCK TAKES NUDGE WAVE EDIT SOFT1 SOFT2 JOG REW SOFT3 FF
D35 LED D36 LED D37 LED D38 LED D39 LED D40 LED D41 LED D42 LED D43 LED D44 LED D45 LED D46 LED D47 LED D48 LED D49 LED D50 LED
R3
PLAY SOFT4 SOFT5 STOP REC PLAY MENU EDIT LOOP EDIT MARK GPI ADR PREROLL OFFSET DOWN MFX GOTO AUDIO BASE PRINT GATE EQ
D51 LED D52 LED D53 LED D54 LED D55 LED D56 LED D57 LED D58 LED D59 LED D60 LED D61 LED D62 LED D63 LED D64 LED D65 LED D66 LED
R4
SETUP M1 SETUP M2 DISK <JUMP JUMP> SETUP GEN FROM TO UNDO FREEZE EDITS FREEZE TRACKS MENU1 MENU2 MENU3 M3 M4
D67 LED D68 LED D69 LED D70 LED D71 LED D72 LED D73 LED D74 LED D75 LED D76 LED D77 LED D78 LED D79 LED D80 LED D81 LED D82 LED
Title
ESP-MFK - LEDs
Fairlight ESP Pty. Ltd.
Unit B 5 Skyline Place
Frenchs Forest 2086
Australia
Number: leds.sch
Revision: 2.0
Design: Chris Alfred
Date: 11-Nov-1998
Sheet 10 of 10

26.0 MFX3 Specifications and Pinouts

26.1 Specifications

26.1.1 Analog Inputs and Outputs

Number:	24
Input impedence:	>10k Ohms
Output impedence:	< 55 Ohms
Maximum input level:	+22dBu
Maximum output level:	+22dBu
Input Gain range:	-96dB to +30dB
	(limited to +16dB by user interface)
	Swichable between -10dbV and +4dBu reference.
Through system SNR:	>89dB [Bandpass 22Hz - 22kHz]
Through system THD:	<0.01% typically 0.005% [Bandpass 22Hz - 22kHz]
Bandwidth (1dB):	20Hz to 20kHz
Sample rate:	32kHz -5% to 48kHz +5%
	(locked to sync source)
Internal sync crystals:	32kHz, 44.0559kHz, 44.1kHz, 48kHz

26.1.2 AES/EBU Inputs

Number:	12 (pairs)
Minimum differential:	200mV
Input impedence:	110 Ohms transformer isolated
Input frequency:	30kHz to 50kHz

MFX3 is insensitive to channel status.

26.1.3 SPDIF Inputs

Number:	12 (pairs)
Minimum level:	200mV
Input impedence:	75 Ohms
Input frequency:	30kHz to 50kHz

MFX3 is insensitive to channel status.

26.1.4 AES/EBU Outputs

Number:	12 (pairs)
Output level:	4V
Output impedence:	110 Ohms transformer isolated
Output frequency:	32kHz -5% to 48kHz +5%
	(locked to sync source)

26.1.5 SPDIF Outputs

Number:	12 (pairs)
Output level:	0.5V
Output impedence:	75 Ohms
Output frequency:	32kHz -5% to 48kHz +5%
	(locked to sync source)

26.1.6 Digital Output Channel Status

SPDIF	Digital Audio
	Copy prohibit (controlled from user interface)
	No pre-emphasis
AES/EBU	Professional
	Normal Audio
	Source Locked
	Sample Frequency set to project sample rate
	Stereophonic
	24bit word length

Note: The channel status is globally selected from the user interface BLUE-Digi menu OUTPUT submenu.

26.1.7 ESP-DIO serial interface

Baud rate:	19200
Format:	8 bits, 1 stop bit, no parity, RS232

26.1.8 LTC Inputs

Number:	2
Input level:	-20dBu to +10dBu
Input impedence:	>10k Ohms
Input rate:	1/80 x playspeed to 30 x playspeed

26.1.9 LTC Output

Output level:	0dBu
Output impedence:	33 Ohms
Output rate:	locked to playback rate

26.1.10 AES Sync input

Minimum differential:	200mV
Input impedence:	110 Ohms transformer isolated
Input frequency:	30kHz to 50kHz

MFX3 is insensitive to channel status.

26.1.11 AES Sync output

Output level:	4V
Output impedence:	110 Ohms transformer isolated
Output frequency:	32kHz -5% to 48kHz +5%
	(locked to sync source)
Data:	Digital zeroes
Channel Status:	Professional
	Normal Audio
	Source Locked
	Sample Frequency set to project rate Stereophonic
	24bit word length

26.1.12 MIDI inputs and outputs

Standard

26.1.13 Video Sync/ VITC input

Note: VITC Input is <u>not</u> currently supported

Impedence:	75 Ohms terminated
Level:	0.5V to 2V
Field rate:	24Hz -5% to 60Hz +5%

26.1.14 Sony Slave

Standard

26.1.15 Sony Master

Standard

26.1.16 GPO

Output type:	Open collector
Maximum voltage:	30V
Maximum current:	40mA

26.1.17 RS232

Standard (same as Personal Computer)

26.1.18 Word clock in

Input impedence:	75 Ohms optically isolated
Input frequency:	32kHz -5% to 48kHz +5%

26.1.19 Word clock output

Output drive:	75 Ohms load
Output frequency:	32kHz -5% to 48kHz +5%
	(locked to sync source)

26.2 Pinout Information

26.2.1 Analogue Inputs

Connectors	1x 15 pin D-mini Female
Input	Balanced
Input level	+22 dBu max
Input sensitivity	-10 dBu / +4 dBu switched
Input attenuation range	14 dB to -99 dB
Input impedance	> 10K ohm
Pin 1	Frame Ground
Pin 2	IN 1 GND
Pin 3	IN 2+
Pin 4	IN 2-
Pin 5	IN 3 GND
Pin 6	IN 4+
Pin 7	IN 4-
Pin 8	NC
Pin 9	IN 1+
Pin 10	IN 1-
Pin 11	IN 2 GND
Pin 12	IN 3+
Pin 13	IN 3-
Pin 14	IN 4 GND
Pin 15	NC

Audio input cables should be wired using male connectors as the MFX input is a female connector as seen below.

26.2.2 AnalogueOutputs

Connectors	1x 15 Pin D-mini Male
Output	Electronic Balanced Differential
Output Level	+22 dBu max at 0 dB digital full scale (nominal +4 dBu)
Output impedance	< 55 ohms
Output load	600 ohms minimum
Pin 1	Frame GND
Pin 2	OUT 1 GND
Pin 3	OUT 2 +
Pin 4	OUT 2 -
Pin 5	OUT 3 GND
Pin 6	OUT 4 +
Pin 7	OUT 4 -
Pin 8	NC
Pin 9	OUT 1 +
Pin 10	OUT 1 -
Pin 11	OUT 2 GND
Pin 12	OUT 3 +
Pin 13	OUT 3 -
Pin 14	OUT 4 GND
Pin 15	NC

Audio output cables should be wired using female connectors as the MFX output is a male connector as seen below.

26.2.3 AES / EBU INPUT

Connector	37 way D-mini Female
Channels	2 x Stereo pairs per I/O Module
Sample Rates	44.1 KHz , 48.0 KHz, 32 KHz, 44.056 KHz
Input Type	200 mv Differential Minimum
Input Level	+22 dBu Peak
Pin 17	AES IN 1 GND
Pin 18	AES IN 2-
Pin 19	AES IN 2+
Pin 35	AES IN 1-
Pin 36	AES IN 1+
Pin 37	AES IN 2 GND

26.2.3 AES / EBU OUTPUT

Connector	37 way D-mini Female
Channels	2 x Stereo pairs per I/O Module
Sample Rates	44.1 KHz, 48 KHz, 32 KHz, 44.056 KHZ
Output level	4.3v Minimum
Pin 14	AES OUT 1 GND
Pin 15	AES OUT 1-
Pin 16	AES OUT 1+
Pin 32	AES OUT 2-
Pin 33	AES OUT 2+
Pin 34	AES OUT 2 GND

26.2.4 SPDIF INPUT

Connector	37 way D-mini Female
Channels	2 x Stereo pairs per I/O Module
Sample Rates	44.1 KHz, 48 KHz, 32 KHz, 44.056 KHz
Input level	200 mv minimum
Pin 12	SPDIF IN 1
Pin 13	SPDIF IN 2
Pin 30	SPDIF IN 1 GND
Pin 31	SPDIF IN 2 GND

26.2.5 SPDIF OUTPUT

Connector	37 way D-mini Female
Channels	2 Stereo pairs per I/O Module
Sample Rates	44.1 KHz, 48 KHz, 32 KHz, 44.056 KHz
Output Level	0.5v p-p
Pin 10	SPDIF OUT 1
Pin 11	SPDIF OUT 2
Pin 28	SPDIF OUT 1 GND
Pin 29	SPDIF OUT 2 GND

26.2.6 GROUND & NO CONNECTIONS

Connector	37 way D-mini Female
Pin 1	GND
Pin 2	NC
Pin 3	NC
Pin 4	NC
Pin 5	NC
Pin 6	NC
Pin 20	NC
Pin 21	NC
Pin 22	NC
Pin 23	NC
Pin 24	NC

Use male connector when assembling cable looms.

26.2.7 LTCA AND LTCB INPUTS

XLR Female	-20 dBm to +10 dBm
Pin 1	GND
Pin 2	IN +
Pin 3	IN -

IMPORTANT NOTE: Unbalanced loads should be connected to Pin 1 Ground and Pin 3 Signal. Pin 2 should not be connected to ground.

26.2.8 LTC OUTPUT

XLR Male	0 dBm
Pin 1	GND
Pin 2	OUT+
Pin 3	OUT -

26.2.9 AES SYNC INPUT

XLR Female

Pin 1	GND
Pin 2	IN +
Pin 3	IN-

26.2.10 AES SYNC OUT

XLR Male

Pin 1	GND
Pin 2	OUT +
Pin 3	OUT -

26.2.11 MIDI

MIDI IN A, MIDI IN B, MIDI IN C, MIDI IN D

5 pin DIN 180

Pin 1	NC
Pin 2	NC
Pin 3	NC
Pin 4	IN+
Pin 5	IN-

MIDI OUT A, MIDI OUT B, MIDI OUT C, MIDI OUT D

5 pin DIN 180

Pin 1	NC
Pin 2	GND
Pin 3	NC
Pin 4	OUT+
Pin 5	OUT-

26.2.12 Video Sync Input

BNC 1v p-p 75 Ohms terminated

26.2.13 Mfx In and Mfx Out

MFX IN and MFX OUT are not currently used.

MFX OUT		MFX IN	
DB15 VGA Female		DB15 VGA Female	
Pin 1	GND	Pin 1	GND
Pin 2	TXS-	Pin 2	RXM-
Pin 3	RXS-	Pin 3	TXM-
Pin 4	ZTPS-	Pin 4	ZTPM-
Pin 5	WCLKS-	Pin 5	WCLKM-
Pin 6	NC	Pin 6	NC
Pin 7	TXS+	Pin 7	RXM+
Pin 8	RXM+	Pin 8	TXM+
Pin 9	ZTPS+	Pin 9	ZTPM+
Pin 10	WCLKS+	Pin 10	WCLKM+
Pin 11	NC	Pin 11	NC
Pin 12	NC	Pin 12	NC
Pin 13	NC	Pin 13	NC
Pin 14	NC	Pin 14	NC
Pin 15	NC	Pin 15	NC

26.2.14 9-Pin

SONY A, SONY B		SONY SLAVE	
DB9 Male		DB9 Female	
Pin 1	GND	Pin 1	GND
Pin 2	TX-	Pin 2	RX-
Pin 3	RX+	Pin 3	TX+
Pin 4	GND	Pin 4	GND
Pin 5	Frame sync	Pin 5	Frame sync
Pin 6	GND	Pin 6	GND
Pin 7	TX+	Pin 7	RX+
Pin 8	RX-	Pin 8	TX-
Pin 9	GND	Pin 9	GND

26.2.15 WCLK IN

word clock sync TTL input

BNC	1 HCMOS load

26.2.16 WCLK OUT

word clock sync TTL output

BNC	max 1 TTL load

26.2.17 VITC IN

Note: VITC is not currently supported.

BNC	1v p-p, 75 Ohms terminated

26.2.18 General Purpose Outputs

DB9 Male Open Collector 30v max, 40 mA max

Pin 1	GND
Pin 2	GPO1
Pin 3	GPO2
Pin 4	GPO3
Pin 5	GPO4
Pin 6	GPO5
Pin 7	GPO6
Pin 8	GPO7
Pin 9	GPO8

26.2.19 Serial Port (RS232)

DB9 Male	RS232
Pin 1	NC
Pin 2	RX
Pin 3	TX
Pin 4	DTR
Pin 5	GND
Pin 6	DSR
Pin 7	RTS
Pin 8	CTS
Pin 9	NC (RI)

26.2.20 SCSI Interface

Single ended SCSI port	50 way Centronics

26.2.21 MFX CONSOLE CONNECTION

Centronics 24 pin Female

Pin 1	Gnd	Pin 13	Gnd
Pin 2	N/C	Pin 14	Gnd
Pin 3	N/C	Pin 15	N/C
Pin 4	N/C	Pin 16	Gnd
Pin 5	TX422+	Pin 17	TX422-
Pin 6	RX422+	Pin 18	RX422-
Pin 7	KEY+	Pin 19	KEY-
Pin 8	MFX Sense	Pin 20	N/C
Pin 9	MIDI OUT+	Pin 21	MIDI OUT-
Pin 10	MIDI IN+	Pin 22	MIDI IN-
Pin 11	KBD232	Pin 23	NC
Pin 12	Data 1	Pin 24	Data 2

26.2.22 VIDEO MONITOR

VGA video	512 x 512 resolution
DB15 VGA Female	Hsync 31.250kHz Vsync 50Hz Bandwidth 20MHz
Pin 1	RED
Pin 2	GREEN
Pin 3	BLUE
Pin 4	GND
Pin 5	GND
Pin 6	GND
Pin 7	GND
Pin 8	GND
Pin 9	NC
Pin 10	GND
Pin 11	GND
Pin 12	NC
Pin 13	HSYNC
Pin 14	VSYNC
Pin 15	NC

26.2.23 PRINTER

Baud-Rate 38400 or 9600, 8 bits, 1 stop bit, No Parity. SERIAL INPUT printers ONLY. EPSON ESC/P - 9 pin protocol or ESC/P2 - 24 pin protocol (preferred).

Serial cable when using DTR handshaking:

Fairlight		Printer	
Sync I/O RS232	D9 Male	D25	
Pin	Name	Pin	Name
1	N/C		
2	RxD	2	TxD
3	TxD	3	RxD
4	DTR	6	DSR
5	Gnd	7	Gnd
6	DSR	20	DTR
7	RTS	5	CTS
8	CTS	4	RTS
9	N/C		

All other pins unused.

When using XON/XOFF handshaking, a Null Modem cable should be used.

To change the printer configuration, type <esc> 'S' from the Disk Recorder. Change the printer parameters with the mouse.

26.2.24 MFX Console Pinouts

Centronics 24 pin Female

Pin 1	Gnd		
Pin 2	N/C	Pin 20	Gnd
Pin 3	N/C	Pin 21	Gnd
Pin 4	N/C	Pin 22	N/C
Pin 5	N/C	Pin 23	Gnd
Pin 6	Data 1	Pin 24	Data 2
Pin 7	KBD232	Pin 25	N/C
Pin 8	MIDI OUT +	Pin 26	MIDI OUT -
Pin 9	MIDI IN +	Pin 27	MIDI IN -
Pin 10	Gnd	Pin 28	SYSC
Pin 11	Key +	Pin 29	Key -
Pin 12	TX 422 +	Pin 30	TX 422 -
Pin 13	RX 422 +	Pin 31	RX 422 -
Pin 14	N/C	Pin 32	N/C
Pin 15	N/C	Pin 33	Gnd
Pin 16	N/C	Pin 34	N/C
Pin 17	N/C	Pin 35	N/C
Pin 18	N/C	Pin 36	Remote RX
Pin 19	N/C	Pin 37	Remote TX

27.0 Software

27.1 Application Components

The MFX3plus is divided up into approximately 32 directories and about 572 files. The root level directory on of a MFX3plus boot drive contains 6 files that are required to run the application. The number of files and directories varies from release to release.

In revision 14, the root level directory is also where projects (.MT files) are found. Due to the connectivity features in revision 15, the project page displays files of all types, not just .MT files. Even though the root level directory on a rev 15 drive can contain projects, many users prefer to keep projects in separate directories to make the project page display easier to navigate for projects. It is important to keep this in mind when attempting file maintenance or repair on a revision 15 boot drive.

The files listed below can be found starting from root level directory of an RBF disk with the MFX3Plus application installed. All files are required by the system, some information may accompany them in the list.

dd.bf
Disk Bootfile
startup.dev
Development Startup
startup.user
Customer's startup file
startup.osk30
OSK30 Startup File
release.list
Release list for file release
machine
Machine ID Detection
CMDS/attr
CMDS/break
CMDS/cio
CMDS/cmp
CMDS/code
CMDS/com
CMDS/compress
CMDS/copy
CMDS/csl
CMDS/date
CMDS/dcheck
CMDS/deiniz
CMDS/del
CMDS/deldir
CMDS/devs
CMDS/dir
CMDS/dird
CMDS/diskcache
CMDS/dsave
CMDS/dump
CMDS/echo
CMDS/events
CMDS/format
CMDS/free
CMDS/fixmod
CMDS/frestore
CMDS/fsave
CMDS/grep
CMDS/ident
CMDS/iniz
CMDS/irqs
CMDS/link
CMDS/list
CMDS/load
CMDS/login
CMDS/kermit
CMDS/makdir
CMDS/make
CMDS/math881
CMDS/mdir
CMDS/mfree
CMDS/moded
CMDS/os9gen
CMDS/p2init
CMDS/partdgen
CMDS/paths
CMDS/pd
CMDS/printenv
CMDS/procs
CMDS/rename
CMDS/save
CMDS/setime
CMDS/shell
CMDS/sleep
CMDS/tape
CMDS/tapegen
CMDS/tapestart
CMDS/tee
CMDS/touch
CMDS/tmode
CMDS/tsmon

CMDS/umacs
CMDS/unlink
CMDS/xmode
CMDS/BOOTOBJS/nil
CMDS/BOOTOBJS/null
CMDS/BOOTOBJS/pcf
CMDS/BOOTOBJS/pipe
CMDS/BOOTOBJS/pipe2
CMDS/BOOTOBJS/pipeman
CMDS/BOOTOBJS/ram
CMDS/BOOTOBJS/rbsccs
CMDS/BOOTOBJS/rbvccs
CMDS/BOOTOBJS/sbf
SYS/errmsg
SYS/loadisp
SYS/moded.fields
SYS/motd
SYS/password.release
SYS/qsys.cfg
SYS/startisp
SYS/startnfs.client
SYS/startnfs.server
SYS/termcap
USR/PIX/5pt.font
USR/PIX/8pt.font
USR/PIX/9pt.font
USR/PIX/LED.font
USR/PIX/fame.ras
USR/PIX/logo.bit
USR/PIX/mfx3.ras
USR/PIX/padlock.bit
USR/PIX/padlock.pix
USR/PIX/files.pix
USR/PIX/redtick.pix
USR/.login
USR/CMDS/abpublish
USR/CMDS/abupgrade
USR/CMDS/abdelete
USR/CMDS/abdebug
USR/CMDS/amd
USR/CMDS/ash
USR/CMDS/bdd
USR/CMDS/befame
USR/CMDS/befameold
USR/CMDS/belogin
USR/CMDS/bemfx
USR/CMDS/beshell
USR/CMDS/bogomips
USR/CMDS/bootgen
USR/CMDS/bsh
USR/CMDS/cdw
USR/CMDS/chown
USR/CMDS/comms
USR/CMDS/crc
USR/CMDS/dcc
USR/CMDS/dccdump
USR/CMDS/df
USR/CMDS/dfn_backup
USR/CMDS/dfn_tbackup
USR/CMDS/dfnserver
USR/CMDS/dgt00x00_000
USR/CMDS/differ
USR/CMDS/dinfo
USR/CMDS/diskinit
USR/CMDS/drt
USR/CMDS/dtst
USR/CMDS/dubchart
USR/CMDS/dvcs
USR/CMDS/e
USR/CMDS/ed
USR/CMDS/errmesg
USR/CMDS/erx
USR/CMDS/espfind
USR/CMDS/esprz
USR/CMDS/espsz
USR/CMDS/fame
USR/CMDS/fame2
USR/CMDS/famesession
USR/CMDS/famesession2
USR/CMDS/fametest
USR/CMDS/fdtool
USR/CMDS/ffs
USR/CMDS/file_gopher
USR/CMDS/find
USR/CMDS/fromfame
USR/CMDS/gfx
USR/CMDS/gfxconfirm
USR/CMDS/gfxdisp
USR/CMDS/gfxecho
USR/CMDS/gfxenter
USR/CMDS/gfxglob
USR/CMDS/gfxio
USR/CMDS/gfxkeymouse
USR/CMDS/gfxlaunch
USR/CMDS/gfxram
USR/CMDS/gfxsub
USR/CMDS/gfxterm
USR/CMDS/gfxtvt
USR/CMDS/gfxwm
USR/CMDS/globals
USR/CMDS/gzip
USR/CMDS/httpd
USR/CMDS/iestat
USR/CMDS/ifconfig
USR/CMDS/inq
USR/CMDS/iopack
USR/CMDS/ipilinks
USR/CMDS/ipis
USR/CMDS/kill_espmsg
USR/CMDS/ksh
USR/CMDS/lha
USR/CMDS/lharc
USR/CMDS/list_espmsg
USR/CMDS/lpr

USR/CMDS/lzw
USR/CMDS/march
USR/CMDS/mdrcheck
USR/CMDS/mdrmsg
USR/CMDS/mdrstart
USR/CMDS/mdump
USR/CMDS/mediad
USR/CMDS/mfx3
USR/CMDS/mfxecho
USR/CMDS/mfxload
USR/CMDS/mfxmouse
USR/CMDS/mfxsession
USR/CMDS/mfxstart
USR/CMDS/mfxstartf
USR/CMDS/mfxstartf2
USR/CMDS/mfxstartft
USR/CMDS/mlist
USR/CMDS/monitor
USR/CMDS/move
USR/CMDS/mrestore
USR/CMDS/mutexes
USR/CMDS/mxtest
USR/CMDS/opt
Utility for creating the MFX3 releases
USR/CMDS/patch
USR/CMDS/ped
USR/CMDS/mfxping
USR/CMDS/qmfxtest
USR/CMDS/qrun
USR/CMDS/qserver
USR/CMDS/qshutdown
USR/CMDS/qstart
USR/CMDS/qtvtlog
USR/CMDS/qtvtmsg
USR/CMDS/qtvttest
USR/CMDS/recache
USR/CMDS/restart
USR/CMDS/rz
USR/CMDS/scct
USR/CMDS/scrun
USR/CMDS/scsidm
USR/CMDS/scsiread
USR/CMDS/semas
USR/CMDS/send
USR/CMDS/services
USR/CMDS/session
USR/CMDS/setblksiz
USR/CMDS/setsys
USR/CMDS/soconfig
USR/CMDS/space
USR/CMDS/start_espmsg
USR/CMDS/su
USR/CMDS/sysinfo
USR/CMDS/sysmesg
USR/CMDS/sysmon
USR/CMDS/sz
USR/CMDS/tapemode
USR/CMDS/tar
USR/CMDS/tcopy
USR/CMDS/telix
USR/CMDS/timer
USR/CMDS/tod_pd
USR/CMDS/tofame
USR/CMDS/totvt
USR/CMDS/trace
USR/CMDS/traw
USR/CMDS/tree
USR/CMDS/tvtsave
USR/CMDS/tvtemu
USR/CMDS/tvterm
USR/CMDS/unwrap
USR/CMDS/upgrade
MFX Software upgrade utility
USR/CMDS/uudecode
USR/CMDS/uuencode
USR/CMDS/ved
USR/CMDS/viddy
USR/CMDS/wrap
USR/CMDS/xcg3
USR/CMDS/xrelease
Utility for creating the MFX3 releases
USR/CMDS/z
USR/CMDS/noded
USR/CMDS_WX/cg4diag
USR/CMDS_WX/cg4test
USR/CMDS_WX/dccdiag
USR/CMDS_WX/flash
USR/CMDS_WX/hssltest
USR/CMDS_WX/mmu
USR/CMDS_WX/osk30
USR/CMDS_WX/osk30_disk
USR/CMDS_WX/osk30_video
USR/CMDS_WX/osk30_kbd
USR/CMDS_WX/setup
USR/CMDS_WX/scanpci
USR/CMDS_WX/scsicache
USR/CMDS_WX/termmode
USR/CMDS_WX/xload
USR/CMDS_WX/netstart
USR/CMDS_WX/enesppci
USR/CMDS_WX/BOOTOBJS/bigram
USR/CMDS_WX/BOOTOBJS/com0
USR/CMDS_WX/BOOTOBJS/dbug
USR/CMDS_WX/BOOTOBJS/dongle
USR/CMDS_WX/BOOTOBJS/esptrap
USR/CMDS_WX/BOOTOBJS/exabyte_1024
USR/CMDS_WX/BOOTOBJS/exabyte_512
USR/CMDS_WX/BOOTOBJS/fame232
USR/CMDS_WX/BOOTOBJS/flight
USR/CMDS_WX/BOOTOBJS/frommfx
USR/CMDS_WX/BOOTOBJS/hssl
USR/CMDS_WX/BOOTOBJS/hs0
USR/CMDS_WX/BOOTOBJS/hs1
USR/CMDS_WX/BOOTOBJS/ie0_WS
USR/CMDS_WX/BOOTOBJS/ifws

USR/CMDS_WX/BOOTOBJS/ipconfig
USR/CMDS_WX/BOOTOBJS/irqcount
USR/CMDS_WX/BOOTOBJS/macfm
USR/CMDS_WX/BOOTOBJS/mdrfm
USR/CMDS_WX/BOOTOBJS/mfx232
USR/CMDS_WX/BOOTOBJS/mfxd
USR/CMDS_WX/BOOTOBJS/mouse
USR/CMDS_WX/BOOTOBJS/moused
USR/CMDS_WX/BOOTOBJS/flfs
USR/CMDS_WX/BOOTOBJS/nvr
USR/CMDS_WX/BOOTOBJS/nvramd
USR/CMDS_WX/BOOTOBJS/osksyscalls
USR/CMDS_WX/BOOTOBJS/p1
USR/CMDS_WX/BOOTOBJS/p2
USR/CMDS_WX/BOOTOBJS/qc
USR/CMDS_WX/BOOTOBJS/qssd
USR/CMDS_WX/BOOTOBJS/qterm
USR/CMDS_WX/BOOTOBJS/pc
USR/CMDS_WX/BOOTOBJS/r0
USR/CMDS_WX/BOOTOBJS/r1
USR/CMDS_WX/BOOTOBJS/rbgen
USR/CMDS_WX/BOOTOBJS/rbuccs
USR/CMDS_WX/BOOTOBJS/scsd
USR/CMDS_WX/BOOTOBJS/sysmbuf
USR/CMDS_WX/BOOTOBJS/tomfx
USR/CMDS_WX/BOOTOBJS/ts
USR/CMDS_WX/BOOTOBJS/tvt
USR/CMDS_WX/BOOTOBJS/tvtctrl
USR/CMDS_WX/BOOTOBJS/tvtd
USR/CMDS_WX/BOOTOBJS/esppcid
USR/CMDS_WX/BOOTOBJS/netman
USR/CMDS_WX/BOOTOBJS/netd
USR/CMDS_WX/BOOTOBJS/net82557
USR/CMDS_WX/BOOTOBJS/if82557
USR/CMDS_WX/BOOTOBJS/hostfm
USR/CMDS_WX/BOOTOBJS/anetd
USR/CMDS_WX/BOOTOBJS/wvf
USR/CMDS_WX/BOOTOBJS/akaifm
USR/CMDS/MFX/all_play
USR/CMDS/MFX/beeps
USR/CMDS/MFX/consoled
USR/CMDS/MFX/edump
USR/CMDS/MFX/fd
USR/CMDS/MFX/fdef
USR/CMDS/MFX/filex
USR/CMDS/MFX/ibm
USR/CMDS/MFX/inputs
USR/CMDS/MFX/gfxabase
USR/CMDS/MFX/law
USR/CMDS/MFX/ls
USR/CMDS/MFX/m
USR/CMDS/MFX/mdl
USR/CMDS/MFX/mdrccq_pb
USR/CMDS/MFX/mdrdcc
USR/CMDS/MFX/mdrdevice_pb
USR/CMDS/MFX/mdreq_pb
USR/CMDS/MFX/mdrextfiles_pb
USR/CMDS/MFX/mdrfade_pb
USR/CMDS/MFX/mdrfiles_pa
USR/CMDS/MFX/mdrfs
USR/CMDS/MFX/mdrint
USR/CMDS/MFX/mdrioq_pb
USR/CMDS/MFX/mdrlevel_pb
USR/CMDS/MFX/mdrmarks_pb
USR/CMDS/MFX/mdrmpatch_pa
USR/CMDS/MFX/mdrname_pa
USR/CMDS/MFX/mdrpassword_pb
USR/CMDS/MFX/mdrpatch_pa
USR/CMDS/MFX/mdrrtfx_pb
USR/CMDS/MFX/mdrscitask
USR/CMDS/MFX/mdrtake_pb
USR/CMDS/MFX/mdrtracks_pa
USR/CMDS/MFX/mdruser_pa
USR/CMDS/MFX/mdrwaves_pb
USR/CMDS/MFX/mdrwavex_pb
USR/CMDS/MFX/mdrwavi_pb
USR/CMDS/MFX/mdrwfld
USR/CMDS/MFX/mdrwsmain
USR/CMDS/MFX/mdrwsplay
USR/CMDS/MFX/mfxack
USR/CMDS/MFX/mfxalready
USR/CMDS/MFX/mfxdump
USR/CMDS/MFX/mfxkey
USR/CMDS/MFX/mix
USR/CMDS/MFX/mixint
USR/CMDS/MFX/mxr
USR/CMDS/MFX/noinputs
USR/CMDS/MFX/omdlexport
USR/CMDS/MFX/out24
USR/CMDS/MFX/quit
USR/CMDS/MFX/readakai
USR/CMDS/MFX/password
USR/CMDS/MFX/readomf
USR/CMDS/MFX/readwvf
USR/CMDS/MFX/recdata
USR/CMDS/MFX/red
USR/CMDS/MFX/redbook
USR/CMDS/MFX/rtb
USR/CMDS/MFX/rw
USR/CMDS/MFX/stop
USR/CMDS/MFX/swap
USR/CMDS/MFX/tcs_start
USR/CMDS/MFX/topwin_pc
USR/CMDS/MFX/ver
USR/CMDS/MFX/wavi
USR/CMDS/MFX/wavx
USR/CMDS/MFX/wd
USR/CMDS/MFX/ws
USR/CMDS/MFX/wvfs
USR/CMDS/MFX/feather
USR/DCC/dilate.bin
USR/DCC/gain.bin
USR/DCC/mdr.bin
USR/DCC/mdx.bin

USR/DCC/mix.bin
USR/MFX/.login
USR/MFX/abase.form
USR/MFX/abase.pform
USR/MFX/mfx.raw
USR/MFX/mfk.raw
USR/MFX/mfk2.raw
USR/MFX/mfx.dummy
USR/QSYS/diotask
USR/QSYS/qctest
USR/QSYS/qmfx
USR/QSYS/qmfxcomms
USR/QSYS/qmidia
USR/QSYS/qprocs
USR/QSYS/qprinter
USR/QSYS/qshell
USR/QSYS/qsonic
USR/QSYS/qsys
USR/SC/.login
USR/SC/CMDS/scdiag
USR/SC/CMDS/BOOTOBJS/osk30kernel
USR/QSYS/TCS/cman
USR/QSYS/TCS/dman
USR/QSYS/TCS/dman_sony
USR/QSYS/TCS/gengen
USR/QSYS/TCS/ltcrdr
USR/QSYS/TCS/mdr
USR/QSYS/TCS/tbase
USR/QSYS/TCS/tcsmain
USR/QSYS/TCS/tman
USR/DIO/dioprog.s
USR/ESPPCI/pciwfm.lod
USR/ESPPCI/V4/pciwfm.lod
USR/ESPPCI/V5/pciwfm.lod
USR/ROMS/app1rom
USR/ROMS/app2rom
USR/ROMS/blowall
USR/ROMS/checkall
USR/ROMS/wxrom
USR/ROOT/.history
USR/ROOT/.login
USR/ROOT/.shellrc
USR/SYS/make.host.template
USR/SYS/dfn_cfg
USR/SYS/image.pal
USR/SYS/mdr_cfg
USR/SYS/mdr_data
USR/SYS/mdr_pages
USR/SYS/mfx_copyright
USR/SYS/mfx_version
USR/SYS/mfxenviron
USR/SYS/mfxready.bin
USR/SYS/setup
USR/SYS/sony_id
USR/SYS/system.pal
USR/SYS/tcs_cfg
USR/XILINX/x_dcc.bin
USR/XILINX/x_pll.bin
USR/XILINX/x_pll16.bin
USR/XILINX/x_pll17.bin
USR/XILINX/x_pll18.bin
USR/XILINX/x_syn.bin
USR/XILINX/ADDRESS.bin
USR/XILINX/AXDATA.bin
USR/XILINX/AXDATA2.bin
USR/XILINX/DXDATA.bin
USR/XILINX/DXTEST1.bin
USR/XILINX/DXTEST2.bin
USR/XILINX/REGISTER.bin
USR/XILINX/VIDADD.bin
USR/XILINX/wb.bin
USR/XILINX/wbgs.bin
USR/XILINX/wbgb.bin
USR/XILINX/wbgsp.bin
USR/XILINX/wbgbp.bin
CMDS/arpstat
CMDS/exportfs
CMDS/ftp
CMDS/ftpd
CMDS/ftpdc
CMDS/hostname
CMDS/idbgen
CMDS/ifstat
CMDS/inetd
CMDS/ipstat
CMDS/ispstart
CMDS/ispcfg
CMDS/ping
CMDS/mbinstall
CMDS/mount
CMDS/mountd
CMDS/netstat
CMDS/ndpd
CMDS/ndpdc
CMDS/ndpio
CMDS/nfsc
CMDS/nfsd
CMDS/nfsstat
CMDS/nppd
CMDS/nppdc
CMDS/portmap
CMDS/routed
CMDS/rpcdbgen
CMDS/telnet
CMDS/telnetd
CMDS/telnetdc
CMDS/undpd
CMDS/undpdc
CMDS/BOOTOBJS/ISP/SysMbuf
CMDS/BOOTOBJS/ISP/ifloop
CMDS/BOOTOBJS/ISP/ifman
CMDS/BOOTOBJS/ISP/inet
CMDS/BOOTOBJS/ISP/ip
CMDS/BOOTOBJS/ISP/lo0

CMDS/BOOTOBJS/ISP/netdb_resolv
CMDS/BOOTOBJS/ISP/netdb_small
CMDS/BOOTOBJS/ISP/nfs
CMDS/BOOTOBJS/ISP/nfs_devices
CMDS/BOOTOBJS/ISP/nfsnul
CMDS/BOOTOBJS/ISP/pk
CMDS/BOOTOBJS/ISP/pkdvr
CMDS/BOOTOBJS/ISP/pkman
CMDS/BOOTOBJS/ISP/pks
CMDS/BOOTOBJS/ISP/sockdvr
CMDS/BOOTOBJS/ISP/sockman
CMDS/BOOTOBJS/ISP/tcp
CMDS/BOOTOBJS/ISP/udp
CMDS/BOOTOBJS/ISP/af_ether
CMDS/BOOTOBJS/ISP/af_unix
USR/CMDS/remotedc
USR/CMDS/remoted
USR/HTTP/FairlightLogo.gif
USR/HTTP/UnderConstruction.gif
USR/HTTP/bullet2.gif
USR/HTTP/index.html
USR/HTTP/line.gif
USR/HTTP/riffmci.html
USR/HTTP/rule18.gif
USR/HTTP/sh.html
USR/HTTP/slurrytile.gif
USR/HTTP/AB/absrch.cgi
USR/HTTP/AB/absrch.html
ETC/Makefile
ETC/host.conf
ETC/hosts
ETC/hosts.equiv
ETC/inetdb
ETC/inetd.conf
ETC/networks
ETC/nfs.map
ETC/nfsd.map
ETC/protocols
ETC/readme.txt
ETC/resolv.conf
ETC/rpc
ETC/rpcdb
ETC/services
USR/WINNT/X86/anetd.exe
USR/WINNT/X86/dfnserver.exe
USR/WINNT/X86/dfn_cfg
USR/WINNT/X86/index.html
USR/WINNT/X86/doco.html
USR/LATTICE/download.html
USR/LATTICE/index.html
USR/LATTICE/wxcgpc7.zip

27.2 Upgrading 14.2 Software Revisions

27.2.1 From Exabyte Tape:

1. Connect Exabyte drive, set to ID 5.
2. Power up the Exabyte drive and insert software tape.
3. Power up (or restart) the MFX3^{plus}.
4. At Disk Recorder project page Type: **quit <return>**. You will be prompted "Close project and shutdown all applications" Type: **y <return>**.
5. At OS9 # prompt Type: **chd /dd <return>**.
6. At OS9 # prompt Type: **upgrade -t <return>**. Choose device number from far-left column, (##) e.g. **1 <return>** (example only!)
7. You will be asked if you want to format the drive

   Answer "no" (**n <return>**) if there are projects on the drive that need to be saved. If in doubt, answer "no".
8. When the upgrade is complete, the system will restart, and load the new console software.
9. From the Project menu screen type: **quit<return>** You will be prompted " Close project and shutdown all applications" Type: **y <return>**.
10. At OS9 # prompt Type: **chd /dd/usr/roms <return>**.

    Type: **blowall <return>** Three x "GOOD" should be displayed after process is complete
11. Type: **chd /dd <return>**, (Return to root directory).
12. To save this software in a 'release file' on the boot disk. Type: **xrelease <return>**.
13. Reboot the system by typing: **restart <return>**.
14. You will be prompted "are you sure you want to reboot the system?" Type: **y <return>**.
15. During reboot process the boot cycle may stop @ Prompt "OS-9/68KV3.0 Waveform Executive '/Term' online 98/03/25 at 15:35:49" Press **<return>.**
16. At OS9 "USER NAME ?" prompt type: **mfx <return>**.
17. At OS9 "MFX" prompt type: **bemfx** (For MFX^{plus}) or **befame** (For Fame) **<return>**.
18. At OS9 "MFX" prompt type: **mfx3 <return>**.
19. Upon reboot you may be prompted "NVRAM version has changed reconfiguration is forced. Do you want to use recommended NVRAM configuration?

    Type: **y <return>**.

27.2.2 From Hard Disk Drive:

1. Connect drive with software release file, set to ID to one of the following addresses that is not used by any other device on the SCSI chain 1,2,3,4 or 6.

2. Power up all drives.

3. Power up the MFX3plus.

10. At Disk Recorder project page Type: **quit** <**return**>. You will be prompted "Close project and shutdown all applications" Type **y** <**return**>.

11. At OS9 # prompt Type: **chd /scx0** <**return**> Where "x" = SCSI ID set in step 1.

12. At OS9 # prompt Type: **upgrade** <**return**>. Choose release file to upgrade to and the device number from far-left column, (##) e.g. **1** <**return**> (example only!)

13. You will be asked if you want to format the drive

    Answer "no" (**n** <**return**>) if there are projects on the drive that need to be saved. If in doubt, answer "no".

14. When the upgrade is complete, the system will restart, and load the new console software.

15. From the Project menu screen type: **quit** <**return**> You will be prompted " Close project and shutdown all applications" Type **y** <return>.

10. At OS9 # prompt Type: **chd /dd/usr/roms** <**return**>.

    Type: **BLOWALL** <return>Three x "GOOD" should be displayed after process is complete

11. Type: **chd /dd** <**return**>, (Return to root directory).

20. To save this software in a 'release file' on the boot disk. Type: **xrelease** <**return**>.

21. Reboot the system by typing **restart** <**return**>.

22. You will be prompted "are you sure you want to reboot the system?" Type: **y** <**return**>.

23. During reboot process the boot cycle may stop @ Prompt "OS-9/68KV3.0 Waveform Executive '/Term' online 98/03/25 at 15:35:49" Press: **<return>.**

24. At OS9 "USER NAME ?" prompt type: **mfx** <**return**>.

25. At OS9 "MFX" prompt type: **bemfx** (For MFXPlus) or **befame** (For Fame) <**return**>.

26. At OS9 "MFX" prompt type: **mfx3** <**return**>.

27. Upon reboot you may be prompted "NVRAM version has changed reconfiguration is forced. Do you want to use recommended NVRAM configuration?

    Type **y** <**return**>.

27.3 Upgrading 15.1 Software Revisions

Upgrading software in 15.1 is more complicated than our previous releases. These steps apply for both TurboSCSI and PCI Systems. This information should assist you:

IMPORTANT TIPS:

If you are upgrading from 14.2 to 15.1, a new file called **/nvr/setup** must be created. Please follow steps 1-22

For succeeding installations of Rev 15.1 please follow Steps 1-3 and 6-22.

MFX3+ 15.1 *(and above)* Software Installation

1. While running MFX3, type **quit**<RETURN> to exit the program.

2. Type **belogin**<RETURN> from OS9 prompt

3. Restart MFX3

4. The bootup will stop at a login screen. Type <RETURN>, then **mfx**<RETURN>.

5. Create file **/nvr/setup** using text editor, by typing **ed /nvr/setup**<RETURN>

   This file should contain the following lines, which you can type verbatim, pressing <RETURN> to move to the next line (the spaces do not matter, they are printed here for convenience):

   [Config]

   Web = on

   [Web]

   HOSTNAME = ***hostname***

   IP_ADDRESS = ***AAA.BBB.CCC.DDD***

   DOMAINNAME = ***domainname***

   WHERE: **hostname** is your unique name for this machine (host) on this network (E.g.: **jims_editor**)

   AAA.BBB.CCC.DD are three numbers, each between 0 and 255 that make up the IP address of this host on this network (see item 6 for correct IP address)

   (E.g. **191.100.133.14**)

   domainname is the domain name where this MFX3 belongs (E.g. **studio2**). This can be anything you like.

6. Note that no two machines on the same network can have same HOSTNAME or IP_ADDRESS but they can all have the same DOMAINNAME. Numbers AAA.BBB.CCC must be the same as the first three numbers of your NT server IP address (if you have one). AAA should be 192. BBB and CCC can be anything you like except 255. DDD

must be unique for each machine on the network.

7. **Install release** 15.1.X using file 15_1_XX.gz

8. Disconnect the machine from the 100 Base Hub (if used).

9. Restart MFX3

10. Login as **mfx** as in step 4.

11. Remove the modules **inetdb** and **rpcdb** from memory by repeatedly typing **"unlink inetdb**<RETURN>**"** and **"unlink rpcdb**<RETURN>**"** as long as they exist. Once they are completely removed from memory a message like this will appear:

    unlink: can't unlink "inetdb". 000:221 Module Not Found

    for "inetdb" and a message like this

    unlink: can't unlink "rpcdb". 000:221 Module Not Found

    for "rpcdb"

12. Edit file by typing **ED /dd/ETC/hosts**<RETURN>

13. Find the line that reads

127.0.0.1 localhost

14. Add a line after it that reads:

    AAA.BBB.CCC.DDD hostname

    Where ***hostname*** and ***AAA.BBB.CCC.DDD*** correspond to the name and numbers assigned in step 2

15. Save the file **/dd/ETC/hosts (Blue Z saves the file.)**

16. Type **chd /dd/ETC**<RETURN>

17. Type **idbgen**<RETURN>

18. Type **rpcdbgen *hostname* -c -d -s -r=/dd/ETC <return>**

19. Blow all ROMs as follows

    Type **chd /dd/usr/roms**<RETURN>

    Type **blowall**<RETURN>

20. Connect the network cable (if used) and reboot MFX

21. If the file server is running check that it appears on the file page with its domain name and hostname.

28.0 Disk Drives

28.1 FILE FORMATS

The MFX3plus supports the following disk file formats :

28.1.1 RBF

RBF (Random Block File) is OS-9's native disk file system. RBF supports drives up to approx. 4 GBytes capacity, with a maximum file size of 4 GBytes. This format is used in Fairlight systems from Rev 14 upwards.

**Note: Boot drives must be 'RBF'.

To initialise a disk drive with the 'RBF' file format :

1) Connect the drive to the SCSI chain of an MFX3plus. Make sure the SCSI I.D. is not shared by any other devices.

2) Quit to the shell... Type: **quit** <return> **y**. Type: **df** <return> . Check the drive to be initialised is present. Check SCSI I.D.

3) Type: **diskinit /scX0 -c=128 -v=1024 -z -n=diskname** <return>

   **Note: 'X' = SCSI I.D. of the drive to be initialised.

   '-n=diskname' is optional. If this option is not included, the volume name (in the Project Menu device box) will default to 'MFX3'.

4) Type: **restart** <return> **y** <return> .

5) If the diskinit command fails, replace the '-z' option with a '-r' and try the command again. Always restart after a diskinit command.

If a drive larger than 4 gig is initialised as RBF, any disk space outside the 4 gig barrier is not useable. i.e. disk size is limited to 4 gig.

Diskinit does not do a low level format on the disk. Most, if not all drives manufactured today, have the ability to automatically relocate bad sectors on the fly so these bad sectors no longer have to be 'mapped out' at format time. Even P.C.'s when 'formatting' a drive do not actually do a format, all blocks are written to and then read back. Any bad blocks are detected in this way and mapped out of the file system at that time.

28.1.2 FLFS

FLFS (Fairlight File System) was created by Fairlight to handle devices larger than 4 GBytes. FLFS supports drives of up to 200 GBytes, with a maximum individual file size of 4 GBytes. This format is used in Fairlight systems from Rev 14.2 upwards. (Note: Boot drives cannot be FLFS)

To initialise a disk drive with the FLFS file format :

1) Connect the drive to the SCSI chain of an MFX3plus. Make sure the SCSI I.D. is not shared by any other devices.

2) Quit to the shell... Type: **quit** <return> **y** .

   Type: **df** <return> . Check the drive to be initialised is present. Check SCSI I.D.

3) Type: **diskinit /scX0 -w -n=diskname** <return>

   **Note: 'X' = SCSI I.D. of the drive to be initialised.

   '-n=diskname' is optional. If this option is not included, the volume name (in the Project Menu device box) will default to 'No Volume'.

4) Type: **restart** <return> **y** <return> .

Individual file (project) size is limited to 4 gig.

Diskinit does not do a low level format on the disk. Most, if not all drives manufactured today, have the ability to automatically relocate bad sectors on the fly so these bad sectors no longer have to be 'mapped out' at format time. Even P.C.'s when 'formatting' a drive do not actually do a format, all blocks are written to and then read back. Any bad blocks detected in this way and mapped out of the file system at that time.

28.1.3 MDR-DOS

MDR-DOS (Multitrack Disk Recorder Disk Operating System) was invented by Fairlight to handle large disk recorder files with very low fragmentation. It supports drives up to approx 4 GBytes, with a maximum file size of 4 GBytes. MDR-DOS was the MFX native file system from Revision 9 software to Rev 12. This format is still supported in the latest software, and can be used to transport files from Rev11 & 12 into Rev 14.

Disk drive initialisation can only be performed on an MFX2, or an MFX3 (Rev12 only).

To initialise a disk drive with the 'MDRDOS' file format :

1) Connect the drive to the SCSI chain of an MFX2 (Rev11) or MFX3 (Rev12 only). Make sure the SCSI I.D. is not shared by any other devices.

2) Quit to the shell...

   Type: **quit** <return> **y**.

   Type: **inq** <return> . Check the drive to be initialised is present.

3) Type: **scsiformat /scX0 -m** <return> (where X=SCSI I.D. of drive to be initialised).

This takes approx 10 minutes per gig, though some drives are much quicker.

4) Type: **mdrinit /scX0** <return> . Answer **y** <return> when asked to continue.

5) Type: **boot** <return> .

28.1.4 HFS

HFS (Hierarchical File System) is the Macintosh file system. Fairlight MFX systems can read this file system, and it is used to transport OMF files from Macintosh based systems such as Avid Media Composer and Digidesign ProTools.

Disk drive initialisation to be performed on the host machine (eg. Avid).

Initialization of HFS drive for OMF with FWB Hard Disk Toolkit 2.06 or above.

1. Launch the application with the drive connected on the Macintosh SCSI chain.

2. Select the drive to be initialized from the browser window.

3. Select the **Auto Initialize icon** from the browser window (last con to the right) or select Auto Initialize from the Devices menu.

4. You will be prompted with the Auto Initialize window.

Choose "**Quick**" as a format type (default)

Click "**OK**"

5. A warning message box will pop up

Click "**OK**"

6. You will be prompted one more time with the same warning window.

Click "**OK**" again.

When the initialization process is done a Message box will display a successful result message.

The drive is now ready for OMF.

28.1.5 FAT-16

FAT-16 (File Allocation Table) supports partitions of up to 2 GBytes, with a maximum file size of 2 GBytes. Fairlight MFX can read and write this disk file system, and it is used to transport WAVE files and other file types between MFX and products based on the PC.

Disk drive initialisation to be performed on the host machine (eg. PC).

To initialize a disk drive for 'FAT16 file format', connect the disk drive to a P.C. running either... 1) Windows 95/98 OR 2) Windows NT O.S.

28.1.5.1 From Windows 95/98

Boot to MS-DOS prompt. (Press F8 key when message... 'Booting' appears, then select the right startup mode).

1. Type the following command from the command line:

   C:\> fdisk <**return**>

   The following screen will appear :

   ```
   Microsoft   Windows   98

   Fixed   Disk   Setup   Program

   ©Copyright   Microsoft   Corp.   1983   -   1998

   FDISK    Options

   Current   fixed   disk   drive:   1
   ```

   Choose one of the following:
   1. Create DOS partition or Logical DOS Drive
   2. Set active partition
   3.Delete partition or Logical DOS Drive
   4.Display partition information

   Enter choice: [1]

   Press Esc to exit FDISK
   Select "Create DOS partition or Logical DOS Drive"

2. Create a new partition on the new disk. Note that in order to ensure the disk is FAT16 compliant, the partition must not exceed 2 Gb in size (In case of 4Gb disk, typically two partitions should be created). Newer versions of MS-DOS (Windows 95/98) might offer an option to create partitions larger than 2Gb, but they will not be compatible with MFX3plus software.

3. After the partition(s) have been created, exit fdisk and reboot the P.C. to MS-DOS prompt, as described earlier.

4. Typically, newly formatted partitions will have a 'drive letter' assigned to them in a sequence that follows the disks that are already in system. Eg. If we already have C: and D:, and we create two partitions on a new disk (as described above), they will appear as E: and F: .

5. Format the disks to FAT16 using MS-DOS format utility by executing the following command:

   C:\> **format X:** <return> Where 'X' is the 'drive letter' of the partition created earlier by fdisk.

6. Repeat the above command for any other newly created partitions.

7. Reboot the P.C. and verify that Windows 95/98 can mount the newly created partition(s). They should appear in 'My Computer' applet as new disks, Eg. E:\ and F:\ for the above example.

8. Shutdown PC, remove the disk drive and connect it to an MFX3plus.

9. Restart the MFX3plus and verify that the new partition(s) appear in the device list. Eg. With a FAT16 disk at SCSI I.D. 3, a new partition named C300 will appear.

28.1.5.1 From Windows NT Server/Workstation :

1. Connect the disk drive to the P.C.

2. Select **Start/Programs/Administrative Tools/Disk Administrator** applet... run it.

3. The newly added disk will appear as shaded area.

4. Partition the disk into 2 Gb partition(s) using menus provided.

5. Select **Commit Changes Now**.

6. Right click onto one of the newly created partition images and select **Format.**

7. Select **MS-DOS format** and click OK.

8. Repeat the procedure for any other newly created partitions.

9. Exit Disk Administrator.

10. Verify that Windows 95 has mounted newly created partition(s). They should appear in 'My Computer' applet as new disks.

11. Shutdown Windows NT machine, remove the disk and connect it to an MFX3plus .

12. Restart the MFX3plus and verify that the new partition(s) appear in the device list. Eg. With a FAT16 disk at SCSI I.D. 3, a new partition named C300 will appear.

29.0 MediaLink

29.1 Media Link Software – Description

Medialink Windows NT software provides the fast link between network interfaces and various applications that are necessary for operation of MediaLink network.

Network protocols used for MediaLink connections are UDP/IP used for ANETD connections and TCP/IP used for DFNSERVER connections.

Module ANETD.EXE serves client calls from MFX3+ machines and other Windows NT server providing fast network data transfer.

Module DFNSERVER.EXE serves client calls from MFX3+ machines and other Windows NT server machines providing browsing capabilities, actual data transfers during backup, copy, move, etc.

The following table lists the components that run on Windows NT server machine.

No	Module	Description	Source/Avail
1	ANETD.EXE	Windows NT multithreaded server application that handles ANET protocol requests.	FAIRLIGHT ESP Pty Ltd
2	DFNSERVER.EXE	Windows NT multithreaded server application that handles DFNSERVER client request	FAIRLIGHT ESP Pty Ltd
3	DISKPERF.SYS	Windows NT device driver that replaces standard one supplied by Microsoft	FAIRLIGHT ESP Pty Ltd

29.2 Media Link Software - Fairlight NT Applications

MediaLink Server software runs on Windows NT x86 based server and modules are being supplied with every MFX3+ release package.

Internal Revision number will change with major change of modules ANETD.EXE and DFNSERVER.EXE, while MFX3+ release number for each will change from release to release. They can be verified by executing the following procedures:

1. Open Windows NT Console

2. Changed directory to directory where FAIRLIGHT modules are (**C:\FAIRLIGHT**)

3. Check the ANETD.EXE internal and MFX3+ revisions

4. Type the following line and observe the output

```
> ANETD.EXE -?
ANETD server Ver 1.3   <- ANETD Internal Revision Number
MFX Version: 15.1.05j  <- MFX3+ Software Revision
usage: anetd -<options>
      -z      - print additional debug info
      -d      - turn on debug mode (no physical RD/WR of audio data to/from disks)
```

5. Check the DFNSERVER.EXE internal and MFX3+ revision numbers

6. Type the following line and observe the output

```
>dfnserver   -?
DFN  server  Ver  1.8
MFX  Version:  15.1.05j
usage:   dfnserver   -<options>
       -m=<num>   minimum  malloc  size(default  1024)
      -v           Prints MFX3 version number and exits
      -z          enable debug output
```

Module DISKPERF.SYS currently doesn't have a revision number and it cannot be verified

It is essential that all the machines on a same network should run ANETD.EXE and DFNSERVER.EXE modules that were extracted from the same FAIRLIGHT MFX3+ distribution that runs on client MFX3+ machines.

30.0 APPENDICES

30.1 MFX3 LEVEL MODIFICATION

MFX3 is shipped with a nominal level of +4dBu and +18dB headroom (i.e. +22dBu peak). This comforms to the Australian and American digital audio standards (although these standards are only a guideline).

To modify the level settings, the ***nominal level in dBu*** and ***headroom in dB*** must be known. The peak level is defined as the sum of the nominal level and headroom in dB and is set via resistors on the ESP-AIO audio card. The headroom is set on the level meters via the *red* command.

There are two sets of resistor values to be changed to specify the peak level:

R_{IN} = input gain resistors R37,R38,R41,R42,R45,R46,R49,R50

R_{OUT} = output attenuation resistors **R14,R16,R18,R20**

To set the level meter headroom, type the command:

red <headroom in dB>

30.1.1 STANDARD SETTINGS

Standard	Nominal	Peak	Headroom	R^{IN}	R^{OUT}
tape	+4dBu	+24dBu	20dB	3K	5K1
America Australia Japan (broadcast)	+4dBu	+22dBu	18dB	3K6	6K2
Austria (broadcast)	+6dBu	+18dBu	12dB	5K6	10K
Germany (broadcast)	+6dBu	+15dBu	9dB	8K2	14K3

NOTES:

1. All resistors are 0.1% tolerance ³0.125W.

2. If resistors are not available, select lower R_{IN} and/or higher R_{OUT}.

MFX3 provides electronic 'transformer' outputs. If the cold is connected to GND (i.e. run as single ended unbalanced), the hot will gain by 6dB maintaining the equivalent balanced level. *Note that the maximum achievable level for single ended unbalanced is +20dBu*

30.1.2 SETTINGS FOR OTHER STANDARDS

Assumes the *nominal level* and *headroom* are known.

1. *Determine the peak dB level*

   $PEAK_{dB}$ (dBu) = nominal(dBu) + headroom (dB) + 0.5dB

   Usually the peak level is over estimated to ensure the requested headroom. 0.5dB has been added in the above to account for variations in ADC and DAC peak levels (±0.4dB).

2. *Determine peak level as peak-to-peak voltage*

   $PEAK_{dB}$/20

   $PEAK_{VPP}$ (V) = 1.096 x 10

   (0dBu = 0.775V_{RMS} which is equivalent to 1.096V peak amplitude)

3. *Determine required input and output gain*

   $GAIN_{IN}$ = 7.36 / $PEAK_{VPP}$

   $GAIN_{OUT}$ = $PEAK_{VPP}$ / 4.00

   (7.36V and 4.00V are the nominal ADC and DAC peak levels respectively)

4. *Determine R_{IN} and R_{OUT}*

   R_{IN} = 15000 x $GAIN_{IN}$ / 2

   R_{OUT} = 22000 / $GAIN_{OUT}$

   The value for R_{IN} should be *reduced* to the nearest 0.1% resistor value. The value for R_{OUT} should be *increased* to the nearest 0.1% resistor value. This guarantees the required headroom. 0.125W or higher resistors can be used.

   (15000 and 22000 are the fixed gain setting resistors for the input and output respectively, the factor of 2 for R_{IN} accounts for the differential input)

5. *Set headroom setting in MDR*

   Type: **red <headroom in dB>**

   e.g. to set for 18dB headroom type: red 18

30.2 Error Codes

255:255 Operation Failed
082:001 No Project File
082:002 Feature Not Available in this Release
082:003 File Already Exists - Delete Existing File First
082:004 Cant Get Free Space From Current Device
082:005 Space List Full
082:006 Bad File Descriptor
082:007 MFX File Already Exists
082:008 Bad Channel Number
082:009 Track Is Not Stereo
082:010 Space List Overflow
082:012 Invalid Playtask Request
082:013 The MFX System is Not Running
082:014 Invalid Command
082:015 Bad SMPTE Time
082:016 Non-Existent External File
082:017 No Waveform
082:018 Non-Existent Waveform
082:019 Bad Waveform No.
082:020 Device Table Full
082:021 External File Table Full
082:022 Invalid Library File No.
082:023 Bad Cluster Size
082:024 Space Allocation Table Overflow
082:025 Waveform Table Full
082:026 Bad Space-List Length
082:027 Project File is Maximum Size
082:028 End Of Space
082:029 Waveform Already Referenced
082:030 End Of Waveform
082:031 Error In Space Allocation Table
082:032 Undefined Device
082:033 Invalid Dfn File Number
082:034 Edit List Full
082:035 Invalid File Version No. - Cannot Load
082:036 Bad Call
082:037 Insufficient Waveform Ram
082:038 No Range
082:039 Iram Mgt Error
082:041 Digital Io Module Error
082:044 Must Not Be An Mdr Device
082:045 File is Not an MFX Project
082:046 Invalid Device Number

082:047 DCC Not Responding
082:048 Max Clip Duration Exceeded (2047 Megabytes)
082:049 No Selected Clip At Current Position
082:050 Bad File Type
082:051 Eq System Error
082:052 MFX Console has Wrong Software Revision
082:053 Can't Attach The Current Project
082:054 Track-Lock Protocol Error
082:055 No Clip To Keep
082:056 Cannot Edit Library File
082:057 No Library File Open
082:058 Next Clip Too Far Away - Cannot Overwrite
082:059 Already Recording
082:060 No Marks Left
082:061 No Clip On Selected Track(s)
082:062 No Track Is Armed For Recording
082:063 Can't Do That While Recording...
082:064 Can't Dilate - Out Of Range
082:065 Bad Track Number
082:066 External File Not Open
082:067 Inaccessible Waveform
082:068 Clip Has Waveform External To Library File
082:069 Write Attempted To External File
082:070 Non-Existent External Waveform
082:071 External Waveform Not Okay
082:072 External Waveform Different
082:073 Can't Attach Old Version Library File - Open As Project First
082:074 Waveform Segment List Full
082:075 Cannot Change Project Sample Rate
082:076 Clip Is Not Stereo
082:077 Clip Is Not Mono
082:078 Can't Import - Different Sample Rate
082:079 Big Buffer Too Small
082:080 No Clips Are Grabbed
082:081 Range Not Allowed
082:082 Clipboard Is Empty
082:083 Zero-Width Range
082:084 Arming Status Error
082:085 No Clip In Range
082:086 No Clip At Current Position
082:087 Current Position Is At Head Of Clip
082:088 Current Position Is At Tail Of Clip
082:089 No Clip Entirely Within Range
082:090 Edit List Relocation Error
082:091 Edit List Corrupted
082:092 Edit List In Infinite Loop

082:093 Too Many GFX Modules
082:094 Invalid GFX Module
082:095 Waveform Not Available
082:096 File Layout Violation
082:097 Invalid Space List
082:098 Not Enough Disk Space
082:099 Range Edge Is At Head Of Clip
082:100 Range Edge Is At Tail Of Clip
082:101 No Clip At Range ‘From’ Point
082:102 No Clip At Range ‘To’ Point
082:103 Cannot Open - Bad File Header Or Size
082:104 Not Enough Channels
082:105 Not Enough Tracks
082:106 Coverage Sequence Overflow
082:107 Permission Denied
082:108 Protected by Password - Cannot Open
082:109 Protected by Password - Cannot Rename
082:110 Protected by Password - Cannot Delete
082:111 OMDL Format Error
082:112 Clip Not Found
082:113 All Selected Tracks are SAFE
082:114 Track is SAFE
082:115 File is OPEN - please CLOSE before delete
082:116 Patch Menu Disabled In Escape ‘s’ Page
082:117 Can’t Do That While Auditioning...
082:118 Clip Has Different Sample Width
082:119 Clip is not 16-bit - operation not supported
082:120 Application Error
082:121 No Master Clock
082:122 Can’t Load Console Software
082:123 Heap Empty
082:124 Audio Format Not Supported
082:125 Filetype Not Licensed
082:126 Illegal Filetype For Operation
082:127 Waveforms Incompatible as Stereo Pair
082:128 Cannot Open This Filetype
082:220 Write Attempted To A Read Only Device
082:221 Project is Open for Read Only
082:222 Too Many Files Have Been Marked - Maximum 254
082:223 No Mdr Device On Line
082:224 No Device On Line
082:225 Sony - Communications Error
082:226 Sony - Machine Is In Local Mode
082:227 Sony - No Tape In Machine
082:228 Sony Machine Control Software Not Installed
082:230 No audio found in file

082:240 Incorrect Machine Type
000:001 Operation Terminated
000:002 Keyboard Quit
000:003 Keyboard Interrupt
000:032 Abort
000:033 Erroneous Math Operation
000:034 Illegal Function Image
000:035 Segment Violation (Bus Error)
000:036 Termination Request
000:037 Alarm Time Elapsed
000:038 Write To Pipe With No Readers
000:039 User Signal #1
000:040 User Signal #2
000:041 Address Error
000:042 Chk Instruction
000:043 Trapv Instruction
000:044 Privilege Violation
000:045 Trace Exception
000:046 Line-A Exception
000:047 Line-F Exception
000:064 Illegal Function Code (Math)
000:065 Ascii->Numeric Format Conversion Error (Math)
000:066 Not A Number (Math)
000:067 Illegal Argument
000:102 Bus Trap
000:103 Address Trap
000:104 Illegal Instruction
000:105 Integer Divide By Zero
000:106 “Chk” Or “Chk2” Instruction Trap
000:107 “Trapv”, “Trapcc” Or “Ftrapcc” Instruction Trap
000:108 Privileged Instruction
000:109 Trace Exception
000:110 Illegal Instruction (1010)
000:111 Illegal Instruction (1111)
000:112 Exception 12
000:113 Coprocessor Protocol Violation
000:114 System Stack Frame Format Error
000:115 Uninitialized Interrupt
000:116 Exception 16
000:117 Exception 17
000:118 Exception 18
000:119 Exception 19
000:120 Exception 20
000:121 Exception 21
000:122 Exception 22
000:123 Exception 23

000:124 Spurious Interrupt
000:133 An Uninitialized User Trap (1-15) Was Executed
000:148 Floating Point Unordered Condition
000:149 Floating Point Inexact Result
000:150 Floating Point Divide By Zero
000:151 Floating Point Underflow
000:152 Floating Point Operand Error
000:153 Floating Point Overflow
000:154 Floating Point Not A Number
000:155 Floating Point Unimplemented Data Type
000:156 Pmmu Configuration
000:157 Pmmu Illegal Operation
000:158 Pmmu Access Level Violation
000:159 Exception 59
000:160 Exception 60
000:161 Exception 61
000:162 Exception 62
000:163 Exception 63
000:164 No Permission
000:165 Arguments To F$Chknam Didn'T Match
000:166 System Stack Overflow
000:167 Invalid Event Id Number
000:168 Event Not Found
000:169 The Event Is Busy
000:170 Impossible Event Parameters
000:171 System Data Structures Have Been Damaged
000:172 Module Revision Is Incompatible With Operating System
000:173 Path Became Lost Because Network Node Was Down
000:174 Bad Disk Partition, Or No Active Partition
000:175 Hardware Is Damaged
000:176 Invalid Sector Size
000:177 Unexpected Or Bad Signal
000:200 The Path Table Is Full
000:201 Bad Path Number
000:202 System Irq Table Is Full
000:203 Bad I/O Mode
000:204 System Device Table Is Full
000:205 Bad Module Header
000:206 System Module Directory Is Full
000:207 Memory Full
000:208 Unknown Service Code
000:209 Non-Sharable Module Is Busy
000:210 Bad Page Address
000:211 End Of File
000:212 Irq Vector Is Busy
000:213 Non-Existing Segment

000:214 File Not Accessible
000:215 Bad Pathlist
000:216 File Not Found
000:217 File Segment List Is Full
000:218 Creating An Existing File
000:219 Illegal Memory Block Address
000:220 Modem Data Carrier Lost
000:221 Module Not Found
000:222 System Clock Not Running
000:223 Deleting Stack Memory
000:224 Illegal Process Id
000:225 Bad Irq Parameter
000:226 No Children
000:227 Invalid Trap Number
000:228 Process Has Aborted
000:229 System Process Table Is Full
000:230 Illegal Fork Parameter
000:231 Known Module
000:232 Bad Module Crc
000:233 Signal Error
000:234 Non Executable Module
000:235 Bad Name
000:236 Bad Module Header Parity
000:237 No Ram Available
000:238 Directory Is Not Empty
000:239 No Available Task Number
000:240 Illegal Unit (Drive) Number
000:241 Bad Sector Number
000:242 Media Is Write Protected
000:243 I/O Error - Bad Check Sum
000:244 Read Error
000:245 Write Error
000:246 Device Not Ready
000:247 Seek Error
000:248 Media Full
000:249 Incompatible Media
000:250 Device Busy
000:251 Disk Media Has Changed
000:252 Record Is Busy
000:253 Non-Sharable File/Device Is Busy
000:254 I/O Deadlock Error
000:255 Device Is Format Protected
001:000 Ansi C Number Out Of Range
006:000 Illegal Parameter
006:001 Identifier (Id) Table Full
006:002 Bad Size Error

006:003 Region Definition Full (Overflow)
006:004 Unallocated Identifer Number
006:005 Null Region
006:006 Bad Drawmap/Pattern Mode
006:007 No Active Font
006:008 No Drawmap
006:009 No Audio Play In Progress
006:010 Audio Record/Play Has Been Aborted
006:011 Audio Queue Is Full
006:012 Audio Processor Is Busy
006:100 No Free Slot Is Left In The Resource Table
006:101 The Specified Resource Module Id Is Not A Valid Slot
006:102 The Resource Is Not Sharable
006:103 The Type Of The Resource Is Bad
006:104 The Id Of A Resource Is Bad
006:110 There Are No Items Specified For The Request
006:111 The Item Number Is Out Of Range
006:112 The Number Of Columns Is Out Of Range
006:113 The Item Array Pointer Is Bad
006:114 Request Could Not Be Created
006:115 A Modal Request Has Timed Out
006:116 No Selection Was Made For A Modal Request
006:117 Bad Definition Function Id
006:118 Bad Definition Action Code
006:119 Bad Item State Value
006:120 The Request Rectangle Is Bad
006:130 Bad Standard Behaviour Id
006:131 Bad Standard Definition Id
006:132 Bad Action For Definition Function
006:133 Bad Action For Behaviour Function
006:134 Bad Control State
006:135 Bad Control Part Code
006:136 Bad Flags
006:137 Bad Min, Max Or Value
006:138 Bad Type Of Control
006:140 Cannot Find The Clipboard Device In Preferences
006:141 The Clipboard Is Full
006:142 Type Not Represented In Clipboard
006:143 Clipboard Not Opened For The Requested Access
006:144 Type Offset Is Greater Than The Type Count
006:145 Clipboard Is Not Currently Opened
006:146 Clipboard Is Not Initialised
006:147 Clipboard Is Not Currently Closed
006:148 can't Rewrite, The Type Is Not In The Clipboard
006:150 The Handler Is Unknown
006:155 No Entry Found

006:160 Line Table Overflow
006:161 Text Too Long (Maximum Is 65535)
006:162 Bad Type Or Type Not Implemented
006:163 Attempt To Draw A Line Too Long
006:164 Need A Line Table
006:165 Font Not Set In The Drawmap
006:166 Bad Rectangle
006:180 Global Variable Error
006:185 No Preference Module
006:186 Illegal Argument
006:190 Bad Rectangle For Overlay
006:191 The Overlay Is Not The Top Of The Stack
006:192 Unknown Overlay
006:200 Bad Definition Id
006:201 Bad Definition Action
006:202 Bad Min, Max Or Value
006:203 Bad Coordinates
006:204 Indicator Not Created
006:205 Bad Flags
006:206 Bad Pointer
007:001 (Esp) I/O Operation Would Block. (Iff) This Path Is Read-Only.
007:002 (Esp) I/O Operation Now In Progress. (Iff) This Path Is Write-Only.
007:003 (Esp) Operation Already In Progress. (Iff) There Is No Form Active.
007:004 (Esp) Destination Address Required. (Iff) Wrong Reader For This Type Of Form.
007:005 (Esp) Message Too Long. (Iff) Not An Iff File.
007:006 (Esp) Protocol Wrong Type For Socket. (Iff) Bad Parameters.
007:007 (Esp) Bad Protocol Option. (Iff) Bad Cat Id (For Iff_Open).
007:008 (Esp) Protocol Not Supported. (Iff) Can Not Skip, Size Is Unknown.
007:009 (Esp) Socket Type Not Supported. (Iff) Not To The Data Yet.
007:010 (Esp) Operation Not Supported On Socket. (Iff) Attempt To Seek Back In A Pipe.
007:011 (Esp) Protocol Family Not Supported. (Iff) Fixed Size Chunk Was Not The Correct Size. Could Indicate Wrong Version Of Reader.
007:012 (Esp) Address Family Not Supported By Protocol. (Iff) Can Not Make Floating Point Conversion.
007:013 Address Already In Use
007:014 can't Assign Requested Address
007:015 Network Is Down
007:016 Network Is Unreachable
007:017 Network Dropped Connection On Reset
007:018 Software Caused Connection Abort
007:019 Connection Reset By Peer
007:020 No Buffer Space Available
007:021 Socket Is Already Connected
007:022 Socket Is Not Connected
007:023 can't Send After Socket Shutdown

007:024 Too Many References
007:025 Connection Timed Out
007:026 Connection Refused By Target
007:027 Mbuf Too Small For Mbuf Operation
007:028 Socket Module Already Attached
007:029 Path Is Not A Socket
008:001 Line Down Or Layer 1 Error On Attach.
008:002 Connection Error - Connection Not Made.
008:003 Receive Thread Incoming Packet Handler Error.
008:004 Management Entity Error.
008:005 Unrecognised Service Access Point (Sapi).
008:006 Terminal Endpoint Identifier (Tei) Error.
008:007 Maximum Number Terminal Endpoints In Use.
008:008 Illegal Layer 2 State.
008:009 Terminal Endpoint (Tei) Initialisation Denied.
008:010 Unrecognised Primitive.
008:011 Layer 2 Error On Incoming Message.
008:012 Peer Receiver (Far End) Busy Condition.
008:013 Maximum Number Of Outstanding Messages Exceeded.
008:014 Maximum Number Of Call References In Use.
008:015 Call Reference doesn't Exist.
008:016 Call Progress State Error.
008:017 Receiver Assignment/Removal Error.
150:000 Illegal Device Number
150:001 Bad Command
150:002 Busy
150:003 Media Offline or Non-Existent
150:004 Device Locked
150:005 Can't Locate File to Mark
150:006 Can't Locate File to Unmark
150:007 Device Name Too Long
150:008 No Spare Units
150:009 Invalid Node
150:010 More Than One Destination For Backup
150:011 Two Tape Devices Not Supported
150:012 Limit of 255 Marked Files
150:013 Abort Backup/Restore
150:014 Restoring On-Top Of Itself
150:015 Can't Restore To Tape
150:016 Can't Mark Library File
150:017 File Already Exists At Destination
150:018 Device is in use
150:019 Tape is not in MFX format
150:020 Waiting for to tape to Load - Ctrl 'q' to exit
150:021 Fixed Device
150:022 Bad Device Name

150:023 Can't Perform Operation
150:024 Invalid File ID
150:025 DFN Internal Problem
150:026 Not A Directory
150:027 No Permission
150:028 File Table Full
150:029 File Hasn't Been Locked
150:030 Not Cached
150:031 File in Use - Cannot Open
150:032 File Already Marked
150:033 Backup/Restore/Copy Already In Progress
150:034 Arch Unit No Longer Valid
150:035 No Backup In Progress
150:036 Unit Being Used For Archive
150:037 Error Occurred While Caching Device
150:038 Can't Read From Tape - Old Version
150:039 Device Is Read-Only
160:000 FFS FOLDER LIMIT REACHED
160:001 NODE NO LONGER VALID
160:002 DESTINATION OF MARKED FILE IS LOCKED BY ANOTHER USER
160:003 DESTINATION REQUIRED
160:004 FILE WITH SAME NAME ALREADY MARKED TO DESTINATION
160:005 CAN'T COPY TO TAPE DEVICE
160:006 MESSAGE RECEIVED DURING COPY/MOVE
160:007 NO FILE SELECTED
160:008 INVALID BACKUP HANDLE
160:009 NO UNIT SELECTED
160:010 NO JOB ACTIVE
160:011 PATHNAME TOO LONG
160:012 NETWORK CONNECTION ERROR
160:013 NETWORK HOST NOT ONLINE
065:001 ABase - Field Not Defined
065:002 ABase - Incompatible Version
065:003 ABase - DataBase Not Found
065:004 ABase - DataBase Is Empty
065:005 Publish - No Project Reference
065:006 Publish - Not a Project File
065:007 Publish - Files Don't Match
065:008 ABase - UI Mode Conflict
065:009 ABase - UI Error
065:010 ABase - Invalid Field Value
111:010 DCC Xilinx INIT Error
111:011 DCC Xilinx DONE Error
111:020 DCC BTDO low
111:021 DCC BTDO high
111:022 DCC BTDI low

111:023 DCC BTDI high
111:030 DCC Program Init Failed - Timeout
111:040 DCC Debug Request Timeout
111:050 DCC-MDR - Unknown Request Code
111:051 DCC-MDR - Invalid Parameter
111:052 DCC-MDR - Invalid Overlay Address
111:060 ODIF Path Already Open
111:061 ODIF Path Not Open
111:062 ODIF Open Mode Error
111:063 ODIF I/O Mode Error
111:100 DCC Startup Failed - Timeout
111:101 DCC Request Failed - Timeout
111:102 DCC Unknown Request Code
111:103 DCC Invalid Parameter
111:104 DCC Overlay Not Loaded
111:105 DCC Software Version Not Compatible
111:110 TCS Invalid Timecode Format
111:111 TCS Timecode Bcd Error
111:120 TCS Unknown Device Id
111:121 TCS Transport Must Be Stopped
111:122 TCS Invalid Line In Configuration File
111:123 TCS Invalid Configuration Option
111:124 TCS Invalid Device Name
111:125 TCS Invalid Path Name
111:126 TCS Parameter Expected
111:127 TCS Device Name Not Found
111:150 TCS Invalid Time Range
111:151 TCS Invalid Time1 Parameter
111:152 TCS Invalid Time2 Parameter
111:153 TCS Invalid Autorecord Cmd
111:154 TCS Invalid Mode
111:170 TCS Invalid Master Clock Source
111:200 TCS Device Cannot Be Master
111:201 TCS Device Cannot Be Slave
111:202 TCS Illegal Device Configuration Msg
111:203 TCS Another Master Machine Already Online
111:204 TCS Cannot Change Machine While It Is Online
111:205 TCS Device Already Selected On M1
111:206 TCS Device Already Selected On M2
111:207 TCS Both Sony_B And Remote Cannot Be Online
111:208 INPUTSYNC CONFLICTS WITH LTC LOCK TO MASTER, TRY USING AES SYNC
151:000 No OMF error
151:001 Bad OMF open
151:002 Bad OMF Header
151:003 OMF No byte order

151:004 OMF Error Sample Read
151:005 OMF Error Sample Write
151:006 OMF Error Decompress
151:007 OMF No Data
151:008 OMF Source MOB List
151:009 OMF No Media Descriptor
151:010 OMF Bad TIFF Version
151:011 OMF Bad Descriptor Sample Rate
151:012 OMF Bad Descriptor Length
151:013 OMF Buffer To Small
151:014 OMF Internal MDO error
151:015 OMF Bad Compression Format
151:016 OMF Bad PIX format
151:017 OMF Bad Layout
151:018 OMF Compression Write Error
151:019 OMF Compression Read Error
151:020 OMF Bad Component
151:021 OMF Bad JPEG Baseline
151:022 OMF Bad JPEG Info
151:023 OMF 24 Bit Video
151:024 OMF Internal HNF Error
151:025 OMF Bad TIFF Count
151:026 OMF No Samples Written
151:027 OMF Error Create First
151:028 OMF Code Not Allowed
151:029 OMF JPEG Table Invalid
151:030 OMF Bad Session
151:031 OMF OPEN Bad Session
151:032 OMF META Bad Session
151:033 OMF CLOSE Bad Session
151:034 OMF Bad Close
151:035 OMF Trying to Access Null Object
151:036 OMF Bad Container
151:037 OMF Not OMFI File
151:038 OMF Error Internal CNF
151:039 OMF No Media Type
151:040 OMF Open First
151:041 OMF Null MOBID
151:042 OMF Null MT
151:043 OMF Null DESC
151:044 OMF Bad Media Index
151:045 OMF Can't read yet
151:046 OMF Bad Media Type
151:047 OMF Bad Object
151:048 OMF Corrupt VINFO
151:049 OMF No Memory

151:050 OMF Bad Q Table
151:051 OMF Bad AC Table
151:052 OMF Bad DC Table
151:053 OMF Bad Frame Index
151:054 OMF Bad Frame Offset
151:055 OMF Bad Data Address
151:056 OMF Bento Problem
151:057 OMF Bad Object
151:058 OMF Bad Index
151:059 OMF Internal ANF
151:060 OMF Bad A Structure
151:061 OMF Internal NAT
151:062 OMF No MOBID Property
151:063 OMF Bad Audio Type
151:064 OMF Bad Internal NWT
151:065 OMF Bad AIFC Data
151:066 OMF Bad WAVEData
151:067 OMF Internal ADO
151:068 OMF No Audio Converter
151:069 OMF JPEG CM
151:070 OMF JPEG Disabled
151:071 OMF JPEG Problem
151:072 OMF Bad Export PIX Format
151:073 OMF Bad Export Layout
151:074 OMF Bad Export Compression
151:075 OMF Bad RW Lines
151:076 OMF Internal Data MOBID
151:077 OMF Illegal Set Frame Number
151:078 OMF Bad Sample Offset
151:079 OMF Invalid Linkage
151:080 OMF Invalid MOB Usage
151:081 OMF Invalid Byte Order
151:082 OMF Invalid Attribute Kind
151:083 OMF Required Positive
151:084 OMF Invalid Track Kind
151:085 OMF Invalid Edge Type
151:086 OMF Invalid Film Type
151:087 OMF Invalid MOB Type
151:088 OMF Invalid Track Type Reference
151:089 OMF Invalid Object
151:090 OMF Bad Virtual Create
151:091 OMF Invalid Class ID
151:092 OMF Bad Data Export Compression
151:093 OMF Bad LRC Data
151:094 OMF LRC Is Disabled
151:095 OMF Version Not Supported

151:096 OMF Invalid LRC BLEN
151:097 OMF LRC Descriptor Error
151:098 OMF LRC Mono Only
151:099 OMF LRC Bad Sample Size
151:100 OMF LRC No Seek
071:001 GFX Unknown Attribute Type
071:002 GFX Invalid Attribute Value
071:003 GFX Incompatible or Unknown Graphics Card
071:004 GFX Control Latch Error
071:005 GFX Invalid GFX Object
071:006 GFX Link Error
071:007 GFX Invalid Application Context
071:008 GFX Version Mismatch
071:009 GFX Window Mgr Error
071:010 GFX Geometry Error
071:011 GFX No Root Window
071:012 The GFX Window Mgr is Not Running
071:013 The GFX Window Mgr is Already Running
071:014 Invalid GFX Textport
071:015 Uninitialised GFX Textport
146:001 Flight - Mailbox in Wrong State
146:002 Flight - IPI Timeout
146:003 Flight - DCC Timeout
146:004 Flight - Message Port Init Error
146:005 Flight - Message Queue Full
146:006 Flight - iplock Timeout
146:007 Flight - Semaphore Table Full
146:008 Flight - Semaphore Busy
146:009 Flight - Semaphore Timeout
146:010 Flight - Semaphore Counter Overflow
146:011 Flight - Invalid Semaphore Id
146:012 Flight - Invalid IPL ID
146:013 Flight - Invalid IPI Level
146:014 Flight - Mutex Table Full
146:016 Flight - Mutex Timeout
146:017 Flight - Invalid Mutex ID
146:018 Flight - Too Many Mutexes for one Process
146:019 Flight - Mutex not owned by Process
146:020 Flight - Mutex Deadlock
146:021 Flight - Invalid Ackport Flag State
146:022 Flight - Invalid Ackport ID
146:023 Flight - Invalid DCL ID
146:024 Flight - Restart Timeout
146:025 Flight - Semaphore Initialised
146:026 Flight - Semaphore Released
146:027 Flight - Mutex Released

146:028 Flight - AckPort Released
254:001 ESPMSG Too Many Receivers
254:002 ESPMSG Too Many Senders
254:003 ESPMSG Too Many Ports
254:004 ESPMSG No Receiver For Port
254:005 ESPMSG No Sender
254:006 ESPMSG Version Error
254:007 ESPMSG Invalid Port Id
254:008 ESPMSG Invalid Receiver Id
254:009 ESPMSG Not Owner Of Receiver
254:010 ESPMSG Port Already Linked To Receiver
254:011 ESPMSG Global Directory Module Not Linked
254:012 ESPMSG Argument Error
254:013 ESPMSG Portname Not Found
254:014 ESPMSG Signal Received
254:015 ESPMSG Receive Timeout
254:016 ESPMSG Send (Queue Full) Timeout
254:017 ESPMSG Send (Acknowledge) Timeout
084:001 MACRO FULL
084:002 MACRO RAM FULL
084:003 CONSOLE PKT ERROR
084:004 CONSOLE PKT OVERFLOW
084:005 CONSOLE PKT SIZE ERROR
084:006 CONSOLE PKT TARGET ERROR
084:007 CONSOLE GROUP ATTACH ERROR
084:008 CONSOLE GROUP CONFLICT
084:009 CONSOLE PANEL ERROR
084:010 CONSOLE UNDO UNDERFLOW
083:001 CD-ROM Error
083:002 Cant Open Path to Port/Device
083:003 Cant Link to CD-ROM Device
083:004 Unable to Locate a CDROM Drive on the SCSI Bus
083:005 Unable to Close Session Correctly
083:006 Error Writing Data to CD-ROM
083:007 Number of Bytes to Write is NOT an integral number of CD Blocks
083:008 Cant Get Next Writeable Address
083:009 Cant Erase CD-ROM Media
083:010 Cant Convert Samples into MSF Exactly!
083:011 Track Number Out of Range
083:012 Index Number Out of Range
083:013 Table of Contents Overflow (max 4096)
083:014 Cant Send Table of Contents
083:015 Unknown Directive in configuration File
083:016 Auto TOC Given an Uneven Number of Bytes to Write
083:017 Cant Create Table of Contents File
083:018 Cant Get Memory for Table of Contents

083:019 Cant Get Media Catalogue Number From CD
083:020 Unable to Get Table of Contents From CD
083:021 Cant Get ISRC Number From CD
083:022 Can't get size of Audio File
083:023 Can't Seek to Start of Audio File
083:024 Could not Read in WAV Header
083:025 RIFF ID Not Found in WAV File Header
083:026 WAVE ID Not Found in WAV File Header
083:027 FORMAT ID Not Found in WAV File Header
083:028 WAV File is NOT in PCM Format
083:029 WAV File is NOT at a The Correct Sample Rate
083:030 WAV File is NOT in 16 bit Samples
083:031 WAV File data is NOT in 4 byte chunks
083:032 Could not Read Audio File
083:033 Can't Seek to Start of Audio Data
083:034 Data Offset in ODD Position Within File
083:035 File Size Mismatch - NOT a Valid WAV File
083:036 No Audio File Specified
083:037 Cannot Allocate Best Memory for Disk Transfer
083:038 Unable to Open Configuratrion File
083:039 Unable to Open Audio File
083:040 Not Enough Samples in WAV File to Fulfil TOC Requirements
083:041 Cant Set Media Catalogue Number
083:042 Cant Set ISRC Number
083:043 Current CD is NOT Blank - Replace with Blank CD
083:044 Cant Get Track Information From CD
083:045 Cant Get Disk Information
083:046 Cant Read Buffer Capacity
083:047 Track 1 Must Start at Time Zero
083:048 Cant Decode Table of Contents
083:049 Cant Create WAV File
083:050 Cant Write WAV File Header
083:051 No CD Media Inserted - Insert a Disk
083:052 Unimplemented Data Type
066:001 StarGate timeout
066:002 StarGate Abort
066:003 StarGate Error
066:004 StarGate IOmalloc error
066:005 StarGate Disconnected

30.3 Blue Key Reference

A - Arm	Shows the amount of recording time left on the current disk drive, the record mode, the monitor mode and the level meters.
D - Devices	Shows the devices currently connected to the system.
E - EQ	Shows the EQ applied to a clip.
F - Files	Shows the network nodes, devices, folders and files available to the system.
G - Dynamics	Dynamics are not implemented.
I - Debug	R&D use only
K - Clips	Shows information for clips lying under the cursor on the selected track. This includes layer, name, mono/stereo, level, duration and source file.
L - Libraries	Shows the libraries used in a project.
M - Marks	Shows the marks in a project.
N - Clip Names	Shows the GoTo Clip Name list
P - Patching	Shows the patching of inputs to tracks.
Q - Debug	R&D use only.
R - Ram	R&D use only.
S - System Config	Shows system preferences and configuration. Settings are changed with the mouse.
T - Tracks	Shows the Track display.
W - Waveforms	Shows a list of the project's waveforms. By default, this only shows the waveforms not referenced by clips in the project. Typing "ws a <return>" will show all waveforms. Typing "ws n <return> will return to default operation.
X - Cross Fade	Shows the fade curves.
Z - Debug	Shows system messages and errors.

30.4 OS/9 COMMANDS

ATTR

Function: Display or change file attributes

Syntax: attr [<opts>] {<path> [<opts>] <permissions>}

Attributes: d s pe pw pr e w r

'-' turns attribute on

'-n' turns attribute off

Options:

-a	do not print attributes after changes
-x	directory to search is execution directory
-z	get list of file names from standard input
-z=<path>	get list of file names from <path>

CHD

Function: Change current directory

Syntax: chd <path>

COPY

Function: Copy data from one path to another

Syntax: copy [<opts>] <srcpath> [<dstpath>] [<opts>]

Options:

-a	abort on error
-b=<size>	buffer size
-f	rewrite destination files with no write permission
-p	don't print file names copied (with -w option only)
-r	rewrite destination
-v	verify integrity of files written
-w=<dir name>	wild card copy to <dir name>
-x	look in execution directory for source
-z	get list of file names from standard input
-z=<path>	get list of file names from <path>

CRC

Function: Generate crc for a file

Syntax: crc [-<options>] <file> [-<options>]

Options:

-f	generate default output file
-f=<file>	specify output file
-h	display help
-r	replace output file

DATE

Function: Display system date and time

Syntax: date [<opts>]

Options:

-j	print day, seconds past midnight in julian time
-m	print hour:minute:sec in military format

Dcheck

Function: Check directory/file integrity

Syntax: dcheck [<opts>] <devnam>

Options:

-d=<num>	print path to dir <num> deep
-r	rebuild allocation map from file structure
-y	answer “y” to all questions in repair mode

DEL

Function: Delete files

Syntax: del [<opts>] {<file> [<opts>]}

Options:

-e	erases the disk space that the file occupied
-f	delete files with no write permission
-p	show file name and ask before deleting
-x	delete files from execution directory
-z	get list of file names from standard input
-z=<path>	get list of file names from <path>

DELDIR

Function: Delete a directory

Syntax: deldir [<opts>] {<dir> [<opts>]}

Options:

-q	delete directories without asking questions
-f	delete files with no write permission
-z	get list of directory names from standard input
-z=<path>	get list of directory names from <path>

DF

Function: Print Disks/Tape Drives Found and Mounted on The System

Syntax: df [<opts>]

Options:

-e	Debug Listing
-t=<name>	Only display info with devices with file manager type <name>
-z	Debug Enable

DIR

Function: Display directory contents

Syntax: dir [<opts>] {<dir names> [<opts>]}

Options:

-a	show all files
-d	show directories with a slash
-e	extended dir listing
-n	treat dirs like files
-r	recursive dir listings
-r=<num>	recursive dir listing to depth <num>
-s	unsorted dir listing
-u	unformatted listing
-x	directory is execution dir
-z	get list of dir names from standard input
-z=<path>	get list of dir names from <path>

DISKINIT

Function: Initialise a disk drive

Syntax: diskinit <device>[<size>]

<device>	= device name
<size>	= total sectors (DD.TOT) (dec or $hex)

Options:

-a=<number of allocated sectors>	
-c=<sectors/cluster> (default = 1)	
-d=<min sectors in root dir>	
-i	... <device> is image file
-m=<max sectors in bit map>	
-n=<volume name> (default = 'Blank')	
-p=<partition start sector> (dec or $hex)	
-q	... quiet - do not prompt user
-r	... do not read device
-s	... do not display parameters
-v=<logical block size in bytes>	
-x	... do not use old DD parameters
-z	... read DD.TOT from [scsi] drive
-b	Search for bad blocks before initialization. That might take few hours on larger disks.
-w	initializes partition as FLFS (>4 Gb). Only options -n, -q, -s from the above list can be used with this one

DRT

Function: Test transfer rates.

Syntax: drt -<options> [device] -<options>

Options:

-b=<num>	Size of each read/write in Kb
-a=<hex>	Set Turbo SCSI Synchronous Period
-o=<hex>	Set Turbo SCSI Synchronous Offset
-t=<num>	Number of tracks to seek around
-m=<num)	Seek span per track in Mb
-r=<num)	Number of bytes to read/write in Mb
-h	Heavy seeking (see seek table)

-e	Dont Limit Test to 4096 MB
-i	Do non seek test on last <option r> Mb of Disk
-www	Write to Disk !!!!!
-p	Dont Attempt to Find Sync Card Shared RAM
-s	Print Seek Table
-l=<num>	Run Task at priority <num> (default:1024)
-x	Dont restore synchronous variables on exit
-d	DMA into DCC Memory

DUMP

Function: Formatted display of contents of a device

Syntax: dump [<opts>] <path> [<starting offset>] [<opts>]

Options:

-c	don't compress duplicate lines
-m	dump from a memory resident module
-s	interpret starting offset as sector number
-x	path implies execution directory

ECHO

Function: Echo text to output path and convert hex to ASCII

Syntax: echo [<opts>] [<text>] [<opts>]

Options:

-n	separate text with carriage returns
-r	don't send out a return on exit
-z	get text from standard input
-z=<file>	get text from <file>

ERRMESG

Function: Translate error message

usage: errmesg <options> errorcode<:errorcode> <options>

errmesg num:num where num:num is two decimal numbers

errmesg num where num is a single decimal number

If a single number is prefixed by 0x then that number is used as a full 16 bit HEX error code. The program can be made to exit with the supplied error code with -x.

FIND

Function: Find a file

Syntax: find [<opts>] [<root directory>] <file>

Options:

-d	show directories searched
-a	find all occurrences

FREE

Function: Report free space on disk

Syntax: free [<opts>] {<device> [<opts>]}

Options:

-b=<size>	buffer size

FTP

Function: Connect to a remote internet site and transfer files

Syntax: ftp [<opts>] [<host>] [<opts>]

Options:

-d:	Turn on debug mode.
-g:	Turn off wildcard expansions (name globbing).
-n:	Disable Auto-login to host.
-r:	Overwrite the existing file on get command.
-s:	Do not pre-extend file on received data.
-v:	Verify verbose mode is enabled.

FTPD

Function: Ftp remote file transfer server

Syntax: ftpd [<opts>]

Options:

-d:	Print debugging info to stderr.
-l:	Print logins to stderr

FTPDC

Function: Ftp remote file transfer server handler

Syntax: ftpdc [<opts>]

Options:

-d:	Print debugging info to stderr
-l:	Print logins to stderr

MUST BE FORKED FROM FTPD!

GREP

Function: Searches input module for lines matching expression

Syntax: grep [<opts>] [<expression>] {[<path>] [<opts>]}

Options:

-c	count match lines
-e=expr	same as simple expression
-f=file	read 'file' for expression(s)
-l	print only filenames with matches
-n	number each output line (file relative)
-s	silent mode
-v	invert sense of compare (list non-matches)
-z	get list of file names from standard input
-z=<path>	get list of file names from <path>

IDBGEN

Function: Generate network database module

Syntax: idbgen [<opts>] [<file-name>] [<opts>]

Options:

-d=<path>	Directory to look in to find network database files
default = <current directory)	
-r=<num>	Set module revision to <num>
-to[=]<name>	Specify target operating system
<name>	target operating system OSK OS-9/68K OS9000 or OS9K OS-9000 default operating system = OSK
-tp[=]<name>	Specify target processor and options <name> target processor(s) 68k or 68000 Motorola 000/68010/68070 CPU32 Motorola 68300 family 020 or 68020 Motorola 8020/68030/68040 040 or 68040 Motorola 68040 386 or 80386 Intel 0386/80486/Pentium(tm) PPC Generic PowerPC(tm) Processor 403 PPC 403 601 MPC 601 603 MPC 603 default processor = 68k
-x	Place module in execution directory.

LINK

Function: Link a module in memory

Syntax: link [<opts>] {<modname> [<opts>]}

Options:

-z	get list of module names from standard input.
-z=<path>	get list of module names from <path>

LIST

Function: List a file

Syntax: list [<opts>] {<path> [<opts>]}

Options:

-z	get list of file names from standard input
-z=<path>	get list of file names from <path>

LOAD

Function: Load a module into memory

Syntax: load [<opts>] {<module> [<opts>]}

Options:

-d	load file from data directory
-l	print pathlist of file loaded
-z	get list of module names from standard input
-z=<file>	get list of module names from <file>

LOGIN

Function: Provides system login security

Syntax: login [<opts>] <name> [,] <password>

Options:

-n	operate in non-interactive mode (super user only)

MAKDIR

Function: Create a directory

Syntax: makdir [<opts>] {<dir name> [<opts>]}

Options:

-x	create directory in execution directory
-z	get list of dir names from standard input
-z=<file>	get list of dir names from <file>

MAKE

Function: Keep track of modules for a file

Syntax: make {[<-opts>] [< target file >] [< macros >]}

Options:

-b	don't use built-in rules
-bo	don't use built-in rules for object files
-d	debug mode, print out the file dates in makefile
-dd	double debug mode, very verbose
-f[=]<xxx>	use <xxx> as the makefile (default: makefile)
-f-	reads the makefile from stdin
-i	ignore errors on commands and keep going
-mode[=]<mode>	rule mode (c89, compat, ucc)
-n	don't execute commands, just print them out
-o	don't assume object files need ROF files
-r	show built-in rules for current mode
-s	silent mode, execute commands without echoing them
-t	update the dates without executing the commands
-u	do the make whether it needs it or not
-x	use the cross compiler
-z[=<path>]	get list of files to make from stdin or path

Command line parameters override the MWMAKEOPTS environment variable

MARCH

Function: Create and retrieve achives.

Syntax: march [<file1>] [<files....>]

Options:

-a	Allocate any type of memory for doing transfers
-d=dev	Set Archive Device (default is /mt0)
-c	Put Files on Archive Device
-e	Print Extended Infomation for files on archive device
-h=num	Dump first <num> bytes of file on Archive Device

-k	Keep filenames as is when doing a transfer
-l	List Library files within MDR Files
-x	Extract files from Archive Device
-z	Debug Enable

OS9GEN

Function: Creates boot on disk

Syntax: os9gen {<opts>} <device> {<path>} {<opts>}

Options:

-b=<size>	copy buffer size (default 64k)
-e	extended boot (large >64k or fragmented)
-q=<path>	quick gen .. set sector zero pointing to <path>
-r	remove pointer to boot file (does not delete file)
-x	pathlists relative to execution directory
-z[=<path>]	read list of files from standard input or <path>

PATHS

Function: Display process paths

Syntax: paths {opts}

Options:

-e	display every valid process

PD

Function: Print current directory

Syntax: pd

RENAME

Function: Rename a file or directory

Syntax: rename [<opts>] <path> <name> [<opts>]

Options:

-x	path starts from execution dir

SETIME

Function: Set system date and time

Syntax: setime [<opt>] [yy mm dd hh mm ss] [am/pm]

Options:

-d	don't display time
-s	setime for battery backed-up clocks

UNLINK

Function: Unlink modules from memory

Syntax: unlink [<opts>] {<modname> [<opts>]}

Options:

-z	get list of module names from standard input
-z=<path>	get list of module names from <path>

UPGRADE

Function: Utility to Install an MFX release from File or Tape - Version 1.15

Syntax: upgrade -<options>

Options:

-f=<file>	Absolute Pathlist to MFX3 Software Image
-d=<device>	Search Root of <device> for release files
-n=<name>	Name to Give new disk if and when it is formatted (default:MFX3)
-t	Use tape device (default:/mt0)
-s	Don't sort release files when browsing
-g	Don't OS9GEN disk

XRELEASE

Function: Utility to Generate an MFX release File or Tape

Syntax: xrelease -<options>

Options:

-d=<num>	Tape Density (see tapemode -? for codes)
-e	Eject Tape After Writing
-f=<file>	Name of release file to create (can be SBF device)
-l=<file>	Name of release inventory file (default:release.list)
-r=<file>	Name of existing release file to put to tape (used with -t op
tion)	
-u=<file>	Name of source release file for update
-t	Use this if option f is an SBF device
-z=<num>	Compression 0=none 1=least 9=most (default:5)
-q	tar print errors only

If only option t is specified then default SBF device is /mt0

The Default name of the release file when not a tape device is the name of the MFX revision in the current data directory.

If filename ends in '/' then it specifies the name of the directory in which the release file is to be created with default name

If a source release file is specified with option u then an update file is generated to update from the source release to the current release.

This command is normally invoked at the root directory.

When option t is used the data on the tape is NOT compressed.

30.5 ECNs

The following pages contain tables detailing the current Engineering Chane Notices for the MFX3plus

Compliled by Noel Plummer

ECNs for 010 Card as at 11/6/99

ECN Number	Assembly	New Assembly	Current Rev	New Rev	Date	Description	Name	Special Note	Reason	Details
MFX 67.3	ESP-MFX 010		**1, 2.1, 3**	**1.1, 2.2, 3.1**	22-Mar-95	MFX Console CPU.	Rajeev Ganesh	Change in Line 1 of Rev 2 PCB	To increase the brightness of MFX Console LEDs.	Rev 1 PCB IC 74HC123 at location U4 has to be National Semiconductor Change R12 from 3K3 to 3K9. Mark PCB as Rev 1.1. Rev 2 PCB IC 74HC123 at location U44 has to be National Semiconductor Change R74 from 3K3 to 3K9. Mark PCB as Rev 2.2. Rev 3 PCB IC 74HC123 at location U50 and U44 has to be National Change R74 from 3K3 to 3K9. Mark PCB as Rev 3.1.
MFX 69.1	ESP-MFX010		**1.1, 2.2, 3.1**	**1.2, 2.3, 3.2**	22-Dec-94	MFX Console CPU	Chris Alfred	Correction in typing error on line 2 of Rev 1 PCB.	Allow Genius brand mouse to be used with MFX console. This change should allow any mouse which runs in Microsoft Windows to work on the MFX console.	Rev 1 PCB Disconnect 150R 0.5W modification resistor from U51/1 (14C88), and connect to U51/14. Mark PCB as Rev 1.2. Rev 2 PCB Cut component side track to R2 (150R 0.5W) at end nearest J3. Connect R1 end nearest J3 to R2 end nearest J3. Mark PCB as rev 2.3. Rev 3 PCB Cut component side track to R2 (150R 0.5W) at end nearest J3. Connect R1 end nearest J3 to R2 end nearest J3. Mark PCB as rev 3.2
MFX 70.1	MFX010		**1.2**	**1.3**	01-Feb-95	MFX Console CPU	Chris Alfred		New v6.02 EPROM diagnostics fix Watch Dog test, corrects key names for MFX3 and mouse diagnostic works for Microsoft (2 button) mouse. In MFX3 only the Microsoft mouse (sometimes labelled as 2 button mouse) is used as this format is emulated by all mice. If the system has a 3 button mouse with a selection switch, the switch should be set to MS or 2 so it operates in Microsoft mode. 3 button mice with no selection switch initialises to Microsoft mode. Although this EPROM will work with MFX2 systems, the EPROM diagnostics are now tailored for MFX3. MFX2 systems should use v6.01. MFX3 systems should use v6.02 or higher.	For Rev 1 1. Change U54 to KMON 6.02U. 2. Change U53 to KMON 6.02L. 3. Update revision of PCB. For Rev 2,3 1. Change U48 to KMON 6.02U. 2. Change U49 to KMON 6.02L. 3. Update Revision of PCB.
MFX 86.2	MFX-010		**2.4, 3.3**	**2.5, 3.4**	29-Mar-95	MFX Console CPU	Chris Alfred		To reduce speaker buzz.	Connect 1000uF/16V Radial Electrolytic Capacitor P/No. PCEC7137 between U12/9 and U12/10 such that the negative terminal is connected to U12/9 and the positive to U12/10. Glue the Capacitor to the PCB. Update Revision to 2.5 or 3.4 as appropriate
MFX 100.2	MFX-010		**2.5, 3.4**	**2.6, 3.5**	08-Aug-95	Console Card	Leith Stewart	Affects only those boards using the new LCD DV-40200.	Change of manufacturer for LCD from DMC40202NY-LY to a DV-40200 requires modification to the board.	1. Replace RV2 (10k Ohm pot) with a 1K Ohm pot (Fairlight Part Number: POTR6117). 2. Cut the pin on the pot closest to U11. Make this cut as close to the body of the pot as possible with no more than 1mm exposed. 3. Drill out the hole under RV2 to 4mm. Place a transistor standoff (Fairlight Part no: SDTD3001, RAE Part no: T05-Standoff) in the hole before placing the trim pot. This spacer is to keep the pot away from the board to avoid shorting tracks. 4. *NB* Modify all boards using the Bourns trim pots (ie blue flat mounting type).
MFX 115.2	MFX-010		**2.6, 3.5**	**2.7, 3.6**	16-Apr-96	MFX Console CPU Card	Noel Plummer	This ECN overrides ECNs 115 & 115.1	Jogger wheel direction aliases when spun quickly. If jogger wheel is spun quickly within MDR or the diagnostics, the direction swaps due to the CPU under sampling the jogger wheel. Note that the EPROMs installed in step 2 are only for the MFX console jogger wheel diagnostics to operate correctly. If EPROMs are not available during field upgrade, step 2 can be omitted and the jogger wheel checked in MDR.	PCB Rev: 2.0 1. Remove solder side mod wire, U23 2-5. (W3 should still short pins 1-2). 2. Insert a 74LS74 IC (P/N SITA0074) into IC Socket at U23. 3. Change U48 (27C256) to MFX6_03U. Change U49 (27C256) to MFX6_03L. PCB Rev: 3.0 1. Change W6 to short pins 2-3. (W3 should still short pins 1-2). 2. Change U48 (27C256) to MFX6_03U. Change U49 (27C256) to MFX6_03L. Changes: Details of changes to rev 2 PCB added.
MFX 121.2	MFX010		**3.6 6.0**	**3.7 6.1**	06-Sep-96	Console CPU Card	Leith Stewart		To prevent the battery BR2325 (BT1) from charging, as per UL requirements.	1. Cut track (on solder side) between J12/1 and +ve terminal of battery BT1. 2. Connect a Schottky Diode (MBR120P P/N SDTD5024), on solder side, between J12/1 & +ve terminal of battery BT1 with cathode closest to J12/1. CHANGES MADE: 121.1 Diode orientation corrected and rev 6 PCB added. 121.2 Track cuts corrected.

ECN Number	Assembly	New Assembly	Current Rev	New Rev	Date	Description	Name	Special Note	Reason	Details
MFX 135.1	MFX-010		**3.7, 6.1**	**3.8, 6.2**	17-Jul-96	Console CPU Card	Rajeev Ganesh		To conform to UL requirements.	Ensure that the battery at location BT1 is one of the following only: Mitsubishi type CR2325. Rayovac type BR2325. Seiko type CR2325. Panasonic (Matsushita) type BR2325 (Sanyo not acceptable).
MFX 137	MFX-010		**3.8, 6.2**	**3.9, 6.3**	07-May-96	Console CPU Card	Rajeev Ganesh		To conform to UL requirements	Cable from PCB (J1) to Power supply needs to use UL recognised leads (AVLV2) with VW-1 insulation rated 30V minimum. All leads rated minimum 60 degree C.
MFX 139	MFX-010		**3.9** **6.3**	**3.10** **6.4**	07-Jun-96	Console CPU Card	Erik de Castro Lopo	Applies to UL, EMC and Standard MFX-010 boards.	Change of ROM required for EMC compliance. (For simplicity this ROM will be fitted to all new production.)	Change U48 (27C256) to MFX6_04U. Change U49 (27C256) to MFX6_04L. Note: Not required for existing boards in the feild.
MFX 144.1	MFX010	MFX010E	**6.4**	**6.4**	26-Sep-96	Console CPU Card	Leith Stewart		Modification to delivered MFX-010 boards is required to fit the LDC-30 power supply for EMC consoles.	1. The wires connected to J1 are to be fitted with a different connector housing and crimp pins in order to fit the LDC-30 power supply (Fairlight P/N PSUG8030) on EMC consoles. 2. Cut off the crimp pins at the end of the wires from J1 supplied with the standard MFX-010. 3. Crimp connect pins (JST P/N SVH-21T-1.1 or SVH-21T-P1.1) to the ends of all wires. The connector housing and pins are supplied with the power supply. 4. Fit connector housing (JST P/N VHR-6N) in the following manner; CN2 (Power Supply) J1 (MFX-010) Pin 1 - -12V (CABG212 - 16x0.2 UL1007 Blue) Pin 3 Pin 2 - Gnd (CABG108 - 16x0.2 UL1007 Grey) Pin 2 Pin 3 - Not used Pin 4 - +12V (CABG103 - 16x0.2 UL1007 Orange) Pin 1 Pin 5 - Gnd (CABG121 - 24X0.2 UL1015 Black) Pin 5 Pin 6 - +5V (CABG120 - 24X0.2 UL1015 Red) Pin 4 5. Mate connector to CN2 on LDC-30. Changes: Fix error in Revision Number. New product code for PSU.
MFX 150.5	MFX-010		**6.4**	**6.5**	20-Nov-96	Console CPU Card	Leith Stewart	This change accomodates the implementation of MFX ECN #151 and FAME ECN #3.	Replacement of connector at J1 is required to accomodate the introduction of new power connection assemblies for new consoles.	1. Remove all wires soldered to position J1. 2. At J1, place connector MOLEX 5289-06 (Fairlight P/N COND5280H - 6 PIN MOLEX HEADER WITH LOCKING RAMP) or UL Recognised equivalent. In case of non-availability of connector use three MOLEX 5281-2A (Molex O/N 10-32-1021, Fairlight P/N COND5282H) or UL Recognised equivalent, positioned side by side and closest to pin 1. Remove last pin from third connector to allow the connector to clear the keyed footprint. 3. Re-label board Rev 6.5. Changes: Added third connector.
MFX 153.3	MFX010	MFX010	**6.5**	**6.6**	18-Oct-96	Console CPU Card	Leith Stewart	This ECN to be implemented with ECN 152.	To facilate easy adjustment of both the speaker volume and the display contrast the adjustment pots on the MFX010 card are to moved to the MFK card.	1. Delete or remove 10k trim pot at RV1 (ESP part # POTR6114) 2. Delete or remove 1k trim pot at RV2 (ESP part # POTR6117) 3. Solder cable assembly (Fairlight P/N CABM6259) into the holes (on component side) vacated by the above trim pots using the following connections; RV1 (pin closest LS1) Black J4/1 RV1 (pin closest R5) Brown J4/2 RV1 (pin closest RV2) Red J4/3 RV2 (pin closest RV1) Orange J5/1 Rv2 (pin closest C13) Yellow J5/2 RV2 (pin closest W9) Green J5/3 4. Mate connector on end of cable CABM6259 with header on J4 & J5 (N.B there is a single 6 pin header used for the two positions). 5. Relabel board Rev 6.6. Changes: Added references for connection of wires. Fix error in Revision Number. Change direction of pot movement.
MFX 154.1	MFX-010		**6.6**	**6.7**	26-Sep-96	Console CPU Card	Matt Harding	Used only in conjunction with MFK boards.	To provide diagnostics for testing keys on keyboard. Handling of new keyboard layout on MFK.	1. A new version of ROM firmware released is V7_00L & V7_00U. 2. These ROMs are to be used when constructing a console using the MFK. 3. Diagnostics behave in the same manner as the previous diagnostics. 4. Relabel board Rev 6.7. Changes: Fix error in Revision Number.
MFX 159.1	MFX-010		**6.7**	**6.8**	26-Nov-96	MFX Console CPU Card	Matthew Harding		Diagnostics do not work with Microsoft compatible mice.	1. Replace Eproms (27C256) at positions U48 and U49 with new revision firmware V8_00U and V8_00L respectively. 2. Relabel board Rev 6.8. 3. This firmware is compatible with MFK and Rev 13 Software or greater. It is also compatible with 030/040 and Rev 12 Software. 4. It is recommended that mice are used in two button mode only. The MFX uses only two buttons, and diagnostics test only for two button mice. 5. The Genius Plug & Play mouse will operate correctly without any modification when this firmware is used. Do not modify this mouse. This overrides ECN #156. Changes: Changes to hardware and software compatibility.
MFX 160.1	MFX-010		**6.8**	**6.9**	21-Nov-96	MFX Console CPU Card	Noel Plummer		50 Way connector at J10 interferes with MFK/LCD assembly when console is assembled.	1. Remove connector at J10 (COND6012 - 50W IDC with Ejectors). 2. Replace with a 2 x 25W Box Header, Gold Contacts, UL Recognised (Fairlight P/N COND6791). 3. Relabel board Rev 6.9. Changes: Fairlight P/N corrected in Detail 2

ECNs for 010 Card as at 11/6/99

ECN Number	Assembly	New Assembly	Current Rev	New Rev	Date	Description	Name	Special Note	Reason	Details
MFX 169.1	MFX-010		**6.9**	**6.1**	10-Dec-96	MFX Console CPU Card	Chris Alfred		New Version ROM released which allows use of numeric keypad and punctuation when non-volatile memory is clear. LED diagnostics on key '4'.	Change ROM at U48 to V8_01U.bin (check sum 6070) Change ROM at U49 to V8_01L.bin (check sum BE05) Changes: Check sums added.
MFX 176	MFX-010		**6.1**	**6.11**	15-Jan-96	Console CPU Card	Leith Stewart		New consoles do not require a centronics connector for connection to MFX Pus.	1. Remove connector (F/L P/N COND6766 - CONNECT CENTRONICS24W BENT PCB) from J3. This is a redundant item. Solder mask the holes before assembly. 2. When required to repair or construct an older style console (ASYM6001, ASYM6001E), fit a connector (F/L P/N COND6766 - CONNECT CENTRONICS24W BENT PCB) to position J3.
MFX 180	MFX-010		**6.11**	**6.12**	03-Feb-97	Console CPU Card	Leith Stewart		Minimum power requirement for console is outside operating parameters of power supply.	1. At J1, connect a 100 Ohm resistor between pins 1 (+12V) and 2 (Gnd). RESR1013 - RES 100R 0W4 MR25 1% 2. Relabel board Rev 6.12.
MFX 206	CABM6255		**1.2**	**1.3**	26-May-97	CABLE 010-MFK 50W IDC SIGNAL, UL	RAJEEV GANESH		CABM6255 is too short and gets strained during assembly and dis-assembly of the Console.	Length needs to be extended from 350mm to 480mm. Dawing modified and is attached.
MFX 220	MFX010		**6.12**	**6.13**	03-Sep-97	Console CPU Card	NOEL PLUMMER		Eliminate unused components. Correct speaker jumper setting.	Remove Utilux M6410-2A 2W Connector (CONG5290) at J14. Remove Diode 1N4001 - 1N4004 (SDTD5008) at D5. Install jumper at W2 between pins 1 and 2 Relabel board Rev 6.13
MFX 233	MFX-010		**6.13**	**7**	24-Nov-97	MFX Controller card	Mario Paolino		New PCB MFX-010 Rev 7 This new Rev card provides automatic switching between the Standalone and Fame PSU, incorporates wire mods and other improvements (see PRN 8)	MFX -010 Rev 7 PCB replaces the current Rev 6 All existing stock of Rev 6 is to be consumed before Rev 7 is introduced. Associated changes to the different console models are detailed as follows 1. ECN 234 CSLMFXPSA 2. ECN 235 CSLMFXP19 3. ECN 236 CSLMFXPO2R 4. FAME ECN 7 ASYM7001
MFX 242	MFX-010		**7**	**7.1**	17-Mar-98	MFX Console CPU	Noel Plummer	Attachments (1)	On none FAME consols the automatic voltage selection relay at RL1, was found to chatter on power up. This was thought to be due to interactions between the power pack and the 15,000 uF cap on +12V. The voltage selection is now to be done manually. The relay is to be replaced with headers and voltage selection between FAME and non FAME consoles will be done by moving two jumpers (shunts). The minimum power resistors at R76 and R77 have been found to run too hot.	1. Remove relay RL1, D7 (diode 1N4148), Q2 (transistor BC549), R76, R77 and R78 (resistor 100R). 2. Install two 1x3 0.1" pitch headers (Fairlight P/N CONG5264) in the left hand holes vacated by the relay. Refer to attachment. 3. Install two jumper onto header as follows: Non FAME: Jumpers on two pins closest to power connector J1. FAME: Jumpers on two pins furthest from power connector J1. 4. Install 220R 1W resistors at R76 and R77. 5. Ensure, that for a Non FAME console, that the power cable from back panel to J1 is Fairlight P/N CABM2000. 6. Ensure, that for a FAME console, that the power cable from back panel to J1 is Fairlight P/N CABM2003. This cable can be identified by the loopback wire between pins 5 and 6 on the J1 end. 7. Change assembly revision label on PCB to 7.1

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ECNs for 9PIN Card as at 11/6/99

ECN Number	Assembly	New Assembly	Current Rev	New Rev	Date	Description	Name	Special Note	Reason	Details
MFX 77	ESP-9PIN		**1**	**1**	22-Feb-95	Multi MFX and 9Pin I/F	Chris Alfred	This formalises changes currently in use.	Change ribbon cable length and PCB cutout dimensions to ease assembly.	1. Change ribbon cable length from 80mm to 60mm for ease of assembly. 2. Cut out top reaer corner (near JP1) of the PCB. Dimensions of the cutout to be 30mmx10mm as per sketch attached.
MFX 132.1	ESP-9PIN		**1**	**1.1**	29-Mar-96	Multi MFX and 9PIN I/F	Noel Plummer		ESP-9PIN PCB assemblies have been shipped with an incorrect GAL installed. Install the correct GAL to ensure that multiple interconnection of MFX3s is possible when this feature is implemented.	The incorrect GAL is labeled either "MULTI" or "9PMULTI" and has a check sum of 724F. Change or reprogram and relabel GAL to correct program called "9PIN". Verify check sum is 7D0E with programmer option: type set to no UES. Change assembly revision on PCB to 1.1 NOTE : ECN 132 had the check sum figure of CDE6 which was incorrect. The correct check sum should be 7D0E.
MFX 133	ESP-9PIN	ESP-9PIN	**1.1**	**1.2**	11-Mar-96	ESP 9Pin Control Card	Leith Stewart		To make the 9Pin card comply with EMC requirements.	1. The following changes are required as part of an overall system modification to make the MFX3 rack meet EMC requirements. It is important that this modification is carried out in conjunction with all other ECNs that outline EMC changes. 2. Viewing the board from the solder side with P3 on the lower left, fit the following; Solder a wire (24AWG) from the right hand mounting guide of P3 to the left hand mounting guide of P5. Repeat this for P5 to P4, P4 to P2, & P2 to P1. 3. Solder a wire (24AWG) from the left hand mounting guide on P3 and screw the other end to the support block, Solder a wire (24AWG) from the right hand mounting guide on P1 and screw the other end to the support block (fit a crimp connector if you wish, but not necessary). This is to ensure that all D connector metal shells have electrical continuity to the chassis. 4. When all modifications are complete, relabel PCB as Revision 1.2.
MFX 142	CABM5002 or CABM5003	CABM5002E or CABM5003E			24-Jun-96	CABLE 9PIN CONTROL SCREW SHELL or CABLE 9PIN CONTROL SLIDELOCK	Erik de Castro Lopo		To ensure EMC Compliance for 9 pin cable supplied with EMC Mainframe systems (17MFX3).	Use metal backshells (P/N CONS0900) instead of plastic or metallised plastic backshells. Use braid shielded cable (e.g. Mfgr: Schaltflex LiY-C-Y #37-0510) instead of foil shielded or unshielded cable. Ensure that the cable shield provides 360 degree connection with the backshell as shown in "screened backshell -- good" connection on the drawing attached.
MFX 254	ESP-9PIN		**1.2** **2.0**	**1.3** **2.1**	24-Aug-98	9PIN I/F CARD	Erik de Castro Lopo		External dongle malfunction.	1. On the solder side, cut the track leaving U1/pin13. 2. Connect mod wire from U1/pin12 to P1/pin5. Note to production: All WIP to be modified. Note to subcontractors: All WIP to be modified. Note to the field service: This mod is required on each unit which is using external dongle.
MFX 255	ESP-9PIN		**2.1**	**3**	24-Aug-98	9PIN I/F CARD	George Potkonyak		Cost saving: eliminate need for PCB modification	1. On the PCB layout, remove track between U1/pin 13 and P1/pin 5 2. On the PCB layout add track between U1/pin 12 and P1/ pin 5 Note: Rev. 3.0 assembly is functionally identical to Rev. 2.1
MFX 256.1	ESP-9PIN		**2.1**	**2.1**	29-Sep-98	9Pin I/F Card	George Potkonyak	This ECN cancells out ECN # 256, which is no longer applicable. Refer ECN # 254.	Error in ECN # 256	Use ECN # 254
MFX 278	ESP-9PIN		**3**	**3.1**	09-Feb-99	9Pin I/F Card	Noel Plummer		The 9 pin D connectors on this card have insufficient reach and therefore do not protrude far enough out of the dress panel. This has been found to cause unreliable mating.	1. Change the Female D Connector at P4 to Fairlight P/N: JDF9062 Desc: DB9M Footprint = 9.4mm reach, Solder locating lugs, Select Gold (Au) >= 0.25um/10u". Manufacturer: U.L. Recognised, non-critical 2. Change the Male D Connectors at P3 and P5 to Fairlight P/N: COND7000 Desc: DB9M Footprint = 9.4mm reach, Solder locating lugs, Select Gold (Au) >= 0.25um/10u". Manufacturer: U.L. Recognised, non-critical 3. Re-label PCB as Revision 3.1.

ECNs for AIO Card as at 11/6/99

ECN Number	Assembly	New Assembly	Current Rev	New Rev	Date	Description	Name	Special Note	Reason	Details
MFX 20.2	ESP-AIO		**2**	**2.1**	22-Mar-95	Analog IO Card	Chris Alfred		Improve audio quality. All channels should have SNR better than 86dB, and distortion better than 0.007% This change note must be done in conjunction with Change Note 21.	1. Remove capacitors C29,C38,C60,C31,C40,C62 2. Connect 100nF mono ceramic capacitors on solder side between the following: 2.a U9/1(CS5328) & U9/28. 2.b U9/1 & U29/25. 2.c U11/1(CS5328) & U11/28. 2.d U11/1 & U11/25. 3. Connect 120pF ceramic capacitor between U4/18 (74HC244) and C28/+ on solder side. 4. Connect 1uF 16V tantalum -ve to C60/-, and +ve to C74 pin neraest U15 (AD797 or OP27). 5. Connect 1uF 16V tantalum -ve to C62/-, and +ve to C77 pin nearest U17 (AD797 or OP27). 6. Connect U7 (7905) pin nearest U8 (CS3310) to C91 pin nearest R37 using 32/0.2mm wire (same wire as used pn hard disk power). 7. Cut 2-3mm approximately off pins 6 and 7 of U9 (CS5328) before insertion and connect both pins to U9/11 (U9/11 stays in socket). 8. Cut 2-3mm approximately off pins 6 and 7 of U11 (CS5328), before insertion and connect both pins to U11/11 (U11/11 stays in socket). CHANGES: Changes in paragraphs 7 and 8.
MFX 42.1	ESP-AIO		**2.1**	**2.2**	21-Mar-95	ANALOG I/O CARD	Chris Alfred	Correction in typing error of C18 to C28 on line 6.	Improves Noise figures when DIO/AIO are installed in Analog Rack. Improves Noise figures at 48 Khz. (in conjunction with DIO ECN No. 32)	Remove U9 and U11 from their sockets. Trim pins 6 and 7 on U11 and U9 so that they are approximately equal to 2mm long. (Make sure the mod. wire on U9 and U11 is intact). De-solder and remove the sockets for U9 and U11. Solder U9 and U11 directly onto the PCB. Ensure that pins 6 and 7 of U9 and U11 do not touch the PCB or the capacitors nearby. Disconnect solder side Mod Capacitor across U4/18 and C28. On solderside, connect 120pf capacitor across U4/2 and U4/1. On solder side, connect 120pf capacitor across U4/4 and U4/1.
MFX 65.2	ESP-AIO		**2.2**	**2.3**	12-May-95	Analog IO Card	Erik de Castro Lopo		Removes DC offset on input. Improves frequency response to be within 0.05dB from 20Hz to 20kHz (measured using Neutrik with 22-22kHz filter switched off). Typically, cards produce SNR >88dB and THD <0.005% at 1kHz (measured using Neutrik with 22-22kHz filter switched on). Requires Change Note 93 to be done to ESP-DIO.	Change R5,R6,R9,R10 (all 51R) to 10uF non-polarized capacitors (16V or higher voltage rating). Connect 10k resistors across C59,C63,C61,C64 (all 10nF). Change C65,C66,C67,C68 (all 220pF) to 56pF ceramic. Label card as Rev 2.3.
MFX 246.2	ESP-AIO		**2.3**	**2.4**	25-May-98	Analog IO Card	Chris Alfred	Manufacturing ONLY	Reduced system performance when using analogue inputs.	1. Remove National Semiconductor 74HC244 at Location U4 (Manufacturer of 74HC244 at U5 is non critical) 2. Replace with Texas Instruments 74HC244. 3. Remove 10nF WIMA (Polypropeline) cap at C59, C61 4. Solder a 10nF WIMA cap between U9 pin 27 and C74 on the leg farthest from U9 5. Solder a 10nF WIMA cap between U11 pin 27 and C77 on the leg farthest from U11 6. Change card revision as detailed above
MFX 280.1	ESP-AIO2				24-Mar-99	Analog IO Card	Noel Plummer	ECN 280 Withdrawn and incorporated into ECN 282.1 to avoid confusion.	ECN Withdrawn and amalgamated into ECN282.1	ECN Withdrawn.
MFX 282.1	ESP-AIO2		**1**	**1.1**	24-Mar-99	Analog IO Card	Noel Plummer	Note that the value of the 8 resistors, in item 1 of details, has been changed again in ECN 286 and that the capacitor at C204 has been removed completely in ECN 287..	1. Improvement in Audio O/P SNR for channels 2 and 4. 2. Reduction of Audio clicks when synchronisation sources change and while MFX3 system is in Armed condition. 3. Ability to calibrate for both +22 and +24 dBu and maintain low THD figures.	1. (Refer to ECN 286) Replace 8 Resistors RME9167 (12K) with RME4818 (13K7) in locations R75, R76, R77, R78, R79, R80, R81 and R82. 2. (Refer to ECN 287) Replace Capacitor CCD1562 (220pF) with CCD3004 (330pF) in location C204 3. On component side located in bottom right section of the board, locate thin track which starts bellow C46 and ends at the via above C169. Cut this track close to C169 4. Add a wire-wrap type wire from 74HCT9046AD U36/3 to the via above C169 Note: This wire is to be kept as short as possible and run over the middle section of the board and kept flat against the board with glue 5. Change Assembly Revision Label to Rev 1.1 Note to Subcontractors: Modify all WIP of AIO2_V5 Cards Note to Fairlight Production: Modify all WIP of AIO2_V5 Cards Changes to ECN 282.1: Items 3 and 4 in details added from withdrawn ECN 280. Special Note added.
MFX 286	ESP-AIO2		**1.1**	**1.2**	11-Mar-99	Analog IO Card	George Potkonyak		Improved input level set-up reliability	1. Replace 8 Resistors RME4818 (13K7) in locations R75, R76, R77, R78, R79, R80, R81 and R82 with RME9206 (5K6, +/- 1%, SMD 0805 Metal Film) 2. Cut the 8 track bundle on the solder side as per attached instruction (page 2) 3. Add 12 wire links as per attached instruction (page 3). Wires to be secured to the PCB with an adhesive, at approx. 25 mm intervals 4. Labels PCB assembly as Rev. 1.2 Note to Subcontractors: Modify all WIP and all stock of Rev.1 PCB-s Note to Production: Modify all WIP

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ECNs for AIO Card as at 11/6/99

ECN Number	Assembly	New Assembly	Current Rev	New Rev	Date	Description	Name	Special Note	Reason	Details
MFX 287	ESP-AIO2		**1.2**	**1.3**	16-Mar-99	Analog IO Card	George Potkonyak		Damp clock signals to ensure >= 100dB SNR at +24dBu reference. The cards should have an SNR of >99.5dB at +22dBu reference	1. Change 2 Resistor values in locations R173 and R174 from 33 Ohm to 56 Ohm. 2. Change 4 Network Resistor values in locations U52, U54, U55 and U56 from 33 Ohm to 100 Ohm. 3. Remove 1 Capacitor in location C204. 4. Labels PCB assembly as Rev. 1.3 Note to Subcontractors: Modify all WIP. Note to Production: Modify all WIP.
MFX 290.1	ESP-AIO2		**1.3**	**1.4**	13-Apr-99	Analog IO Card	George Potkonyak	THIS ECN IS CORRECTION TO ECN # 290	Improve SNR to achieve a minimum of 100 dB output level.	1. Fit multilayer ceramic SMD 0603 capacitor, 68 pF, >/= 50V, +/- 20% or better (Fairlight part # CCD1180), between U39/pin1 and R173 pad away from the C204. 2. Change Card revision to Rev. 1.4 Note to Production: Modify all WIP of Rev. 1.3 cards and relabel to Rev. 1.4 Note to Subcontractors: Modify all WIP of Rev. 1.3 cards and relabel to Rev. 1.4 Note to Field Service: Modify all Rev. 1.3 cards and relabel to Rev. 1.4
MFX 293	ESP-AIO2 ESP-AO2		**1.4** **1.3**	**6.0** **6.0**	22-Apr-99	Analog IO Card and Analog O/P Card	George Potkonyak	INTRODUCTION OF REVISION 6 BLANK PCB	To eliminatet modification to the Rev. 1 AIO_V5 Card	1. Numer of tracks re-routed and a pad for Capacitor C205 added. 2. PCB Revision changed to Rev.6 (ESP-AIO2_R6)
MFX 295.1	ESP-AIO2		**6**	**6.1**	27-Apr-99	Analog IO Card	George Potkonyak	THE TRACK CUTTING AND WIRE LINK MODIFICATION SPECIFIED IN THIS ECN NEED NOT BE DONE TO REV. 1.4 CARDS. THIS ECN REPLACES ECN # 295.	Improve SNR to achieve a minimum of 97 dB output level on all channels at all sampling rates. Eliminate the "Muting" problem.	1. A multilayer ceramic capacitor added, SMD 0603, 68 pF, >/= 50V, +/- 20% or better (Fairlight part # CCD1180), in location C205 on PCB Rev. 6. 2. Cut track near U2/pin 7 (under U2) as shown on sheets 1 and 2 of the ECN attachment. 3. Cut track near U55/pin 4 as shown on sheets 1 and 3 of the ECN attachment. 4. Add wire link between U2/pin 7 and U55/pin 4, routed as shown on the sheet 4 of the ECN attachment. Glue wire link to PCB at approx. 20 mm intervals. 5. XILINGS Program in U53 changed to AIOX10.JED, with Checksums: 14B4 for JED File and xxxx for JTAG File. New Assembly Revision is Rev. 6.1 NOTE TO SUBCONTRACTORS: Modify all WIP
MFX 297	ESP-AIO2		**1.4** **1.5**	**1.5** **1.6**	27-Apr-99	Analog IO Card	George Potkonyak		To eliminate the "Muting" problem.	1. XILINX program in U53 changed to AIOX10.JED, with Checksums: 14B4 for JED File and 0x5752 for JTAG File. 2. Card revision raisd to Rev. 1.5 NOTE TO PRODUCTION: Reprogram U53 on all Cards in WIP. Relabel the U53 accordingly. Relabel Card assembly to Rev. 1.5 If SNR at 48 MHz sampling rate is below 97 dB, modify card as per ECN295.1, Items 2,3 and 4 and relabel card to Rev. 1.6 NOTE TO FIELD SERVICE: Reprogram U53 on all Cards in WIP. Relabel the U53 accordingly. Relabel Card assembly to Rev. 1.5 If SNR at 48 MHz sampling rate is below 97 dB, return card to Fairlight for modification
MFX 300	ESP-AIO2-A		**1.6** **6.1**	**1.6** **6.1**	04-May-99	Analog IO Card (+15, 16 & 18 dBu)	George Potkonyak	THIS ECN INTRODUCES A NEW VERSION OF AIO2 CARD +15, 16 & 18 dBu INPUT CLIPPING LEVEL. MINIMUM ACCEPTABLE SNR FOR THIS MODIFICATION IS 96 dB FOR ALL SAMPLING RATES, EXCEPT 32 MHz, FOR WHICH IT IS 85 dB MINIMUM.	To create a +15, 16 or 18 dBu input clipping level card from a +22 dBu input clipping level card.	1. Re-connect the mod wires from Pin 5 to Pin 6 on four IC-s (SSM2143) U23, U24, U25 and U26. THIS MOD IS APPLICABLE ONLY TO REV 1.6 CARDS (not to Rev 6.1) 2. Lift Pins 1 and 5 on four IC-s (SSM2143) U23, U24, U25 and U26 and connect a resistor between each lifted pin and its pad. Use the following resistor: 5k6, SMD 0805, Metal Film, 1% (Fairlight Part Number RME9206). THIS MOD IS APPLICABLE TO BOTH REVISIONS (1.6 and 6.1) 3. Card revisions remain unchanged (Rev. 1.6 or Rev. 6.1), however, the card part number changes to ESP-AIO2-A NOTE TO PRODUCTION: If there is a need to modify the card to +15, 16 or 18 dBu level, the card is to be labeled with a new part number ESP-AIO2-A. Revision level remains the same. NOTE TO FIELD SERVICE: Do not modify cards in the field. Request Fairlight, Sydney to supply the required stock. ADDITIONAL NOTE: ALL AIO2 CARDS LABELED WITH ESP-AIO2 (only) PART NUMBER ARE SET TO +22dBu.
MFX 302.1	ESP-AIO2		**1.6** **6.1**	**1.7** **6.2**	07-May-99	Analog IO Card	George Potkonyak	THIS ECN REPLACES ECN # 302.	To eliminae or reduce the chance of some capacitors exploding on power-up.	1. Replace two 47uF capacitors in locations C155 and C156 (which are 20V rated) with two capacitors: 22uF, Tantalum, Low ESR, SMD E-Case, 35V (Fairlight Part No. CTD9108) 2. Replace five 100uF capacitors in locations C159, C160, C161, C162 and C176 (which are 16V rated) with five capacitors: 33uF, Tantalum, Low ESR, SMD E-Case, 25V (Fairlight Part No. CTD2330) 3. Replace three 100uF capacitors in locations C163, C164 and C177 (which are 10V rated) with three capacitors: 100uF, Tantalum, Low ESR, SMD E-Case, 16V (Fairlight Part No. CTD6298 - which were taken out of C159, C160, C161, C162 and C176). 4. Card revision raisd from Rev.1.6 to Rev. 1.7 and from Rev. 6.1 to Rev. 6.2 NOTE TO PRODUCTION: Modify all Cards in WIP. Re-label Revision accordingly. NOTE TO FIELD SERVICE: Modify all Cards in service. Re-label Revision accordingly.

ECNs for AIO Card as at 11/6/99

ECN Number	Assembly	New Assembly	Current Rev	New Rev	Date	Description	Name	Special Note	Reason	Details
MFX 304	ESP-AIO2 ESP-AO2		**6.2** **6.2**	**7.0** **7.0**	19-May-99	Analog IO Card and Analog O/P Card	George Potkonyak	INTRODUCTION OF REVISION 7 BLANK PCB	To enable setting to 12 to 24 dBu using trimpots	1. Rev. 7 PCB introduced 2. IC-s in locations U7, U8, U9 and U10 changed to OPA2064AU (Fairlight Part No. SAS7843) 3. U62 and U63, OPA2134 (same as in locations U46-U41) added (Fairlight Part No. SAS3907) 4. Trim Pot values in locations R65, R66, R67 abd R68 changed to 500R Multiturn, 3224J Series, SMD (Fairlight Part No. RPT2337) 5. Resistor values in locations R75, R77, R79 and R81chnaged to 820R, Thick Film, 0.1W, 1% SMD0805 (Fairlight Part No. RME7459) 6. Link (0R0 Resistor, Fairlight Part No. RME0001) in location JP3 removed 7. Pads for Links (0R0 Resistor, Metal Film, >= 0.125W, 1%, SMD0805, Fairlight Part No. RME0001) in locations JP9, JP12, JP13, JP28 and JP29 added. Final configuration to be detrmined on test. 8. Pin Header pads in locations JP24, JP25, JP26 and JP27 added for future use. Link to be fitted between pins 1 and 2 only for 15 dBu set-up. 9. C206, C207, C208 Pads added - NOT to be populated 10. Card revision raised to Rev. 7.0
MFX 307	ESP-AIO2 ESP-AO2		**7**	**7.1**	03-May-99	Analog IO Card and Analog O/P Card	George Potkonyak	DRAFT	xxxxxxxxx	1. Replace two 68pF capacitors in locations C204 and C205 with two capacitors 33pF Multi Layer Ceramic (Fairlight Part No. CCD3997) 2. Add resistor 33R (Fairlight Part No. RME5033) at location R186 3. Add resistor 0R (Fairlight Part No. RME001) at location R179, R180, R187 4. Add capacitor 100nF Multi Layer Ceramic (Fairlight Part No. CCE4356) at locations C212, C213, C214, C215, C216 and C211 5. Replace two inductors in locations L3 and L4 with Chip Inductor 22uH (Fairlight Part No. TCS0668) 6.Card revision is raised from Rev7.0 to Rev 7.1 7. NOTE TO PRODUCTION: Modify all Cards in WIP and Re-label Revision accordingly 8. NOTE TO SERVICE: Modify all Cards in Service and Re-label Revision accordingly

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ECNs for AO Card as at 11/6/99

ECN Number	Assembly	New Assembly	Current Rev	New Rev	Date	Description	Name	Special Note	Reason	Details
MFX 94	ESP-AO		**2.2**	**2.3**	12-May-95	Analog Output (Only) Card	Erik de Castro Lopo		Improves frequency response to be within 0.05dB from 20Hz to 20kHz (measured using Neutrik with 22-22kHz filter switched off). Typically, cards produce SNR >88dB and THD <0.005% at 1kHz (measured using Neutrik with 22-22kHz filter switched on). Requires Change Note 95 to ESP-DO.	Change C65,C66,C67,C68 (all 220pF) to 56pF ceramic. Label card as Rev 2.3.
MFX 281	ESP-AO2		**1**	**1.1**	15-Feb-99	Analog O/P Card	Mario Paolino		1. Improvement in Audio O/P SNR for channels 2 and 4 2. Reduction of Audio clicks when synchronisation sources change and while MFX3 system is in Armed condition. 3. Ability to calibrate for both +22 and +24 dBu and maintain low THD figures	1. On component side located in bottom right section of the board, locate thin track which starts bellow C46 and ends at the via above C169. Cut this track close to C169 2. Add a wire-wrap type wire from 74HCT9046AD U36/3 to the via above C169 Note: This wire is to be kept as short as possible and run over the middle section of the board and kept flat against the board with glue Label Assembly as Rev 1.1 Note to Sub-Contractors: Modify all WIP of AO2 cards and all stock of the current revision of AIO2_V5 PCB-s Note to Fairlight Production: Modify all WIP of AO2_V5 Cards
MFX 283	ESP-AO2		**1**	**1.1**	15-Feb-99	Analog O/P Card	Mario Paolino		1. Improvement in Audio O/P SNR for channels 2 and 4 2. Reduction of Audio clicks when synchronisation sources change and while MFX3 system is in Armed condition. 3. Ability to calibrate for both +22 and +24 dBu and maintain low THD figures	1. Replace Capacitor CCD1562 (220pF) with CCD3004 (330pF) in location C204 2. Assembly Revision is Rev 1.1 Note to Subcontractors: Modify all WIP of AO2_V5 Cards Note to Fairlight Production: Modify all WIP of AIO2_V5 Cards
MFX 288	ESP-AO2		**1.1**	**1.2**	16-Mar-99	Analog O/P Card	George Potkonyak		Damp clock signals to ensure >= 100dB SNR at +24dBu reference. The cards should have an SNR of >99.5dB at +22dBu reference	1. Change 2 Resistor values in locations R173 and R174 from 33 Ohm to 56 Ohm. 2. Change 4 Network Resistor values in locations U52, U54, U55 and U56 from 33 Ohm to 100 Ohm. 3. Remove 1 Capacitor in location C204. 4. Labels PCB assembly as Rev. 1.2 Note to Subcontractors: Modify all WIP. Note to Production: Modify all WIP.
MFX 291.1	ESP-AO2		**1.2**	**1.3**	14-Apr-99	Analog O/P Card	George Potkonyak	THIS ECN IS CORRECTION TO ECN # 291	Improve SNR to achieve a minimum of 100 dB output level.	1. Fit multilayer ceramic SMD 0603 capacitor, 68 pF, >/= 50V, +/- 20% or better (Fairlight part # CCD1180), between U39/pin1 and R173 pad away from the C204. 2. Change Card revision to Rev. 1.3 Note to Production: Modify all WIP of Rev. 1.2 cards and relabel to Rev. 1.3 Note to Subcontractors: Modify all WIP of Rev. 1.2 cards and relabel to Rev. 1.3 Note to Field Service: Modify all Rev. 1.2 cards and relabel to Rev. 1.3
MFX 293	ESP-AIO2 ESP-AO2		**1.4** **1.3**	**6.0** **6.0**	22-Apr-99	Analog IO Card and Analog O/P Card	George Potkonyak	INTRODUCTION OF REVISION 6 BLANK PCB	To eliminatet modification to the Rev. 1 AIO_V5 Card	1. Numer of tracks re-routed and a pad for Capacitor C205 added. 2. PCB Revision changed to Rev.6 (ESP-AIO2_R6)
MFX 294.1	ESP-AO2		**6**	**6.1**	27-Apr-99	Analog O/P Card	George Potkonyak	THE TRACK CUTTING AND WIRE LINK MODIFICATION SPECIFIED IN THIS ECN NEED NOT BE DONE TO REV. 1.3 CARDS. THIS ECN REPLACES ECN # 294.	Improve SNR to achieve a minimum of 97 dB output level on all channels at all sampling rates. To eliminate the "Muting" problem.	1. A multilayer ceramic capacitor added, SMD 0603, 68 pF, >/= 50V, +/- 20% or better (Fairlight part # CCD1180), in location C205 on PCB Rev. 6. 2. Cut track near U2/pin 7 (under U2) as shown on sheets 1 and 2 of the ECN attachment. 3. Cut track near U55/pin 4 as shown on sheets 1 and 3 of the ECN attachment. 4. Add wire link between U2/pin 7 and U55/pin 4, routed as shown on the sheet 4 of the ECN attachment. Glue wire link to PCB at approx. 20 mm intervals. 5. XILINX program in U53 changed to AIOX10.JED, with Checksums: 14B4 for JED File and xxxx for JTAG File. New Assembly Revision is Rev. 6.1 NOTE TO SUBCONTRACTORS: Modify all WIP
MFX 296	ESP-AO2		**1.3** **1.4**	**1.4** **1.5**	27-Apr-99	Analog O/P Card	George Potkonyak		To eliminate the "Muting" problem.	1. XILINX program in U53 changed to AIOX10.JED, with Checksums: 14B4 for JED File and 0x5752 for JTAG File. 2. Card revision raisd to Rev. 1.4 NOTE TO PRODUCTION: Reprogram U53 on all Cards in WIP. Relabel the U53 accordingly. Relabel Card assembly to Rev. 1.4 If SNR at 48 MHz sampling rate is below 97 dB, modify card as per ECN294.1, Items 2,3 and 4 and relabel card to Rev. 1.5 NOTE TO FIELD SERVICE: Reprogram U53 on all Cards in WIP. Relabel the U53 accordingly. Relabel Card assembly to Rev. 1.4 If SNR at 48 MHz sampling rate is below 97 dB, return card to Fairlight for modification

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ECNs for AO Card as at 11/6/99

ECN Number	Assembly	New Assembly	Current Rev	New Rev	Date	Description	Name	Special Note	Reason	Details
MFX 301	ESP-AO2-A		**1.5** **6.1**	**1.5** **6.1**	04-May-99	Analog O/P Card (+15, 16 & 18 dBu)	George Potkonyak	THIS ECN INTRODUCES A NEW VERSION OF AO2 CARD +15, 16 & 18 dBu INPUT CLIPPING LEVEL. MINIMUM ACCEPTABLE SNR FOR THIS MODIFICATION IS 96 dB FOR ALL SAMPLING RATES, EXCEPT 32 MHz, FOR WHICH IT IS 85 dB MINIMUM.	To create a +15, 16 or 18 dBu input clipping level card from a +22 dBu input clipping level card.	1. Re-connect the mod wires from Pin 5 to Pin 6 on four IC-s (SSM2143) U23, U24, U25 and U26. THIS MOD IS APPLICABLE ONLY TO REV 1.5 CARDS (not to Rev 6.1) 2. Lift Pins 1 and 5 on four IC-s (SSM2143) U23, U24, U25 and U26 and connect a resistor between each lifted pin and its pad. Use the following Resistor: 5k6, SMD 0805, Metal Film, 1% (Fairlight Part Number RME9206). THIS MOD IS APPLICABLE TO BOTH REVISIONS (1.5 and 6.1) 3. Card revisions remain unchanged (Rev. 1.5 or Rev. 6.1), however, the card part number changes to ESP-AO2-A NOTE TO PRODUCTION: If there is a need to modify the card to +15, 16 or 18 dBu level, the card is to be labeled with a new part number ESP-AO2-A. Revision level remains the same. NOTE TO FIELD SERVICE: Do not modify cards in the field. Request Fairlight, Sydney to supply the required stock. ADDITIONAL NOTE: ALL AO2 CARDS LABELED WITH ESP-AO2 (only) PART NUMBER ARE SET TO +22dBu.
MFX 303.1	ESP-AO2		**1.5** **6.1**	**1.6** **6.2**	07-May-99	Analog O/P Card	George Potkonyak	THIS ECN REPLACES ECN # 303.	To eliminae or reduce the chance of some capacitors exploding on power-up.	1. Replace two 47uF capacitors in locations C155 and C156 (which are 20V rated) with two capacitors: 22uF, Tantalum, Low ESR, SMD E-Case, 35V (Fairlight Part No. CTD9108) 2. Replace five 100uF capacitors in locations C159, C160, C161, C162 and C176 (which are 16V rated) with five capacitors: 33uF, Tantalum, Low ESR, SMD E-Case, 25V (Fairlight Part No. CTD2330) 3. Replace three 100uF capacitors in locations C163, C164 and C177 (which are 10V rated) with three capacitors: 100uF, Tantalum, Low ESR, SMD E-Case, 16V (Fairlight Part No. CTD6298 - which were taken out of C159, C160, C161, C162 and C176). 4. Card revision raisd from Rev.1.5 to Rev. 1.6 and from Rev. 6.1 to Rev. 6.2 NOTE TO PRODUCTION: Modify all Cards in WIP. Re-label Revision accordingly. NOTE TO FIELD SERVICE: Modify all Cards in service. Re-label Revision accordingly.
MFX 304	ESP-AIO2 ESP-AO2		**6.2** **6.2**	**7.0** **7.0**	19-May-99	Analog IO Card and Analog O/P Card	George Potkonyak	INTRODUCTION OF REVISION 7 BLANK PCB	To enable setting to 12 to 24 dBu using trimpots	1. Rev. 7 PCB introduced 2. IC-s in locations U7, U8, U9 and U10 changed to OPA2064AU (Fairlight Part No. SAS7843) 3. U62 and U63, OPA2134 (same as in locations U46-U41) added (Fairlight Part No. SAS3907) 4. Trim Pot values in locations R65, R66, R67 abd R68 changed to 500R Multiturn, 3224J Series, SMD (Fairlight Part No. RPT2337) 5. Resistor values in locations R75, R77, R79 and R81chnaged to 820R, Thick Film, 0.1W, 1% SMD0805 (Fairlight Part No. RME7459) 6. Link (0R0 Resistor, Fairlight Part No. RME0001) in location JP3 removed 7. Pads for Links (0R0 Resistor, Metal Film, >= 0.125W, 1%, SMD0805, Fairlight Part No. RME0001) in locations JP9, JP12, JP13, JP28 and JP29 added. Final configuration to be detrmined on test. 8. Pin Header pads in locations JP24, JP25, JP26 and JP27 added for future use. Link to be fitted between pins 1 and 2 only for 15 dBu set-up. 9. C206, C207, C208 Pads added - NOT to be populated 10. Card revision raised to Rev. 7.0
MFX 307	ESP-AIO2 ESP-AO2		**7**	**7.1**	03-May-99	Analog IO Card and Analog O/P Card	George Potkonyak	DRAFT	xxxxxxxxxx	1. Replace two 68pF capacitors in locations C204 and C205 with two capacitors 33pF Multi Layer Ceramic (Fairlight Part No. CCD3997) 2. Add resistor 33R (Fairlight Part No. RME5033) at location R186 3. Add resistor 0R (Fairlight Part No. RME001) at location R179, R180, R187 4. Add capacitor 100nF Multi Layer Ceramic (Fairlight Part No. CCE4356) at locations C212, C213, C214, C215, C216 and C211 5. Replace two inductors in locations L3 and L4 with Chip Inductor 22uH (Fairlight Part No. TCS0668) 6.Card revision is raised from Rev7.0 to Rev 7.1 7. NOTE TO PRODUCTION: Modify all Cards in WIP and Re-label Revision accordingly 8. NOTE TO SERVICE: Modify all Cards in Service and Re-label Revision accordingly

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ECNs for AMB24 Card as at 11/6/99

ECN Number	Assembly	New Assembly	Current Rev	New Rev	Date	Description	Name	Special Note	Reason	Details
MFX 68	AMB24		**1**	**1.1**	22-Dec-94	Analog Mother Board (24 Channel)	Chris Alfred		Fitment of extra brace to provide extra rigidity to the Mother Board.	Please see attached drawings identifying location and alignment of Brace to the Mother Board. The Brace has to be mounted on the solder side.
MFX 73	AMB24		**1.1**	**1.1**	16-Jan-95	Analog Mother Board 24 Channels	Chris Alfred		Voltage drop across the 10A Fuse requires that the fuse be eliminated from the mother-board	Do not mount fuse-holder and connect +5V to TP6 instead of TP1.
MFX 267.1	ESP-AMB24		**2.0** **1.0**	**2.1** **1.1**	28-Jan-99	AMB24 ANALOG MOTHERBOARD	George Potkonyak		To reduce the system level of noise.	1. Prepare a red PVC insulated cable, 112 conductors of 0.25 mm diameter (5.20 mm nominal diameter), by cutting it to 585 mm length and stripping each end. Crimp a Lug, Fairlight part # CONG8152 to one end of cable. 2. Similarly, prepare a black PVC insulated cable, of the same size, cut to 610 mm length. 3. Solder the stripped end of the red cable across pins 77 and 78 on the connector CN6 on the solder side. 4. Solder the stripped end of the black cable across pins 59 and 60 on the connector CN6 on the solder side. Note: Cables to be routed in the direction of the existing cables, towards the connector CN1. 5. Label the motherboard as Rev. 2.1 or Rev. 1.1 accordingly Note to Production: All WIP to be modified. Note to Subcontractors: All WIP not yet installed into chassis to be modified.

ECNs for AMB8 Card as at 11/6/99

ECN Number	Assembly	New Assembly	Current Rev	New Rev	Date	Description	Name	Special Note	Reason	Details
MFX 61	AMB8		**1**	**1.1**	08-Dec-94	Analog Mother Board (8 Channel)	Chris Alfred		Fitment of extra brace to provide extra rigidity to the Mother Board.	Please see attached drawings identifying location and alignment of Brace to the Mother Board. The Brace has to be mounted on the solder side.
MFX 62	ESP-AMB8		**1.1**	**1.2**	13-Dec-94	Analog Mother Board (8 Channel)	Chris Alfred		The edge-connectors on the Analog Mother Board need to be raised to ensure an adequate mechanical connection with the plug-in cards. Placement of Fibre Insulator strips underneath the card-edge connectors overcomes this.	Place TWO Fibre Insulator strips under EACH Connector before soldering connector to Mother-Board. Make sure that the Connector is pushed down firmly while soldering so that the insulator strips are held in tightly. Part No. GENM300/005B, Insulator Strip 34 Way, Qty X 4 Part No. GENM300/005C, Insulator Strip 48 Way, Qty X 2

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ECNs for CG4 Card as at 11/6/99

ECN Number	Assembly	New Assembly	Current Rev	New Rev	Date	Description	Name	Special Note	Reason	Details
MFX 162.1	ESP-CG4		**3**	**3.1**	05-Nov-96	Colour Graphics 4 and Mixer Card	Erik de Castro Lopo		Fix for missing PCB tracks. First production version of ESP-CG4.	1. Program the 22v10 GALs at locations U16 and U17 with the file CG4OUT01.JED. 2. Program another 22v10 GAL with the file CG4FIX00.JED and piggy back it on top of U17 connecting pins 1, 12 and 24 to the corresponding pins of U17. The other pins of the piggy-backed GAL should be cut short enough to prevent shorting out the pins on the GAL below it. Call the piggy-backed GAL Ux. 3. Connect a wire from the via connected to U20/19 to Ux/5. 4. Connect a wire from TP9 (connected to U3/44) to Ux/6. 5. Connect a wire from the via connected to U3/50 to Ux/7. 6. Connect a wire from the via between U20/10 and negative terminal of C18 to Ux/8. 7. Connect a wire from TP6 (circled in white and connected to U3/103) to Ux/9. 8. Connect a wire from U19/19 to Ux/16. 9. Connect a wire from U21/19 to Ux/17. 10. Connect a wire from U15/24 to Ux/18. (When finding the pin numbers for U14 and U15, the 32 pin PCB overlay should be used as a reference, not the 28 pin IC.) 11. Connect a wire from U14/29 to Ux/19. (When finding the pin numbers for U14 and U15, the 32 pin PCB overlay should be used as a reference, not the 28 pin IC.) 12. Connect a wire from U15/29 to Ux/20. (When finding the pin numbers for U14 and U15, the 32 pin PCB overlay should be used as a reference, not the 28 pin IC.) 13. Ensure pin 1 of the Crystal Oscillator Module at X1 is closest to C6 and not as per the PCB overlay. 14. Pin 1 of both JP1 and JP2 to be on the solder side only. 15. Label the card Rev 3.1 Change : The programme file for U16 and U17 changed from CG4OUT00.JED to CG4OUT01.JED.
MFX 163	ESP-CG4		**3.1**	**3.2**	04-Nov-96	Colour Graphics and Mixer Card	Erik de Castro Lopo		To allow for implemention of modifications to interrupt levels.	1. Connect a wire from the via connected to U2/59 to TP10 (connected to U3/76). 2. Reprogram the CG4 2064 Lattice devices using upload file WXCG2.DLD. 3. Label the PCB as REV. 3.2
MFX 170.1	ESP-CG4		**3.2**	**3.3**	06-May-97	Colour Graphics and Mixer Card	Erik de Castro Lopo	Immediate implementaion	To allow for operation of High Speed Serial Link (HSSL) (Mixer Interface) for cables longer than 10 Metres.	1. Short out R3. 2. Install an 1 x 8 SIL Header (Fairlight P/N CONG5272-8) at RN2. 3. Install 4 shorting plugs (Fairlight P/N COND6747) on header above at RN2 1-2, RN2 3-4, RN2 5-6, RN2 7-8. 4. Use WXCG3.DLD program to load CG4 Lattice devices. Changes: Installed header at RN2 with shorting plugs instead of simply shorting out PCB pads.
MFX 172	CAB5068				11-Dec-96	Cable Assy 14R CG4 - RGB01	Leith Stewart		There is not enough excess length to allow easy assembly.	1. New specifications for the following cable have been released; CAB5068 - CABLE ASSY 14R CG4 - RGB01 Rev 1.1 2. All further purchases of this item must be to the new specification. 3. Use all old stock from wharehouse before implementing the new specification cable.
MFX 177.2	ESP-CG4		**3.3**	**3.4**	21-Feb-97	Colour Graphics 4 and Mixer Card	Erik de Castro Lopo		Improve reliability of communication between MFX3 and FAME mixing console via the HSSL.	1. Cut the solder side track connected to U22/1. 2. Note : All added components (ie resistors and capacitors) in the following steps must be placed physically within the boundary of the PCB. 3. Connect a 47pF capacitor in series with a 47R resistor between U22/1 to U22/7 on the solder side. Parts required; Fairlight P/N PCCC2564/2 - CAP CERM 47PF 50V 5MM SPACING [2N7] or PCCC2564 - CAP CERAMIC 47pF 50V .1" [2N7] RESR1009 - RES 47R 0W4 MR25 1% [2E3] 4. Connect a 47pF capacitor in series with a 47R resistor between U22/15 to U22/14 on the solder side. 5. Connect a 47pF capacitor in series with a 47R resistor between U23/1 to U23/7 on the solder side. 6. Connect a 47pF capacitor in series with a 47R resistor between U23/15 to U23/14 on the solder side. 7. Connect a mod wire from U24/7 to TP28 (connected to U2/71). 8. Connect a mod wire from TP29 (connected to U2/78) to U22/1. 9. Reprogram the CG4 2064 Lattice devices using upload file WXCG4.DLD.
MFX 181	ESP-CG4		**3.4**	**3.5**	04-Feb-97	Colour Graphics 4 and Mixer Card	CHRIS ALFRED		Invert XMTCLK signal from ESP-CG4 on high speed serial link cable to fix design error.	1.,Cut solder side track to JP2/17 (26 way IDC) ,(Pin 1 of connector JP2 is on the solder side nearest JP1 20 way IDC). 2.,Connect JP2/17 to RN6/2. 3.,Cut component side track to JP2/16. 4.,Connect JP2/16 to RN6/4.
MFX 217	ESP-CG4		**3.5, 4.0**	**3.6, 4.0**	12-Aug-97	Colour Graphics 4 and Mixer Card	Erik de Castro Lopo		Texas Instruments IC 26LS31 found to be unreliable (HSSL dropping bytes).	IC 26LS31 at location U27 must be manufactured either by Philips or by National Semiconductor only.

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ECNs for CG4 Card as at 11/6/99

ECN Number	Assembly	New Assembly	Current Rev	New Rev	Date	Description	Name	Special Note	Reason	Details
MFX 258	ESP-CG4		**4**	**4.1**	26-Aug-98	Colour Graphics 4 and Mixer Card	Mario Paolino	Production Only Field Action: None WIP Action: None	Cost Reduction measure: Parts only required on CG4's used in Fame UG have been removed. These parts will be added to the Fame UG BOM	1. Delete from BOM SIGB1025 Ic HCPL2630 x 3 2. Delete from BOM SIGB00251/30 Ic CY6C421-30 x 2 3. Add to BOM ICSD7008 IC Socket 8 Pin machine pin 0.3" x 3 4. Add to BOM ICSD7028S IC Socket 28 Pin machine pin 0.3" x 2 5. Change Card revision as detailed above
MFX 268	ESP-CG4		**4.1**	**4.2**	06-Oct-98	CG4 CARD	Erik de Castro Lopo		Reboot Problem on Fame Installations.	1. New WXMIXR Lattice Source wxcgpc9.zip Note to Production: Load new WXMIXR Lattice Program to all units in WIP as per instruction contained in wxcgpc9.zip. Re-label CG4 cards to Rev. 4.2 Note to Subcontractors: Load new WXMIXR Lattice Program to all WIP units as per instruction contained in wxcgpc9.zip. Re-label CG4 Cards to Rev. 4.2 Note to Service: Load new WXMIXR Lattice Program to all Fame installations as per instruction contained in wxcgpc9.zip. Re-label CG4 cards to Rev. 4.2
MFX 285	ESP-CG4		**4.2**	**4.3**	04-Mar-99	Colour Graphics card	Mario Paolino		Introduction of the RIO Rev 3.0 card has altered the inrush current requirements of the fuse on the CG4.	1. Remove the fuse (Fairlight Pt No FUSG5317A) 1A Quick Blow. 2. Replace with fuse (Fairlight Pt No FUSG5338) 1A Antisurge. Change Assembly Revision as detailed above. Note to Production: Modify all existing WIP Note to Subcontractors: Modify all WIP of ESP-CG4 Cards
MFX 305	ESP-CG4		**4.3**	**4.4**	27-May-99	Colour Graphics 4 and Mixer Card	Mario Paolino		Reversal of ECN 258 To maintain compatability of the ESP-CG4 between the MFX and Fame systems, the parts removed by ECN 258 as a cost reduction measure have been re-installed by ECN 305	1. ADD three IC HCPL2630 at locations U24 U25 U26 (Fairlight Pn: SIGB1025) 2. ADD two IC CY7C421-30 at locations U22 U23 (Fairlight Pn: SISB00251/30) Card revision is raised to 4.4 NOTE TO SERVICE: Update all spares stock NOTE TO PRODUCTION: Update all WIP NOTE TO ASSEMBLER: Update all WIP

ECN Number	Assembly	New Assembly	Current Rev	New Rev	Date	Description	Name	Special Note	Reason	Details
MFX 3	ESP-DCC		**1**	**1.1**	28-Apr-94	Digital Channel Card	Chris Alfred		Prevent incorrect clocking of DCCIRAM GAL causing IRAM errors.	220R resistor between U17/13 and Vcc 330R resistor between U17/13 and GND
MFX 23	ESP-DCC		**1.1**	**1.2**	26-Jul-94	Digital Channel Card	Chris Alfred		Remove capactive termination on FS256 which causes false clocking on FSYNC.	Connect both pins of C17 together. Connect both pins of C21 together.
MFX 27.1	ESP-DCC		**1.2**	**1.3**	22-Nov-94	Digital Channel Card	Chris Alfred		Change Note 28 requires that Sockets are NOT required on locations U29 and U32 The Revision numbers have also been corrected.	Do NOT place sockets on locations U29 and U32 (both 74FCT841)
MFX 28.1	ESP-DCC		**1.3**	**1.4**	22-Nov-94	Digital Channel Card	Chris Alfred	Changes in Rev. No.	Stop clicking on playback due to addressing errors caused by noise on WRAM accesses during background reads.	Change DCCWRAM gal at U70 to DCCWRAM2. Change U29 to 74FCT2841. Change U32 to 74FCT2841. Change U90 to 74FCT2827. Change U91 to 74FCT2827. For production, it should not be necessary for sockets to be installed for U29,U32,U90,U91.
MFX 35	ESP-DCC		**1.4**	**No change**	19-Oct-94	Digital Channel Card	Chris Alfred		Terminate RS422 signals from DIO card to stop noise when neither the DCC nor the DIO are driving the signals causing the DCC to malfunction. The signals are undriven during the transition of Sync between HOUSE and INPUT.	Change note withdrawn due to software fix in Rev 12.0.23
MFX 58	ESP-DCC		**1.4**	**1.5**	29-Nov-94	Digital Channel Card	Chris Alfred		Stop audio clicking when ESP-DCC to ESP-DIO 26way cables are close to each other due to noise induction.	Short-out capacitors C18,C19,C20,C22,C23,C24. C17 and C21 were shorted-out in change note 23. Capacitors C17,C18,C19,C20,C21,C22,C23,C24 do not need to be installed.
MFX 136	ESP-DCC	ESP-MX1	**1.5**		14-Mar-96	FAME Mixer Card	Andrew Bell		FAME will require the introduction of a new variant on the DCC, containing no waveform RAM. This card will be known as MX1, and is used only for mixing digital audio signals in the FAME system. Up to 2 of these cards will be fitted to FAME systems, in addition to the DCCs used to play disk tracks. MX1 will have no application in normal MFX3 systems.	The ESP-MX1 card is made by deleting the following parts from an ESP-DCC card. 1. U39,U40,U47,U48,U54,U55,U61,U62,U68,U69,U75,U76,U81,U82,U88,U89 441024Z-70 2. U90, U91 74FCT2827 3. U63, U77 74FCT245 4. U56, U83 74FCT652 5. U29, U32 74FCT2841 6. U70 GAL16V8 (DCCWRAM) 7. U43 74FCT157 8. RN10 47R 8 pin 9. RN11 33R 8 pin
MFX 195.2	ESP-DCC4, ESP-DCC6, ESP-MX1				26-May-97	Digital Channel Card / FAME Mixer Card	NOEL PLUMMER		Withdrawal of alternatives for the 74AC646.	ECNs 195 and 195.1 are hereby withdrawn as there was found to be problems with the alternative ICs after more extensive testing. Changes: 195.1 Another 5 alternatives added. Changes: 195.2 Total withdrawal of ECNs 195 and 195.1
MFX 207.3	ESP-DCC4, ESP-DCC6, ESP-MX1		**1.5**	**1.6**	09-Jul-98	Digital Channel Card / FAME Mixer Card	Noel Plummer		The height of the jumper headers and jumpers (shunts) is causing interference problems with adjacent cards.	1. Change jumper plug from COND6747 to COND6747L, which has been defined as: Connector shorting plug (2 pin jumper, shunt), open body, gold >= 10u", maximum height 6.5mm "AMP (142270-5), e-cam (283-11-2X or 283-11-3X or 283-11-4X), Method (960F-202-35), Molex (90059-0009), Nextron (281-11-60 or 281-11-2X or 281-11-3X)" Avnet, Interconnections, Adilam, Amtron 2. Header 6 x 2, Fairlight P/N CONG5233-6 has been changed to CONG5624-6 which has been defined as: Connector Header 6 x 2 (stick header), Select Gold >= 10u", Max height above PCB = 8.7 mm, Total Pin length = 11.3 + 0.5, -1.1 mm U.L. Recognised, non-critical, AMP (103186-6), e-cam (206-030-012-107 or 206-060-012-107), Methode (910F-1-206-02) Suppliers = AMP, Amtron, Adilam 3. Header 9 x 2, Fairlight P/N CONG5233-9 changed to CONG5624-9 which has been defined as: Connector Header 9 X 2 (stick header), Select Gold >= 10u", Max height above PCB = 8.7 mm, Total Pin length = 11.3 + 0.5, -1.1 mm U.L. Recognised, non-critical, AMP (103186-9), e-cam (206-030-018-107 or 206-060-018-107), Methode (910F-1-209-02) Suppliers = AMP, Amtron, Adilam 4. Replaced header 2 pin P/N CONG5266 with CONG5266L: Connector 2 Pin Header, Select Gold >= 10u", Max height above PCB = 8.7 mm, Total Pin length = 11.3 + 0.5, -1.1 mm U.L. Recognised, non-critical, AMP (103186-1), e-cam (205-030-002-107 or 205-060-002-107), Methode (910F-1-102-02), Molex (22-28-4023) AMP, Amtron, Adilam, Utilux Changes 207.1: Redefinition of CONG5233-6 and CONG5233-9 withdrawn and replaced by new part numbers CONG5624-6 and CONG5624-9. Additional parts options added. 207.2 Expanded the range of headers by adding AMP and Methode brands. 207.3 Changed pin length tolerance

ECNs for DCC Card as at 11/6/99

ECN Number	Assembly	New Assembly	Current Rev	New Rev	Date	Description	Name	Special Note	Reason	Details
MFX 252.1	ESP-DCC6, DCC8, ESP-MX1		**1.6**	**1.7**	24-Aug-98	Digital Channel Card	Mario Paolino	Amendment to ECN 252	GAL 16V8C-7LP at location U46 & U53 causes audio click problems	1. Replace GAL 16V8C-7LP at location U46 & U53 with GAL 16V8B-7LP i.e. this GAL must be a "B" version 2. Change assembly revision as detailed above Special Note: All DCC's produced since 17/4/98 have a "B" GAL at location U46 and all DCC's produced since 4/8/98 have a "B" GAL at location U53
MFX 263.1	ESP-DCC4, DCC6, DCC8, ESP-MX1		**1.7**	**1.8**	20-Nov-98	Digital Channel Card and MX1 Card	Noel Plummer	Note it not necessary to modify successfully working cards modified under the previous release (263) of this ECN.	To facilitate easier adjustment of the PLL VCO bias voltage. It has been found that the variable cap can be difficult to adjust. By using precision frequency setting components in the VCO circuitry, the value of the variable cap C13 can be substantially reduced. The full turn adjustment range will then be from about 1.2 to 3.0 Volts. In addition, it is anticipated that the temperature and mechanical stability of this adjustment will be improved.	Replace variable capacitor C13 with a 4.2 - 20p, 450 +/- 300 ppm/degree C, Vertical, two hole, (Pink), Fairlight P/N CAT2415, Murata P/N TZ03T200ER169. Very Important - Mask PCB holes for this component, wave and wash the PCB before installing and hand soldering this component. Replace C12 with Ceramic 39p, NPO 0 +/- 60 ppm/degree C, 5%, 50V, Fairlight P/N PCCC2544, Murata P/N DD104-989CH390J50. Replace L2 with Inductor 0.15uH, 2% , 1.27 A, 0.07 ohm, Q >= 45, SRF >= 420 MHz, Fairlight P/N TCA2430 (specially selected) Replace C25 with a varactor Diode BB809, Fairlight P/N SDTD5040, cathode closest to U23 (same as D2). Change Assembly Revision on PCB Label to 1.8. Instructions to Sub-Contractor: Modify all WIP as per above. Instructions to Production: Modify all WIP as per above when parts become available. Instructions to Service: Implement where needed. Changes: 263.1 Changed variable cap to 4 - 20 pF and 0.15 uH inductor to tighter tolerance.
MFX 264	DCC8		**1.7**	**2**	21-Sep-98	Digital Channel Card	Noel Plummer	All variations of the ESP-DCC card: DCC8, DCC6, MX1, will now be rationalised to DCC8 only, to simplify manufacture and inventory.	The ESP-DCC PCB has been redesigned. The new PCB is revision 2. It incorporates all mods up to 1.7, therefore assembly revision 2.0 is equivalent to assembly revision 1.7 On the rev 1 cards, the variable cap at 6.8 to 45pF, was often difficult to adjust. By using precision frequency setting components in the VCO circuitry, the value of the variable cap C13 can be substantially reduced. Provision has been made, on this new layout, to use 1% silver mica caps and a 11 turn tuneable inductor, if necessary. A cut-out of almost 3" has been inserted in the main edge connector, to reduce insertion and extraction force of the PCB, into the Digital Mother Board, by about 36%.	New Revision ESP-DCC Blank PCB - Rev 2 Fairlight P/N PWAEESPDCCR2 Install a BB809 Varactor Diode (varicap) at C25 orientated the same as D2 (cathode closest to C16). The new PCB features the following enhancements: New GAL (U35) and LED (LD1) added to indicate PLL out of lock. Incorporated mods from rev 1 (2 resistors added, 8 caps removed). Layout changed so that a right angled variable cap can be installed. Variable cap positioned so adjustment possible without extender card. Enlarged variable cap hole diameter from 1 mm to 1.3 mm. Increased pad to track clearance on solder side to improve reliability. All pads and vias teardropped for improved reliability. All jumpers pre-linked, on bottom layer.
MFX 271.3	DCC8		**2**	**2.1**	04-Dec-98	Digital Channel Card	Noel Plummer		The value of the fixed capacitor in the PLL circuit needs to be changed slightly to correctly set the range of the trimmer cap C13. The output enable pin of the PLCK GAL at U35 needs to be grounded to facilitate using the GAL in latched mode. The PLCK GAL has been updated to enable the PLL lock indicator LED to completely turn off when the circuit is in lock. (Note that the LED will only light on power up or if a fault develops taking the PLL out of lock). Removal of unused headers.	Remove C12 and C27. Replace C12 with a 33pF 2% Silver Mica Cap from Cornell Dubilier P/N CD5EC330G03. (Some production prototypes were fitted with a 15p and 18p Silver Mica at C12 and C27). Rev 2 blank PCBs (12 only made) require a modification wire on the solder side between U35 pin 10 and pin 11. Rev 2A blank PCBs will come with pin 11 grounded and so do not require the mod wire. Change PLCK GAL at U35 to PLCK2. Change TGEN2 GAL at U60 back to TGEN. TGEN2 caused a problem with machine operation. Note that no cards should have left the factory with TGEN2 installed. Remove headers at JP2, JP3, JP4, JP5, JP6, JP7 and JP8. Change assembly revision to 2.1 Change history to this ECN: 271.1 Incorrect reference to U36, changed to U35. PLCK GAL name corrected. 271.2 TGEN GAL restored back to original program and PLCK GAL changed instead. 271.3 Mod wire on U35 restricted to rev 2 PCBs. Reference made to reversal of TGEN GAL in body of this ECN.
MFX 272.1	DCC8		**2**	**2A**	04-Dec-98	Digital Channel Card Blank PCB	Noel Plummer		The ESP-DCC Rev 2 blank PCB has been slightly modified. The new PCB is revision 2A. Pin 11 of U35 has been grounded by thermal relief to the ground plane. (Note this means it is unnecessary to connect a mod wire as detailed in ECN 271, between pins 10 & 11 of U35). Capacitors footprints at C12, C27, C28 and C25 had four holes to accommodate various pitches. One hole for each cap has been removed to eliminate the possibility of a solder bridge being created during wave soldering.	New Revision ESP-DCC Blank PCB - Rev 2A Fairlight P/N PWAEESPDCCR2A Change history of this ECN: 272.1 Incorrect references to U36 corrected - changed to U35.

ECN Number	Assembly	New Assembly	Current Rev	New Rev	Date	Description	Name	Special Note	Reason	Details
MFX 9	ESP-DIO		**3**	**3.1**	28-Apr-94	Digital IO Card	Chris Alfred			DUART communications Connect U19/13 to U10/21 (68681FN) Connect U19/11 to U10/20 Cut solder side track to U26/12 (3486) Connect U26/12 to U26/8 *XIRQ to PA7 *XIRQ to PA7 Connect U10/18 to U10/27 (68HC11) *INDET analog input detect Cut solder side track to U10/31 on side nearest U6 Connect CN6/21 to U10/22 RESET Connect 1N4148 in parallel with R29, cathode to end nearest C22 (Vcc). EPROM Install Eprom BOOT V3.3 at U12 (27C512) PALS Install TEST2 pals at U14,U17
MFX 18	ESP-DIO		**3.1**	**3.2**	15-Jul-94	Digital IO Card	Chris Alfred		New DIO software. Required for software revisions 12.0.08 and higher. Must be done in conjunction with Change Note 19.	Change 27C512 eprom at U12 to BOOT V4.0.3.
MFX 21.1	ESP-DIO		**3.2**	**3.3**	28-Nov-94	Digital IO Card	Chris Alfred		Improve audio quality. Test clock signals to CLKGEN pal modulate WCLK output. Once this modification has been done, the diagnostic test clock signals (TWCLK and T256FS) cant be selected as the sample clocks. The clocks from the ESP-SYN (via the ESP-DCC and TSB cable) must be used. This change note must be done in conjunction with Change Note 20.	Cut component side tracks to pins 3 and 4 of U22 (CLKGEN pal). Ensure jumpers JP1 and JP2 are installed.
MFX 32.1	ESP-DIO		**3.3**	**3.4**	28-Oct-94	Digital IO Card	Chris Alfred	This change to be carried out in conjunction with change note 42 on ESP-AIO assembly.	Improve noise figures at 48kHz to bring them inline with 44k1. Make noise figures similar for channels 1,2 and 3,4. Remove clicking at 48KHz when not using National Semiconductor Ics 3486 and 3487. Remove clicking at 48khz Digital inputs 3 and 4 (Change detail No. 8 only). Cards are deemed to be acceptable if 48kHz,44.1kHz and 44.056kHz produce 87dB SNR and 0.01% THD when in system (22-22K).	Cut and remove bottom half of pin 13 on U31 (IC 3486). Leave On Delay Line bel A447-0250-10, cut all pins (except 7 and 14) Piggy-back the delay line on U31 (3486) connecting delay/14 to U31/16, and delay/7 to U31/8. Connect delay/13 to empty plate thru hole beneath U31/13. Connect U31/13(IC 3486 shortened leg) to Delay/1. On solder side, connect 47pF capacitor across U31/13 and U31/14 as On solder side, connect 100pF capacitor across U28/3 and U28/7. On solder side, connect 150pf capacitor across U11/8 and U11/12.
MFX 48.1	ESP-DIO				28-Nov-94	Digital IO Card	Chris Alfred		Terminate FS256 and FSYNC.	Change note deleted.
MFX 57	ESP-DIO		**3.4**	**3.5**	28-Nov-94	Digital IO Card	Chris Alfred		Clicking on channels 3,4 at 48k fixed in software revision 12.0.27. This change note reverses Detail 8 of Change note 32A.	Remove 150pF modification capacitor connected to U11/12. Some ESP-DIO cards were released with the capacitor connected to U29/6 - this capacitor should be removed.
MFX 60	ESP-DIO		**3.5**	**3.6**	06-Dec-94	Digital IO Card	Chris Alfred		Fix SPDIF input.	Remove resistors R2,R4,R17,R18.
MFX 64.1	ESP-DIO		**3.7**	**3.6**	16-Mar-95	Digital IO Card	Chris Alfred			Change Note No. 64 withdrawn and PCB reverted to previous Revision Number.
MFX 89	ESP-DIO		**3.6**	**3.7**	10-Apr-95	Digital IO Card	Chris Alfred		Stop MSN/WSN and TSB errors when on INPUT sync. The 256Fs clocks from the AES decoders is delayed and widened.	Disconnect and remove the delay line piggy-backed onto U31 (3486). Reconnect U31/13 to the PCB hole beneath it. Remove the 47pF capacitor connected on the solder side between U31/13 and U31/14. Ensure that 100pF capacitor across U28/3 and U28/7 on the solder side has been removed. Ensure that 150pF capacitor across U11/8 and U11/12 on the solder side has been removed. Cut component side track to U30/1 (3487). The track exits U30 between pins U30/15 and U30/16. Cut component side track to U30/15. Connect U18/19 (CS8411) to U6/10 (22V10 DIDECO pal). Connect U11/19 (CS8411) to U6/9. Connect U6/11 to U8/6 (74HC259). Connect U6/14 to U30/1. Connect U6/15 to U30/15. Change pal at U6 to DIDECO2.
MFX 93	ESP-DIO		**3.7**	**3.8**	12-May-95	Digital IO Card	Erik de Castro Lopo	This Change Note requires Change Note 65B to be performed on ESP-AIO.	Improves SNR of the AIOs by preventing audio frequency beating between the 12.288 MHz crystal on the ESP-DIO and the sampling rate clocks.	Change Y1 (12.288 MHz crystal) to 12.00 MHz. Label card as Rev 3.8.

ECNs for DIO Card as at 11/6/99

ECN Number	Assembly	New Assembly	Current Rev	New Rev	Date	Description	Name	Special Note	Reason	Details
MFX 96	ESP-DIO		**3.8**	**3.9**	16-May-95	Digital IO Card	Erik de Castro Lopo		Reinstates detail 3 of Change Note 64 which was erroneously removed with Change Note 64A.	Change gal at U22 to CLKGEN2. All pins to be placed in socket. Label card as Rev 3.9.
MFX 111	ESP-SYN		**2.8 3.0**	**2.9 3.1**	20-Oct-95	Fix DIO communications	Chris Alfred	Implementation of this is mandatory.	Communication errors to the DIO would cause the sytem to exit to the shell with 'Error #003 Interrupt key pressed' report. The communcation errors are due to a timing error when accessing the DUART on the ESP-SYN card. The error reports DIO status "J" timeout on TVTs on R&D machines.	1. Change DSACK pal at U41 to DSACK3. The pal MUST be 22V10-15. 2. Change IODEC pal at U69 to IODEC5. On Rev 2.8 leave pin 22 of the pal out of the socket. On Rev 3.0 leave pin 22 in the socket. 3. Disconnect modification wire between U28/10 (68681) and U41/3 (DSACK 22V10-15). This wire was added on ECN 46A. 4. Connect U28/10 to RN14/5 (4k7 10 pin resistor pack) and to U41/7. 5. Update revision of card.
MFX 126.4	PWBMESPDIO	PWBMESPDIO-E	**3.9**	**3.9**	15-Aug-97	Digital Input Output Card	Mario Paolino	Applicable to all machines with a requirement for EMC compliance. To be used in conjunction with ECN # 123, 124, 125 (or later revisions)	To modify the current DIO card to meet EMC requirements. The following changes are required as part of an overall system modification to make the MFX3 rack meet EMC requirements. It is important that this modification is carried out in conjunction with all other ECNs that outline EMC changes.	1. Viewing the board from the solder side with CN3 on the left, fit the following; Solder a wire (16/0.2 UL 1007) from the left hand mounting guide of CN4 to the right hand mounting guide of CN2. 2. Repeat this for CN2 to CN3. 3. Attach a solder tag CONG5204 Utilux H256 or RS #446-642 using the screw underneath the support block near CN3. Solder the other end to the left hand mounting guide on CN3. This is to ensure that all D connector metal shells have electrical continuity to the chassis. 4. VERY IMPORTANT Trim the mounting guides and arrange the wires so that they protrude NO higher than 1.5mm above the PCB surface. 5. When all modifications have been completed, the part number for the assembly becomes PWBMESPDIO-E. Changes: 126.2 Paragraph 2. Change on line 3 to show use of solder tag instead of crimp terminal. Paragraph 3 & 4 deleted, information now contained in ECN # 126.3 Paragraph 2. Change on line 3 giving correct RS part number. 126.4 Paragraph 1,2,3,4. Add Product Code for solder tag, Add detailed steps. Add mounting guide dimentions.
MFX 251	ESP-DIO-E, ESP-DO-E		**3.9**	**4**	23-Jul-98	Digital I/O and Digital Output Only Card	Noel Plummer		The ESP-DIO PCB has been redesigned. The new PCB is revision 4. Rev 4 PCB incorporates all mods (including EMC) up to 3.9 therefore assembly revision 4.0 is equivalent to assembly revision 3.9.	New Revision ESP-DIO Blank PCB - Rev 4 Fairlight P/N PWAEESPDIOR4 The new PCB features the following enhancements: Revised split power plane on pp2. Modified boundary keep out to match routing drawing. Corrected power ground expansion on 125 thou holes. Moved tracks away from four screw holes at corners to eliminate need for fibre washers. Increased clearance between pads and solder side tracks. Teardropping added to all pads for improved PCB reliability. Fairlight logo on silkscreen.
MFX 253.1	ESP-DIO-E & ESP-DO-E		**3.9**	**3.9**	08-Oct-98	DIO (EMC) CARD & DO (EMC) CARD	Noel Plummer		DIO detection failure with power cycled at 3 seconds OFF interval	UNITS IN WIP: Replace 74LS14 chip (Fairlight part # SITA0014) with 74HC14 in location U33. UNITS IN FIELD: If the DIO detection problem is found, replace 74LS14 chip in location U33 on the DIO card with 74HC14 chip. If 74HC14 not available can use 74LS14 Motorola or National brand but NOT TI brand. Changes: 253.1 ECN Withdrawn
MFX 270.2	ESP-DIO-E & ESP-DO-E		**3.9 or 3.10, 4.0**	**3.11, 4.1**	23-Oct-98	DIO (EMC) CARD & DO (EMC) CARD	Noel Plummer	This ECN replaces ECN 253	DIO detection failure with power cycled at 3 seconds OFF interval The fix detailed in ECN 253 was found not to be 100% successful. This new fix is both more successful and much easier to implement.	Rev 3.x Remove tantalum cap at C22. Insert a 3 pin Dallas reset controller IC, DS1233-15 (15%), TO-92 package, Fairlight P/N SIGB0101, at C22 in the following manner. With the edge connector of the PCB closest to you and the flat side of the IC facing U28, insert the middle pin (pin 2) into the hole marked positive (+). Insert the right hand pin (pin 1) of the DS1233 into the other hole of C22. Slide 9mm of insulation onto the left hand pin (pin 3) of the IC and solder it to the left hand lead of R29 (side closest C22). Rev 4.0 Remove diode at D900, tantalum cap at C22 and 100k resistor at R29. Insert a 3 pin Dallas reset controller IC, DS1233-15 (15%), TO-92 package, Fairlight P/N SIGB0101, at C22 in the following manner. With the edge connector of the PCB closest to you and the flat side of the IC facing U28, insert the middle pin (pin 2) into the hole marked positive (+).

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ECNs for DIO Card as at 11/6/99

ECN Number	Assembly	New Assembly	Current Rev	New Rev	Date	Description	Name	Special Note	Reason	Details
										Insert the right hand pin (pin 1) of the DS1233 into the other hole of C22. Slide 9mm of insulation onto the left hand pin (pin 3) of the IC and insert it into the left hand HOLE of R29 (side closest C22). Position this new IC so that its top is no higher than 8mm above the PCB. Note: After this modification the type and brand of IC at U33 no longer matters. Change the assembly revision of the card as per above. UNITS IN WIP: Replace cap at C22 with DS1233 IC in location C22. UNITS IN FIELD: If the DIO detection problem is found, replace cap at C22 with DS1233 IC in location C22. Changes: 270.1 Seperated mod details for 3.x and 4.0 270.2 Added height restriction details for the DS1233 IC.
MFX 289	ESP-DIO-E & ESP-DO-E		**3.11 or 4.1**	**3.12 or 4.2**	30-Mar-99	DIO (EMC) CARD & DO (EMC) CARD	Mario Paolino	This ECN applies to DIOE and DOE cards that will have an AIO2 card attached.	To gain access to the trim pots on the AIO2 and AO2 cards, the D connector cuttout on the support panel needs to be extended.	1. Remove support panel AUP0001XE 2. Add support panel AUP0008X Change Assembly Revision to 3.12 or 4.2
MFX 298	ESP-DIO		**4.2**	**4.3**	27-Apr-99	DIO CARD	George Potkonyak	THIS ECN APPLIES ONLY TO DIO CARDS WHICH ARE USED IN "SANDWICHES" WITH AIO2 (24-BIT) CARDS		1. Reprogram U14 and U17 GAL-s with TEST3 Program, Checksum 978A 2. Assembly revision raised from to Rev. 4.3 NOTE TO PRODUCTION: Reprogram U14 and U17 on all cards in WIP. Relabel GAL-s accordingly. Relabel Card to Rev. 4.3 NOTE TO SUBCONTRACTORS: Reprogram U14 and U17 on all cards in WIP. Relabel GAL-s accordingly. Relabel Card to Rev. 4.3 NOTE TO FIELD SERVICE: If upgrading machines with 24-bit AIO2, reprogram U14 and U17 on DIO Cards. Relabel GAL-s accordingly. Relabel Card to Rev. 4.3

ECN Number	Assembly	New Assembly	Current Rev	New Rev	Date	Description	Name	Special Note	Reason	Details
MFX 95	ESP-DO		**3.7**	**3.8**	12-May-95	Digital Output Card.	Erik de Castro Lopo	This Change Note requires Note 94 to be performed on Digital Output (Only) Card ESP-AO.	Improves SNR of the AOs by preventing audio frequency beating between the 12.288 MHz crystal on the ESP-DO and the sampling rate clocks.	Change Y1 (12.288 MHz crystal) to 12.00 MHz. Label card as Rev 3.8.
MFX 98	ESP-DO		**3.8**	**3.9**	19-May-95	Digital Output (Only) Card	Noel Plummer		Reinstates detail 3 of Change Note 64 which was erroneously removed with Change Note 64A. This improves audio quality.	Change gal at U22 to CLKGEN2. All pins to be placed in socket. Label card as Rev 3.9.
MFX 130.5	PWBMESPDO	PWBMESPDO-E	**3.9**	**3.9**	15-Aug-97	Digital Output Card	Mario Paolino	Applicable to all machines with a requirement for EMC compliance. To be used in conjunction with ECN # 123, 124, 125, 126, 127, 128, 128 (or later revisions)	To modify the current DO card to meet EMC requirements. The following changes are required as part of an overall system modification to make the MFX3 rack meet EMC requirements. It is important that this modification is carried out in conjunction with all other ECNs that outline EMC changes.	1. Viewing the board from the solder side with CN3 on the left, fit the following; Solder a wire (16/0.2 UL 1007) from the left hand mounting guide of CN4 to the right hand mounting guide of CN3. 2. Attach a solder tag CONG5204 Utilux H256 or RS #446-642 using the screw underneath the support block near CN3. Solder the other end to the left hand mounting guide on CN3. This is to ensure that all D connector metal shells have electrical continuity to the chassis. 3. VERY IMPORTANT Trim the mounting guides and arrange the wires so that they protrude NO higher than 1.5mm above the PCB surface. 4. When all modifications have been completed, the part number for the assembly becomes PWBMESPDO-E. Changes: 130.4 Paragraph 2. Re-specify cable and connector specifications. 130.5 Paragraph 1,2,3 Add Product Code for solder tag. Add detailed steps. Add mounting guide dimentions.
MFX 251	ESP-DIO-E, ESP-DO-E		**3.9**	**4**	23-Jul-98	Digital I/O and Digital Output Only Card	Noel Plummer		The ESP-DIO PCB has been redesigned. The new PCB is revision 4. Rev 4 PCB incorporates all mods (including EMC) up to 3.9 therefore assembly revision 4.0 is equivalent to assembly revision 3.9.	New Revision ESP-DIO Blank PCB - Rev 4 Fairlight P/N PWAEESPDIOR4 The new PCB features the following enhancements: Revised split power plane on pp2. Modified boundary keep out to match routing drawing. Corrected power ground expansion on 125 thou holes. Moved tracks away from four screw holes at corners to eliminate need for fibre washers. Increased clearance between pads and solder side tracks. Teardropping added to all pads for improved PCB reliability. Fairlight logo on silkscreen.
MFX 253.1	ESP-DIO-E & ESP-DO-E		**3.9**	**3.9**	08-Oct-98	DIO (EMC) CARD & DO (EMC) CARD	Noel Plummer		DIO detection failure with power cycled at 3 seconds OFF interval	UNITS IN WIP: Replace 74LS14 chip (Fairlight part # SITA0014) with 74HC14 in location U33. UNITS IN FIELD: If the DIO detection problem is found, replace 74LS14 chip in location U33 on the DIO card with 74HC14 chip. If 74HC14 not available can use 74LS14 Motorola or National brand but NOT TI brand. Changes: 253.1 ECN Withdrawn
MFX 270.2	ESP-DIO-E & ESP-DO-E		**3.9 or 3.10, 4.0**	**3.11, 4.1**	23-Oct-98	DIO (EMC) CARD & DO (EMC) CARD	Noel Plummer	This ECN replaces ECN 253	DIO detection failure with power cycled at 3 seconds OFF interval The fix detailed in ECN 253 was found not to be 100% successful. This new fix is both more successful and much easier to implement.	Rev 3.x Remove tantalum cap at C22. Insert a 3 pin Dallas reset controller IC, DS1233-15 (15%), TO-92 package, Fairlight P/N SIGB0101, at C22 in the following manner. With the edge connector of the PCB closest to you and the flat side of the IC facing U28, insert the middle pin (pin 2) into the hole marked positive (+). Insert the right hand pin (pin 1) of the DS1233 into the other hole of C22. Slide 9mm of insulation onto the left hand pin (pin 3) of the IC and solder it to the left hand lead of R29 (side closest C22). Rev 4.0 Remove diode at D900, tantalum cap at C22 and 100k resistor at R29. Insert a 3 pin Dallas reset controller IC, DS1233-15 (15%), TO-92 package, Fairlight P/N SIGB0101, at C22 in the following manner. With the edge connector of the PCB closest to you and the flat side of the IC facing U28, insert the middle pin (pin 2) into the hole marked positive (+). Insert the right hand pin (pin 1) of the DS1233 into the other hole of C22. Slide 9mm of insulation onto the left hand pin (pin 3) of the IC and insert it into the left hand HOLE of R29 (side closest C22). Position this new IC so that its top is no higher than 8mm above the PCB. Note: After this modification the type and brand of IC at U33 no longer matters. Change the assembly revision of the card as per above. UNITS IN WIP: Replace cap at C22 with DS1233 IC in location C22. UNITS IN FIELD: If the DIO detection problem is found, replace cap at C22 with DS1233 IC in location C22. Changes: 270.1 Seperated mod details for 3.x and 4.0 270.2 Added height restriction details for the DS1233 IC.

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ECNs for DO Card as at 11/6/99

ECN Number	Assembly	New Assembly	Current Rev	New Rev	Date	Description	Name	Special Note	Reason	Details
MFX 289	ESP-DIO-E & ESP-DO-E		**3.11 or 4.1**	**3.12 or 4.2**	30-Mar-99	DIO (EMC) CARD & DO (EMC) CARD	Mario Paolino	This ECN applies to DIOE and DOE cards that will have an AIO2 card attached.	To gain access to the trim pots on the AIO2 and AO2 cards, the D connector cuttout on the support panel needs to be extended.	1. Remove support panel AUP0001XE 2. Add support panel AUP0008X Change Assembly Revision to 3.12 or 4.2
MFX 299	ESP-DO		**4.2**	**4.3**	27-Apr-99	DO CARD	George Potkonyak	THIS ECN APPLIES ONLY TO DO CARDS WHICH ARE USED IN "SANDWICHES" WITH AO2 (24-BIT) CARDS		1. Reprogram U14 and U17 GAL-s with TEST3 Program, Checksum 978A 2. Assembly revision raised from to Rev. 4.3 NOTE TO PRODUCTION: Reprogram U14 and U17 on all cards in WIP. Relabel GAL-s accordingly. Relabel Card to Rev. 4.3 NOTE TO SUBCONTRACTORS: Reprogram U14 and U17 on all cards in WIP. Relabel GAL-s accordingly. Relabel Card to Rev. 4.3 NOTE TO FIELD SERVICE: If upgrading machines with 24-bit AO2, reprogram U14 and U17 on DO Cards. Relabel GAL-s accordingly. Relabel Card to Rev. 4.3

ECNs for LTC Card as at 11/6/99

ECN Number	Assembly	New Assembly	Current Rev	New Rev	Date	Description	Name	Special Note	Reason	Details
MFX 6	ESP-LTC		**2**	**2.1**	28-Apr-94	LTC and AES IO	Chris Alfred		PCB error	Cut component side track to P4/1 Cut component side track to P4/2 Cut component side track to P4/3 Cut component side track to P5/2 Cut component side track to P5/3 Connect P4/2 to T2/3 (PE65612) Connect P4/3 to T2/4 Connect P5/1 to U5/8 (74HC4053) Connect P5/2 to T1/3 (PE65612) Connect P5/3 to T1/4 Change C15 to 680pF ceramic
MFX 78.1	ESP-LTC		**2.1**	**2.1**	07-Apr-95	LTC and AES IO	Chris Alfred	Correct typing errors.	Change in flat ribbon cable length due to ease of assembly.	Change flat ribbon cable length from 60mm to 80mm.
MFX 85	ESP-LTC		**2.1**	**2.2**	24-Mar-95	LTC and AES IO	Chris Alfred		Greater noise immunity when there is no input connected to LTC input. This stops the diagnostics reporting bad code and interrupt overrun when no input is connected. It is not essential for this change to be done for correct operation of the system. Cards already at revision 2.1 need not incorporate this change. If the card must be upadated to a higher revision than 2.2, then this change must be implemented. New unpopulated production cards should incorporate this change.	Change R13 to 4k7. Change R26 to 4k7.
MFX 101	ESP-LTC		**2.2**	**2.3**	08-Jun-95	LTC board	Chris Alfred		Allow selection between LTCA or LTCB connector to be fed to LTCA reader chip. This modification is preparation for MFX to only require one LTC reader (LTCA reader).	Cut solder side track to JP1/8. Cut component side track to U5/12 (74HC4053). The track exits U5 between pins U5/4 and U5/5. Connect JP1/8 to JP1/12. Connect U5/12 to U2/7 (LM311).
MFX 127.1	PWBMESPLTC	PWBMESPLTC-E	**2.3**	**2.3**	03-Aug-98	LTC-E Card.	Noel Plummer	ECN withdrawn and replaced by ECN 227.3	ECN withdrawn and replaced by ECN 227.3	ECN withdrawn and replaced by ECN 227.3 Changes: 127.1 ECN withdrawn and replaced by ECN 227.3
MFX 227.3	ESP-LTC-E		**2.3**	**2.3**	03-Aug-98	LTC and AES I/O card, EMC Version.	Noel Plummer	This ECN overrides ECN 127. To be used in conjunction with ECN # 123, 124, 125, 126 (or later revisions) for EMC requirements.	Installation of XLR connectors on ESP-LTC-E by card assembly contractors.	1. ADD: 3 x Connector XLR Female Fairlight P/N COND0119 Neutrik NC3FD-L-1 2. ADD: 2 x Connector XLR Male Fairlight P/N COND0120 Neutrik NC3MD-L-1 3. View the board with P1 on the left, component side up. Solder 25mm long flying leads (16/0.2 UL1007) from the XLR connectors to the PCB in the following manner. (refer attached diagram) A: For connectors P1, P2 & P4, attach pin1 of connector to left hand hole, pin2 of connector to right hand hole & pin3 to middle hole. Earth shell of connector to pin1." B: For connectors P3 & P5, attach pin1 of connector to right hand hole, pin2 of connector to left hand hole, & pin3 to middle hole. Earth shell of connector to pin 1." Changes: 227.2 Correction of ECN 227.1 227.3 Correction of ECN 227.2
MFX 275	ESP-LTC & ESP-LTC-E	ESP-LTC-C	**2.3**	**3**	02-Dec-98	LTC and AES I/O card	Noel Plummer		The ESP-LTC PCB has been redesigned. The new PCB is revision 3. It incorporates all mods (including EMC) up to revision 2.3. Assembly revision 3.0 is equivalent to assembly revision 2.3 except for the addition of C19 between pin 1 of P4 (AES SYN input) and ground. The new PCB eliminates the need for the two version of the assembled card, the non-EMC (ESP-LTC) and EMC (ESP-LTC-E) versions.	New Revision ESP-LTC Blank PCB - Rev 3 Fairlight P/N PWAEESPLTCR3 The new PCB features the following enhancements: Incorporates all mods up to Assembly Rev 2.3 plus C19. Layout changed from 2 layer to 4 layer. Both inner power planes split into 3 zones. XLRs changed to PCB EMC type Neutrik NC3FD-H and NC3MD-H, to eliminate the flying leads. PCB depth reduced by 1.35" to 3.175" to facilitate cable insertion onto the Midi card. Increased pad to track clearance on solder side to improve reliability. All pads and vias teardropped for improved reliability. Moved support blocks 0.025" towards PCB edge so that blocks align with the edge. Added Fairlight Logo on top overlay.

ECNs for MFK Card as at 11/6/99

ECN Number	Assembly	New Assembly	Current Rev	New Rev	Date	Description	Name	Special Note	Reason	Details
MFX 152.2	ESP-MFK	ESP-MFK	**2**	**2.1**	28-Oct-96	Console Keyswitch	Leith Stewart	This ECN to be implemented with ECN 153.	1. There is not enough space to install JP2 and JP3 on the MFK card as they interfere with the jogger connector. 2. To facilate easy adjustment of both the speaker volume and the display contrast the adjustment pots on the MFX010 card are to moved to the MFK card.	1. Delete or remove connectors JP2 and JP3. (ESP part # CONG5208). Mask holes during wavesoldering. 2. On the solder side, install a single 6 pin header (e.g Molex 6410 Series UL Recognised) at JP4 and JP5 (ESP part # CONG5289). 3. Install a 10k trim pot at RV1 (ESP part # POTR6114) 4. Install a 1k trim pot at RV2 (ESP part # POTR6117) Changes: Change 2 x 3 way headers to 1 x 6 way header. JP4 & 5 on solder side.
MFX 175	AUPC1000X		**2**	**3**	23-Dec-96	MFK Keyplate	Leith Stewart		Keyplate assembly cannot be correctly aligned due to manufacturing tolerances of the faceplate assembly.	1. Refer to drawing D3.760.002, Sheet 1 of 2. The 7 mounting holes (Reference B) are specified as 5.0mm diameter holes. Resize these holes to 7.0mm diameter. 2. Touch up resized holes with black paint. 3. New drawing issued D3.760.002 Rev 3.0.
MFX 206	CABM6255		**1.2**	**1.3**	26-May-97	CABLE 010-MFK 50W IDC SIGNAL, UL	RAJEEV GANESH		CABM6255 is too short and gets strained during assembly and dis-assembly of the Console.	Length needs to be extended from 350mm to 480mm. Dawing modified and is attached.
MFX 225.1	ESP-MFK	ESP-MFK	**2.1**	**2.2**	19-Sep-97	Console Keyswitch	ANDREW BELL		To facilitate a new feature in system software revision 14.3 - a legend change is required on 8 keycaps used on the MFK assembly.	1. DELETE: SWD1000 Keytop Set for MFX Console - ESPMFK card 2. ADD: SWD1001 Keytop Set for MFX Console - ESPMFK card 3. Relabel the PCB Rev. 2.2 Difference: 8 x keycaps have changed, refer to overlay 1. Blank key is now Audio Base 2. MFX key is now Export MFX 3. B1 key is now Blank 4. B2 key is now Blank 5. B3 key is now Blank 6. B4 key is now Blank 7. M1 key is now Blank 8. M2 key is now Blank Implementation: The new keytop set is to be used immediately i.e. independently of the release of software.

ECN Number	Assembly	New Assembly	Current Rev	New Rev	Date	Description	Name	Special Note	Reason	Details
MFX 5	ESP-MIDI		**2**	**2.1**	28-Apr-94	SYNC IO Support and MIDI	Chris Alfred		Additional synchronisation features.	MCLKIN from AES reference. Connect U23/19 (CS8411) to JP5/45. VSYNC reference Connect U5/3 (LM1881) to JP5/46 and U16/3 (74HC251). RTS/CTS for RS232 Cut component side track to U33/9 (74HC4053) Connect U33/9 to RN3/3 Cut solder side track to U18/8 (68681FN) Cut solder side track to U18/5 Connect U18/43 to U14/6 (TR1) Connect U18/42 to U20/6 (TR1) Connect U18/5 to JP2/18 Connect RN3/2 to JP2/17. V+/V1 to JP2 Connect JP2/19 to JP6/3 Connect JP2/20 to JP6/4 . Timecode readers Cut component side track to U13/5 Cut solder side track to U13/6 Cut solder side track to U12/5 Cut solder side track to U12/6 Connect U12/5 to U13/5 and JP2/14 Connect U12/6 to JP6/10 Connect U13/6 to JP6/8 Cut component side track to U20/27 Cut solder side track to plate-thru near U14/2 Connect U17/13 to U12/11 and U13/11 Connect U12/10 to U12/16 Connect U13/10 to U13/16 Connect U12/9 to U20/27 Connect U13/9 to U14/27
MFX 16	ESP-MIDI		**2.1**	**2.2**	29-Jun-94	Sync IO support and MIDI	Chris Alfred		Shift signals to allow for full RS232 implementation on ESP-IO in fututre. Once these changes have been made, SC Disagnosticssx must be Rev 1.3 or higher.	Cut solder side track to U18/40 (68681) Cut solder side track to U18/3 Cut component side track to U33/11 (74HC4053) Connect U14/5 (TR1) to U11/8 (68681) Connect U20/5 (TR1) to U11/5 Connect U33/11 to U11/30
MFX 30	ESP-MIDI		**2.2**	**2.3**	15-Aug-94	MIDI Card	Chris Alfred		Differentially buffer AES sync. To be done in conjunction with Change Note 29.	Cut component side track to Q1 collector (BC549). Cut component side track to Q2 collector (BC549). Cut solder side track to R30 pin nearest edge of PCB. Connect U23/19 (CS8411) to U29/15 (3487). Connect U29/14 to JP5/40. Connect U29/13 to JP5/38. Q1 and Q2 collectors are pins nearest R29.
MFX 31	ESP-MIDI		**3**	**3.1**	12-Sep-94	MIDI Card	Chris Alfred		The Rev 3 PCB is equivalent to a Rev 2.1 assembled board. Make Rev 3.1 PCB same as Rev 2.3 PCB.	Cut solder side track to U18/40 (68681) Cut solder side track to U18/3 Cut component side track to U33/11 (74HC4053) Connect U14/5 (TR1) to U11/8 (68681) Connect U20/5 (TR1) to U11/5 Connect U33/11 to U11/30 Cut component side track to Q1 collector (BC549). Cut component side track to Q2 collector (BC549). Cut solder side track to R30 pin nearest edge of PCB. Connect U23/19 (CS8411) to U29/15 (3487). Connect U29/14 to JP5/40. Connect U29/13 to JP5/38. Q1 and Q2 collectors are pins nearest R29.
MFX 38.1	ESP-MIDI		**2.3, 3.1**	**2.4, 3.2**	16-Mar-98	MIDI card	Chris Alfred	Correction to show that the same ECN applies to Rev 3 cards	Modifications to use ESP-PLL board.	Connect 75R across J1. Disconnect modifications to U5/3 (LM1881). Connect U5/7 to U16/3 (74HC251). Disconnect modification wire to RN3/3. Connect U33/9 (74HC4053)to RN2/3. Connect RN3/3 to U16/15. Disconnect modification wire to JP5/45. Disconnect modification wire to U29/15 (3487). Disconnect modification wire to U29/14. Disconnect modification wire to U29/13. Disconnect modification wire joining U12/11 and U17/13. Connect 40way cable with 40way IDC cable connector at one end, and the other end to the ESP-MIDI solder side as follows and the other end to the ESP-MIDI solder side as follows: Wire - ESP-MIDI: 1 - U15/4, 2 - U15/5, 3 - U15/6, 4 - U15/7, 5 - U15/8, 6 - U15/9, 7 - U15/10, 8 - U15/11, 9 - U18/38, 10 - U19/11, 11 - U30/3, 12 - U30/13, 13 - U23/6, 14 - U23/7, 15 - U23/4, 16 - U23/3, 17 - U23/2, 18 - U23/1, 19 - U23/28, 20 - U23/27,

ECN Number	Assembly	New Assembly	Current Rev	New Rev	Date	Description	Name	Special Note	Reason	Details
										Wire - ESP-MIDI: 21 - U23/11, 22 - U16/3, 23 - U16/14, 24 - U16/4, 25 - U17/12, 26 - U17/5, 27 - JP5/45, 28 - JP5/35, 29 - U18/40, 30 - U18/31, 31 - U18/8, 32 - U12/11, 33 - JP5/46, 34 - JP5/42, 35 - JP5/40, 36 - JP5/38.
MFX 39	ESP-MIDI		**2.4, 3.2**	**2.5, 3.3**	20-Oct-94	MIDI Card	Chris Alfred		FRVIDEO output from LM1881 has slow rise time. Noise induced from AESWCLK on cable to ESP-PLL can cause glitches at switching point of receiving buffer caused edge detection. This change note buffers the signal so fast edge signal is transferred to ESP-PL	Remove modification wire between U5/7 (LM1881) and U16/3 (74HC251) Connect U5/7 to U27/5 (74HC04). Connect U27/6 to U16/3.
MFX 40.1	CABM7327				21-Nov-94	ESP-SYN to ESP-MIDI 60 way cable	Chris Alfred		ESP-MIDI Rev 4 PCB and above has JP5 (60way half pitch connector) re-configured. This requires that the two 30 way cables should not have a cross-over twist. ESP-MIDI revisions below 4.0 MUST use existing twisted cables Part No. CABM7328.	Cable to be manufactured without the two 30 way cables having a cross-over twist. Parts requied are; a. Connector part no. COND6102, Quantity X2 b. 34 Way flat cable part no. CABG6021 to be modified to 30 way. Length to be determined as per machine configuration.
MFX 43	ESP-MIDI		**2.5, 3.3, 4**	**2.6, 3.4, 4.1**	01-Nov-94	MIDI Card	Chris Alfred		Fix LTC port B interrupt detection. MIDICLK on inputs IP2-5 cause buss noise when reading input port.	Cut solder side track to U11/43 (68681) on side nearest U6. Cut solder side track to U11/42 (68681) on side neatest U10. Connect U8/4 (74HC590) to U10/40 (68681).
MFX 49	ESP-MIDI		**2.6, 3.4**	**2.7, 3.5**	04-Nov-94	MIDI Card	Chris Alfred		Use frame clock from LTC readers rather than bit clock.	Cut solder side track to U17/12 (74HC251). Cut solder side track to U16/4 (74HC251). Connect U17/12 to U14/20 (TR1). Connect U16/4 to U20/20 (TR1).
MFX 51	ESP-MIDI		**2.7, 3.5**	**2.8, 3.6**	14-Nov-94	MIDI Card	Chris Alfred		Fix design error. Disables word clock from multi-mfx interface.	Cut both solder side tracks to JP1/15. Connect JP2/11 to U17/4 (74HC251). Once this modification is done, the 'SC' diagnostic 'UC' command for the ESP-9PIN is obsolete and will not work.
MFX 52	ESP-MIDI		**4.1**	**4.2**	18-Nov-94	MIDI Card	Chris Alfred		Fix design errors.	Connect U30/5 (3486) to U18/11 (74HC374). Use MIDECO gal at U15. Cut both solder side tracks to JP4/15. Connect JP6/11 to U16/4 (74HC251). Connect JP4/15 to JP5/40.
MFX 54	CABM7300				21-Nov-94	ESP-PLL to ESP-MIDI 40 way Cable	Chris Alfred		New Cable required for ESP-MIDI Rev 4 PCB connector location JP5 (40 Way header/box connector) for Data transfer to ESP-PLL connector location JP7 (40 Way header/box connector). Part Number allocated CABM7300.	40 way cable required to be made up in a one-to-one connection using 40 way flat cable connector sockets as per following specifications; a. Connector part no. COND6035, Quantity X 2 b. 40 way flat cable part no. CABG6042, Length X 170mm
MFX 66	CABM7332				16-Dec-94	ESP-PLL to ESP-MIDI Rev. 4 26 way Cable	Chris Alfred		New Cable required for ESP-MIDI Rev 4 PCB connector location JP6 (26 Way header/box connector) for Interface connections to ESP-PLL connector location JP3 (26 Way header/box connector). Part Number allocated CABM7332.	26 way cable required to be made up in a one-to-one connection using 26 way flat cable connector sockets as per following specifications; a. Connector part no. COND6004, Qty X 2 b. 26 way flat cable part no. CABG6014, Length X 170mm.
MFX 72	ACCU.				16-Jan-95	Installation of ESP-MIDI Rev 4 in ACCU	Chris Alfred		ESP-MIDI Rev 4.	1. Dis-connect 10 way female IDC connector from S4 on CMI 354 (MFX Interface card) and connect to ESP-Midi connector location JP3. 2. Dis-connect cable from connector location J2 on CMI 335 (Analog Motherboard) on one side and S2 of PCB CMI354 on the other end; and discard 3. Dis-connect 28-way female IDC connector from S1 on CMI 354 (MFX Interface card) and connect to PCB CMI335 at connector location J2. The extra length of this cable should be tied into a location J2. The extra length of theis csble should be tied into a small, neat bundle and located appropriately with cable ties etc. 4. Cable connecting ESP-MIDI Rev 4 to SYNC Module does not require the twist. This cable assembly is presently made up of the following two parts; i. Sync to external P/No CABM7328A. ii.MIDI to external P/No. CABM7328B. The Part No. for this cable assembly (comprising both parts) is CABM7328 presently. Part No.s have been allocated to each part as above. The new cable assembly Part No. CABM7328/4 also comprises of two parts with a change only on the MIDI to external cable. New Part No. allocated is CABM7328C and the specifications of the new MIDI to external cable are; a: Connector P/N COND6028, Qty X 1 b: Connector P/N COND6837, Qty X 1 c: Connector P/N COND6102, Qty X 1 d: Connector P/N CABG6021, Length X 1.4m Drawings for both cables are attached. Summary: Existing Cables are CABM7328, made up from both CABM7328A & CABM7328B. New Cables are CABM7328/4 made up of CABM7328A & CABM7328C 5. Dust covers or other alternatives for the unused 25 pin D-type, 9 pin types and the 24 pin MFX connectors is under investigation and will be informed at a later date.

ECNs for MID Card as at 11/6/99

ECN Number	Assembly	New Assembly	Current Rev	New Rev	Date	Description	Name	Special Note	Reason	Details
MFX 75.1	ESP-MIDI		**4.2**	**4.3**	09-Feb-95	MIDI Card	Chris Alfred		DUART (68681) at U17 can be destroyed by noise received via MFX cable. This Change Note buffers the *MFXDETECT signal to protect the DUART, and references the cable GND to the system digital ground. When the DUART is destroyed, the system can't detect the Sync IO module when the MFX cable is not CONNECTED. There are also cases of the destroyed DUART causing intermittent crashes of the MFX console (usually detected by the PLAY light flashing and transport remains stationary). If similar problems are occurring, the DUART at U17 should be replaced and this Change Note performed on the card.	Cut solder side track to R2 (2K2) on side nearest U1 (LM1881). Connect R2 pin nearest JP1 to U6/3 (74HC14). Connect U6/4 to U17/3 (68681). Place shorting plugs on all 4 positions on JP1. (i.e. short pins 1-2, 3-4, 5-6, and 7-8).
MFX 83	ESP-MIDI		**2.8, 3.6, 4.3**	**2.9, 3.7, 4.4**	08-Mar-95	MIDI Card	Chris Alfred		Remove overshoot on SYSCLK input to TR1 timecode reader chip to significantly reduce probability of TR1 starting in test mode which stops it reading timecode. There is a bug in the TR1 chip which can cause it to power-up in test mode. The test mode can only be exited by power-cycling the chip until it does not start in test mode. This problem is still under investigation by ARTI (the manufacturer of the TR1) and Fairlight. After this modification, the TR1 will start in test mode approximately once in 60 power-cycles.	Connect 100pF ceramic capacitor across U14 (TR1) pins 1 and 4. Connect 100pF ceramic capacitor across U20 (TR1) pins 1 and 4.
MFX 84	ESP-MIDI		**2.9, 3.7, 4.4**	**2.1, 3.8, 4.5**	10-Mar-95	MIDI Card	Chris Alfred		Fix random failure of LTC readers. The SYSCLK input is driven by a CMOS gate. The tIMCD input is held low while the *RESET is asserted on the ESP-SYN.	Rev 4 PCB 1 Remove U12 and U13 (both 74LS157). 2. Lift pin 15 of a 74HC157 and place in U12. 3. Lift pin 15 of a 74HC157 and place in U13. 4. Connect the lifted U13/15 to the lifted U12/15 and to U6/6 (74HC14) 5. Connect U6/5 to RN5/10. Rev 2 and 3 PCB 1. Remove U12 and U13 (both 74LS157). 2. Lift pin 15 of a 74HC157 and place in U12. 3. Lift pin 15 of a 74HC157 and place in U13. 4. Connect the lifted U13/15 to the lifted U12/15 and to U29/13 (3487) 5. Connect U29/15 to RN5/10.
MFX 99.2	ESP-MIDI		**4.5**	**4.5**	15-Jul-96	MIDI card	Chris Alfred	For manufacturing only.	Unavailabilty of ARTI TR1 ICs.	1. Do not place IC ARTI TR1 and socket at location U20. 2. Connect U20/5 to U20/1. 3. Do not place modification capacitor of 100pF between pins 1 and 4 of U20. (ECN # 83)
MFX 102	ESP-MIDI		**3.8**	**3.9**	13-Jun-95	MIDI Card	Chris Alfred	Rev 3 cards only	40 way cable directly soldered too ESP-MIDI Rev3 to ESP-PLL card does not have all signals connected. This stops AES sync working when using DIRECT mode as provided by x_pll xilinx revs above 5. Note that some old Rev 3 ESP-MIDI cards have the last four wires of the 40 way cable stripped off, this mod is not possible on these cards. Instead, the card should be replaced with a Rev 4 card.	Connect cable wire pin 38 to U23/19 (CS8411). Connect cable wire pin 40 to JP4/15.
MFX 104.2	ESP-MIDI		**4.5**	**4.5**	15-Jul-96	MIDI Card	Erik de Castro Lopo		The ARTI TR1 chip is no longer available.	1. The ARTI TR1 chip at location U14 may be replaced with Otari I-0055 chip without further modification. 2. Do not place modification capacitor of 100pF between pins 1 and 4 of U14.
MFX 118	ESP-MIDI		**4.5**	**4.6**	21-Nov-95	MIDI Card	Chris Alfred		Allow ESP-MIDI Rev 4 to operate correctly when using Music Software. The MIDI C input to the CMI28 Midi Processor card was not terminated which would cause spurious interrrupts thus slowing MIDI Processor operation.	1. Connect solder side edge connector (CN1) pin 43B to TP2.

Complied by Noel Plummer

ECNs for MID Card as at 11/6/99

ECN Number	Assembly	New Assembly	Current Rev	New Rev	Date	Description	Name	Special Note	Reason	Details
MFX 129.2	PWBMESPMIDI	PWBMESPMIDI-E	**4.6**	**4.6**	14-Oct-96	MIDI Card.	Leith Stewart	Applicable to all machines with a requirement for EMC compliance. To be used in conjunction with ECN # 123, 124, 125, 126, 127, 128 (or later revisions)	To modify the current MIDI card to meet EMC requirements.	1. The following changes are required as part of a system modification to make the MFX3 rack meet EMC requirements. It is important that this modification is carried out in conjunction with all other ECNs that outline EMC changes. 2. Replace BNC connector J1 with metal shell connector (F/Light # COND6998 - Connector BNC Vitelec VBM211). Ensure that the star washer is placed and that the nut is well tightened to the support panel to ensure good electrical contact. 3. Replace all 5 pin DIN connectors (P1 to P4) with metal shell DIN connectors (F/Light # COND6786 - Connector 5P DIN Preh 71206-050). 4. Viewing board with P1 on the left, component side up, attach flying leads (UL Recognised 16/0.2mm wire) for connectors P3 & P4 in the following manner. Attach pin4 of connector to bottom right hole, attach pin2 of connector to centre hole, and attach pin5 of connector to bottom left hole. For each connector, the holes on the PCB not previously mentioned should be left unattached. Do not earth shell of connector. Ensure pins 1 & 3 of connector are not in contact with anything. Cut off excess tabs if necessary. 5. Viewing board with P1 on the left, component side up, attach flying leads (UL Recognised 16/0.2mm wire) for connectors P1 & P2 in the following manner. Attach pin4 of connector to bottom right hole, and attach pin5 of connector to bottom left hole. For each connector, the holes on the PCB not previously mentioned should be left unattached. Do not earth shell of connector. Ensure pins 1, 2 & 3 of connector are not in contact with anything. Cut off excess tabs if necessary. 6. When all modifications have been completed, the part number for the assembly becomes PWBMESPMIDI-E. Changes: Add Gnd Connection to DIN connectors.
MFX 143	ESP-MIDI		**4.6**	**4.7**	27-Jun-96	MIDI Card	Chris Alfred		OTARI LTC reader chips are unable to read both timcode and user bits without causing errors in the read data. Any such errors will stop MFX3 from locking to LTC. The most commonly observed effect is an inability to lock to LTC when using SONY slave.	See included diagram of solder-side for track-cut locations. 1. Cut solder-side track to JP5/6 (34 way box connector) on side nearest U14 (TR1). 2. Cut solder-side track to plate-thru via directly between pins 5 and 24 of U20 (TR1). 3. Connect U23/16 (CS8411) to JP5/6. 4. Connect U14/24 (TR1) to U14/28.
MFX 148	ESP-MIDI-E		**4.6**	**4.7**	27-Jun-96	MIDI Card (EMC)	Chris Alfred		OTARI LTC reader chips are unable to read both timcode and user bits without causing errors in the read data. Any such errors will stop MFX3 from locking to LTC. The most commonly observed effect is an inability to lock to LTC when using SONY slave.	See included diagram of solder-side for track-cut locations. 1. Cut solder-side track to JP5/6 (34 way box connector) on side nearest U14 (TR1). 2. Cut solder-side track to plate-thru via directly between pins 5 and 24 of U20 (TR1). 3. Connect U23/16 (CS8411) to JP5/6. 4. Connect U14/24 (TR1) to U14/28.
MFX 149.1	ESP-MIDI & ESP-MIDI-E		**4.7**	**4.8A, 4.8O**	25-Sep-96	MIDI Card and MIDI Card (EMC)	Rajeev Ganesh		The ATRI TR1 LTC reader chip has frame interrupt biased early by 16 subframes; whereas the OTARI I-0055 LTC reader chip has no such bias. Software prior to revision 12.3.17 aligns timecode correctly for the TR1; but is aligned 16 subframes late for the I-0055. The bias can be observed by measuring the difference between the LTC input and LTC generator output from MFX3. This ECN provides a way for software revisions 12.3.17 and higher to know which chip is installed via the setting of the DIP switch (S1) switch 1 to ensure correct timecode alignment for both LTC readers.	Set DIP switch (S1) switch 1 (switch nearest U18) according to the table below: LTC Readers at U14 and U20 — S1 switch 1 ARTI TR1 — OFF OTARI I-0055 — ON Relabel PCB as 4.8A if ATRI chip present, or 4.8O if OTARI chip present
MFX 228.2	ESP-MIDIE		**N/C**	**N/C**	17-Mar-98	Midi and Sync Control card	Mario Paolino	Correction to Revision Number This ECN applies to Board Assembler	Installation of DIN connectors Correction of ECN 228	1. ADD: 4 x Socket COND6787 DIN 5P 45 FE15 2. Solder the flying leads to the DIN connectors as per the following diagram. 3. No Change to the Revision Number

ECNs for MID Card as at 11/6/99

ECN Number	Assembly	New Assembly	Current Rev	New Rev	Date	Description	Name	Special Note	Reason	Details
MFX 249.1	ESP-MIDI & ESP-MIDI-E	ESP-MIDI-C	**4.8x**	**5.0x**	20-Jul-98	Midi and Sync Control card	Noel Plummer		The ESP-MIDI PCB has been redesigned. The new PCB is revision 5. Rev 5 PCB incorporates all mods up to 4.8 therefore assembly revision 5.0 is equivalent to assembly revision 4.8. The new PCB also eliminates the need for the two version of the assembled card, the non-EMC (ESP-MIDI) and EMC (ESP-MID-E) versions. The new PCB also features the following enhancements: Allows installation of Preh locking DIN EMC type connectors. Rear panel connectors to connected to chassis ground. JP3 moved alongside JP7 to eliminate need for short cable on JP3. Pad to track clearance increased for improved reliability. Jumpers eliminated by pre-linking JP1 and JP9 on PCB. Teardropping added to all pads for improved PCB reliability.	New Revision ESP-MIDI Blank PCB - Rev 5 P/N PWAEESPMIDIR5 Part Number 1MFXPWBMIDC replaces 1MFXPWBMIDE and 1MFXPWBMIDZ Part Number MANMESPMIDC replaces MANMESPMIDIE and MANMESPMIDI Other new part numbers with related P/Ns shown in brackets: EXCMIDC (EXCMIDE and EXCMIDI) FAULTYMIDC (FAULTYMIDE and FAULTYMIDI) REPMIDC (REPMIDE and REPMIDI) WARMIDC (WARMIDE and WARMIDI) The 4 jumpers (P/N COND6747) and the 4 x 2 Header (P/N CONG5233-4) have been eliminated by pre-linking on the PCB. The re-positioning of JP3 has eliminated the need to plug the short extender cable (P/N CABM7334) into JP3, before assembling the SYNC-IO module. Changes: 249.1 Deleted line 4 of Details of Change, corrected part numbers in first three lines of Details of Change.
MFX 266	ESP-MIDI-C		**5.0x**	**6.0x**	28-Sep-98	Midi and Sync Control card	Noel Plummer		The ESP-MIDI blank PCB has been updated again to correct JP3 layout error in rev. 5. The new PCB is revision 6 which is electrical equivalent to rev. 5 PCB. Rev. 6 allows a box header to once again be used at JP3. JP8 has been moved slightly to the left, to improve alignment with the cable which comes from the LTC card. The position of mounting holes for the aluminium support blocks has been corrected. They have been moved 0.025" closer to the front panel board edge.	New Revision ESP-MIDI Blank PCB - Rev 6 P/N PWAEESPMIDIR6

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ECNs for P19 Card as at 11/6/99

ECN Number	Assembly	New Assembly	Current Rev	New Rev	Date	Description	Name	Special Note	Reason	Details
MFX 229	1MFXCSLPSAN, 1MFXCSLPO2N, 1MFXCSLP19N				16-Oct-97	CONSOLE MFX+ S/A , O2R, 19"	Noel Plummer		A number of MFX+ consoles have recently been shipped with a non-locking type DIN connector on the external power supplies. This connector has been found to cause problems if the console is moved while powered and in particular the console's config info, stored in the NVRAM, is corrupted.	Replace the DIN connector with a locking type (Fairlight P/N COND6784, Preh P/N 71430-070, Farnell P/N 437-220) as per attached drawing PSU2001.DW2 rev 1.7.
MFX 235	CSLMFXP19		**1.4**	**1.5**	24-Nov-97	MFX Plus 19" Rack Mount Console	Mario Paolino		Introduction of MFX-010 Rev 7 PCB see ECN 233	1. Delete CABM6259 2. Add CABM6259C 3. Change assembly revision to 1.5
MFX 260	CSLMFXP19		**2**	**2.1**	31-Aug-98	MFX Plus 19" rack mount console	Mario Paolino	Production Only Field Action: None WIP Action: None	The cable providing power to the LCD backlight, loops from one LCD to the next. The centre connector has 2 wires crimped onto the one pin which makes the join unreliable.	Delete: 1 x CABM6258 MFX010 to MFK LCD power Add: 2 x CABM6261 MFX010 to MFK LCD power Change Assembly revision as detailed above.

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ECNs for PCI Card as at 11/6/99

ECN Number	Assembly	New Assembly	Current Rev	New Rev	Date	Description	Name	Special Note	Reason	Details
MFX 221	ESP-PCI		**5**	**5.1**	04-Sep-97	PCI Card	MARIO PAOLINO		Connector JP3 is for R&D use. Not required for production.	1. Remove Connector 1 * 8 Header, CONG5272-8 from location JP3 2. Relabel PCB Assembly as 5.1.
MFX 248	ESP-PCI		**5.1**	**5.2**	13-Aug-98	PCI Card	Noel Plummer		The Lattice firmware on the PCI card has been changed for the following reasons. To fix clicks in audio during record. To allow use of Symbios 53C810 based cards.	Reload the PCI Lattice device using the wxcgpc7.dld file. This file is included with documentation in the wxcgpc7.zip file available from the Fairlight BBS. Refer to wxcgpc7.doc for instructions. Change assembly revision number on the PCI PCB to 5.2
MFX 306	ESP-PCI		**5.2**	**5.2**	27-May-99	PCI Card	Mario Paolino	For Your Information Only	Superceded Network & SCSI card have been replaced by currently available substitutes.	1. Fairlight Pn: PASYPWBPNE Ether Express PRO 10/100TX PCI Buss RJ45 was IT PILA8460 is now a IT PILA8460B 2. Fairlight Pn: PASYPWBPSN PCI Fast SCSI II card was Symbios 8100S is now a Symbios 810 Assembly revision number remains the same.

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ECNs for PLL Card as at 11/6/99

ECN Number	Assembly	New Assembly	Current Rev	New Rev	Date	Description	Name	Special Note	Reason	Details
MFX 33	ESP-PLL		**2**	**2.1**	10-Oct-94	Phase Locked Loop Card	Chris Alfred		Connect WCLKREF to external PLL connector JP4. Schmitt trigger on frame inputs.	Change U23 to 74LS244. Connect JP4/9 to U14/10 (PLWDIV). Mark PCB as Rev 2.1.
MFX 36	ESP-PLL		**2.1**	**2.2**	19-Oct-94	Phase Lock Loop Card	Chris Alfred		Quicker lock time and reduced jitter from RUNPLL,FRAMEPLL. Remove phase comparator feed-thru to VCO control on word clock PLLs.	Change R46 to 10k. Change R49 to 39k. Change C46 to 100nF monolithic capacitor. Connect 470nF monolithic capacitor across R54. Connect 470nF monolithic capacitor across R58. Connect 470nF monolithic capacitor across R62. Mark PCB as Rev 2.2.
MFX 41	ESP-PLL		**2.2**	**2.3**	28-Oct-94	Phase Lock Loop Card	Chris Alfred		Fix error in crystal oscillator circuit. Fix adjustment range of crystals.	Do not populate capacitor locations C64, C65, C82 and C83 till further notice.
MFX 45	ESP-PLL		**2.3**	**2.4**	01-Nov-94	Phase Lock Loop Card	Chris Alfred		Fix WCLKOUT level. Remove VITC sync glitches. Fix audio clicks.	Change R8 to 4R7. Connect 75R across C2 (10p). Cut component side track to U11/7 (LM1881) on side nearest C18. Connect JP3/13 to U23/9 (74LS244). Remove R35,R38,R40. Connect U25/5 (74HC14) to U16/4 (PLWMUX). Connect U26/5 (74HC14) to U16/6. Connect U26/9 to U16/8.
MFX 47	ESP-PLL		**2.4**	**2.5**	03-Nov-94	Phase Lock Loop card	Chris Alfred		Fix clicking when NS 3486 chips used in system.	Change PLWMUX at U16 to PLWMUX2.
MFX 50	ESP-PLL		**2.5**	**2.6**	11-Nov-94	Phase Lock Loop Card	Chris Alfred		Improve distortion at 48k and 32k.	Change R57 (100k) to 100R. Change R61 (100k) to 100R. Change R65 (100k) to 100R.
MFX 53	ESP-PLL		**2.6**	**2.7**	18-Nov-94	Phase Lock Loop Card	Chris Alfred		Connect WCLK from multi-MFX interface to PLL card.	Connect JP7/40 to U18/56 (XC3042).
MFX 54	CABM7300				21-Nov-94	ESP-PLL to ESP-MIDI 40 way Cable	Chris Alfred		New Cable required for ESP-MIDI Rev 4 PCB connector location JP5 (40 Way header/box connector) for Data transfer to ESP-PLL connector location JP7 (40 Way header/box connector). Part Number allocated CABM7300.	40 way cable required to be made up in a one-to-one connection using 40 way flat cable connector sockets as per following specifications; a. Connector part no. COND6035, Quantity X 2 b. 40 way flat cable part no. CABG6042, Length X 170mm
MFX 55	ESP-PLL		**2.7**	**2.8**	23-Nov-94	Phase Lock Loop Card	Chris Alfred		Fix marginal locking to LTC at 30fps. Faster frame source lock time.	Change C42 to 470nF monolothic ceramic. Change R46 to 100k. Change C46 to 470nF monolithic ceramic. Change R52 to 100k.
MFX 66	CABM7332				16-Dec-94	ESP-PLL to ESP-MIDI Rev. 4 26 way Cable	Chris Alfred		New Cable required for ESP-MIDI Rev 4 PCB connector location JP6 (26 Way header/box connector) for Interface connections to ESP-PLL connector location JP3 (26 Way header/box connector). Part Number allocated CABM7332.	26 way cable required to be made up in a one-to-one connection using 26 way flat cable connector sockets as per following specifications; a. Connector part no. COND6004, Qty X 2 b. 26 way flat cable part no. CABG6014, Length X 170mm.
MFX 90	ESP-PLL		**2.8**	**2.8**	13-Apr-95	Phase Lock Loop Card	Chris Alfred	This formalises current use.	Fix error in crystal oscillator circuit. Fix adjustment range of crystals.	1. Place and solder following capacitors C64 Ceramic 33pF 50V as per BOM Rev. 3.0 C65 Ceramic 33pF 50V as per BOM Rev. 3.0 C82 Ceramic 33pF 50V as per BOM Rev. 3.0 C83 Ceramic 12pF 50V as per BOM Rev. 3.0 (This overrides ECN 41) 2. Solder following capacitors on the solder side. Ceramic 150pF 50V parallel to C64. Ceramic 82pF 50V parallel to C65. Ceramic 82pF 50V parallel to C82. Ceramic 56pF 50V parallel to C83. 3. It is essential that crystals Y1, Y2,Y3 and Y4 be exactly the same as are presently in use i.e. Manufacturer: Rakon Supplier: Dalkeith Batch : #215 MAR Marking: DDD16 4. If the crystals as above are not available then capacitors C64, C65, C82, C83 should be left off.
MFX 123	ESP-PLL		**2.8**	**2.9**	08-Feb-96	Phase Lock Loop Card	Erik de Castro Lopo	Applies to all production machines.	To remove redundant crystal modules for EMC compliance.	1. Remove 20MHz Crystal Module (X1).

ECNs for PLL Card as at 11/6/99

ECN Number	Assembly	New Assembly	Current Rev	New Rev	Date	Description	Name	Special Note	Reason	Details
MFX 128	PWBMESPPLL	PWBMESPPLL-E	**2.9**	**2.9**	22-Feb-96	Phase Lock Loop Card	Leith Stewart	Applicable to all machines with a requirement for EMC compliance. To be used in conjunction with ECN # 123, 124, 125, 126, 127 (or later revisions)	To modify the current PLL card to meet EMC requirements.	1. The following changes are required as part of a system modification to make the MFX3 rack meet EMC requirements. It is important that this modification is carried out in conjunction with all other ECNs that outline EMC changes. 2. Replace all BNC connectors with metal shell connector (F/Light # COND6998 - Connector BNC Vitelec VBM211). Ensure that the star washer is placed and that the nut is well tightened to the support panel to ensure good electrical contact. 3. Viewing the board solder side up, P1 on the left, solder a wire (24AWG) from the right shell mounting guide of P1 (9P M) to the left hand mounting guide of P2 (9P M) together using 24AWG wire. Solder another wire (24AWG) to the left hand mounting guide of P1 and screw the other end to the support block screw (a crimp terminator may be used). 3. When all modifications have been completed, the part number for the assembly becomes PWBMESPPLL-E.
MFX 146.1	ESP-PLL		**2.9**	**2.1**	17-Sep-97	Phased Lock Loop Card	ERIK DE CASTRO LOPO		Increase output level of WCLK OUT signal to 4V p-p when terminated.	Remove 75R modification resistor across C2 (10pf). Change U15 from 74ACT244 to 74F244(or 74FCT244).
MFX 147.1	ESP-PLL-E		**2.9**	**2.1**	05-Dec-97	Phased Lock Loop Card EMC Version	Chris Alfred		Increase output level of WCLK OUT signal to 4V p-p when terminated.	Remove 75R modification resistor across C2 (10pf). Change U15 from 74ACT244 to 74F244(or 74FCT244).
MFX 209.1	ESP-PLL, ESP-PLL-E				11-Jun-97	Phase Lock Loop Card (including EMC Version)	NOEL PLUMMER		The 2 x 9 pin header, JP5 was included on the PLL card for initial development work and is no longer required.	Delete 2 x 9 pin header CONG5233-9 at location JP5, for new build.
MFX 245	ESP-PLL, ESP-PLL-E	ESP-PLL-C	**2.1**	**3**	08-Apr-98	Phased Lock Loop Card EMC Version	Noel Plummer		The ESP-PLL PCB has been redesigned. The new PCB is revision 3. Rev 3 PCB incorporates all mods up to 2.10 therefore assembly revision 3.0 is equivalent to assembly revision 2.10. Rev 3 PCB uses variable oscillators modules, inplace of the previous discrete sample rate clock circuitry. This, plus some other changes has resulted in a component count reduction of over 50 pieces compared with the rev 2 PCB. The new PCB also eliminates the need for the two version of the assembled card, the non-EMC (ESP-PLL) and EMC (ESP-PLL-E) versions.	New Revision ESP-PLL Blank PCB - Rev 3 Part Number 1MFXPWBPLLC replaces 1MFXPWBPLLE and 1MFXPWBPLLZ Part Number MANMESPPLLC replaces MANMESPPLLE and MANMESPPLL Part Number EXCPLLC replaces EXCPLLE and EXCPLL Part Number REPPLLC replaces REPPLLE and REPPLL Part Number WARPLLC replaces WARPLLE and WARPLL Part Number FAULTYPLLC replaces FAULTYPLLE and FAULTYPLL
MFX 247.1	ESP-PLL-C	ESP-PLL-C	**3.1**	**3**	27-Aug-98	Phased Lock Loop Card EMC Version	George Potkonyak	Features introduced by ECN 247 are no longer required.	PLX card deleted.	Cutting of tracks not required. Installation of header at JP4 not required Installation of jumpers between pins 7 and 10 and pins 8 and 0 of JP4 not required Note 1: 150 pF capacitors at C77 and C79 still required Note 2: Field units already modified as per ECN 247 DO NOT have to be reverted to Rev.3.0 Note 3: Units in WIP already modified as per ECN 247 DO NOT have to be reverted to Rev. 3.0
MFX 259	ESP-PLL-C		**3.0** **3.1**	**3.2** **3.2**	27-Aug-98		George Potkonyak		Possibility of tracks under the aluminium block being shorted.	Install an insulation pad, TO-220, Failight Part No. WASH0023, under the aluminium support block near U3. Note to Service: Modify all stock and all units containing Rev. 3.0 or Rev. 3.1 PLL-C cards, when they are being serviced. Relabel cards to Rev. 3.2 Note to Production: Modify all stock and relabel cards to Rev. 3.2 Note to Subcontractors: Modify all stock and relabel cards to Rev. 3.2
MFX 279.1	ESP-PLL-C	ESP-PLL-C	**3.2**	**3.3**	23-Feb-99	Phased Lock Loop Card EMC Version	George Potkonyak	This ECN replaces ECN 279 (a modification added).	The 9 pin D connectors on this card have too much reach causing the support panel to bend. PCB Rev. 3A manufactured for the introduction of the PLX card which has been abandoned.	1. Change the Male D Connector at P1 and P2 to Fairlight P/N: COND6047/M Desc: DB9M 0.318" (8.1mm) footprint, Male PCB R/A, Solder locating lugs, Select Gold => 15u". Manufacturer: U.L. Recognised, non-critical 2. Fit 2 Shorting Jumpers at JP4 location: one between Pins 7 and 10 and one between Pins 8 and 9 on all Rev. 3A blank PCB-s 3. Re-label assembly as Revision 3.3. Note to Subcontractors: Modification # 2 above required only till stock of Rev. 3A PCB-s used. Rev. 3 PCB-s do not need this modification. Note to Production: Modify all Cards in WIP. Note to Field Service: No action required. All cards leaving the factory have been modifiied.

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ECNs for PSA Card as at 11/6/99

ECN Number	Assembly	New Assembly	Current Rev	New Rev	Date	Description	Name	Special Note	Reason	Details
MFX 168	ASYM7001, CSLMFXPSA		**N/A**		10-Dec-96	MFX Plus Console FAME & Standalone	Leith Stewart		MFK board interferes with LCD Data Cables.	1. Remove 7 x 2 header (CONG5233-7) from LCD Data Outputs. 2. Fit new 7 x 2 Right Angle Header (CONG5246-7) to the LCD Data Outputs.
MFX 171	CSLMFXPSA ASYM7001				11-Dec-96	MFX3 Plus Console FAME Console	Leith Stewart		Wire gauge too heavy on the cables that solder to boards.	1. New specifications for the following cables have been released; CABM6258 - CABLE MFK DISPLAY PNL POWER,UL Rev 1.1 CABM6259 - CABLE 010-MFK, TRIM POTS, UL Rev 1.1 CABM6260 - CABLE MFX010, SPEAKER, UL Rev 1.1 2. All further purchases of these items must be to the new specification. 3. Use all old stock from wharehouse before implementing the new specification cables.
MFX 193	1MFXCSLPSAU, 1MFXCSLPSAE	1MFXCSLPSAN			20-Mar-97	MFX PLUS CONSOLE STAND ALONE	RAJEEV GANESH		MFX PLUS Stand alone Console has acquired UL Listing and EMC compliant status.	P/N 1MFXCSLPSAU and 1MFXCSLPSAE are not to be used any more. P/N 1MFXCSLPSAN to be UL and CE labelled. CMS BOM amended to include LABAMP3819S (Qty 2), LAB1005, and Gaskets GSKTD0910, GSKTD3720.
MFX 229	1MFXCSLPSAN, 1MFXCSLPO2N, 1MFXCSLP19N				16-Oct-97	CONSOLE MFX+ S/A , O2R, 19"	Noel Plummer		A number of MFX+ consoles have recently been shipped with a non-locking type DIN connector on the external power supplies. This connector has been found to cause problems if the console is moved while powered and in particular the console's config info, stored in the NVRAM, is corrupted.	Replace the DIN connector with a locking type (Fairlight P/N COND6784, Preh P/N 71430-070, Farnell P/N 437-220) as per attached drawing PSU2001.DW2 rev 1.7.
MFX 234	CSLMFXPSA		**1.5**	**1.6**	24-Nov-97	MFX Plus Stand Alone Console	Mario Paolino		Introduction of MFX-010 Rev 7 PCB see ECN 233	1. Delete CABM6259 2. Add CABM6259C 3. Change assembly revision to 1.6
MFX 241	1MFXPCLSPSAN			**NO CHANGE**	04-Mar-98	MFX+ STAND-ALONE CONSOLE	George Potkonyak		Two of two screws used, 12 mm long, are too short and may cause the stripping of the threads in the threaded inserts.	Replace two screws M4 x 12 mm, posi, Ni plated, part number SCRH1063, with M4 x 16 mm screws, posi, Ni plated, part number FSE0356. 12 mm length of the centre screw is sufficient and remains at the same, 12 mm long. The two screws are used for the fitting of the trim panel to the underside of wrist rest (one at each end). Documents affected: Bill of Material CSLMFXPSA revision raised from 1.5 to 1.6
MFX 261	CSLMFXPSA		**2**	**2.1**	31-Aug-98	MFX Plus stand alone console	Mario Paolino	Production Only Field Action: None WIP Action: None	The cable providing power to the LCD backlight, loops from one LCD to the next. The centre connector has 2 wires crimped onto the one pin which makes the join unreliable.	Delete: 1 x CABM6258 MFX010 to MFK LCD power Add: 2 x CABM6261 MFX010 to MFK LCD power Change Assembly revision as detailed above.

ECNs for RGB01 Card as at 11/6/99

ECN Number	Assembly	New Assembly	Current Rev	New Rev	Date	Description	Name	Special Note	Reason	Details
MFX 172	CAB5068				11-Dec-96	Cable Assy 14R CG4 - RGB01	Leith Stewart		There is not enough excess length to allow easy assembly.	1. New specifications for the following cable have been released; CAB5068 - CABLE ASSY 14R CG4 - RGB01 Rev 1.1 2. All further purchases of this item must be to the new specification. 3. Use all old stock from wharehouse before implementing the new specification cable.

ECNs for RIO Card as at 11/6/99

ECN Number	Assembly	New Assembly	Current Rev	New Rev	Date	Description	Name	Special Note	Reason	Details
MFX 216	ESP-RIO		**2**	**2.1**	28-Jul-97	Rear Input Output Card	ERIK DE CASTRO LOPO		Change required to make ESP-RIO compatible with current Software.	1. Remove Resistor network RN3. 2. Remove Resistor network RN4. 3. Label PCB Assembly as Rev. 2.1
MFX 219	ESP-RIO		**2.1**	**2.2**	03-Sep-97	REAR INPUT OUTPUT CARD	ERIK DE CASTRO LOPO		Some Monitors e.g. NEC 3FG do not SYNC correctly when connected to ESP-RIO.	1. Connect a solid core, single strand, modification wire from pin 4 of connector J2 to pin 5 of connector J2. This connects pin 5 of the VGA connector to ground. 2. Relabel PCB Assembly as 2.2.
MFX 222	ESP-RIO		**2.2**	**2.3**	05-Sep-97	REAR INPUT OUTPUT CARD	ERIK DE CASTRO LOPO		Reduce the coupling of SCSI noise onto the RGB output signal.	1. Connect a wire of following specifications: 1/0.6mm (0.28 square mm cross-sectional area) Voltage : 300V Current : 7 Amp @ 70 degrees Celsius. Insulation : Green. between the shell of J2 (RGB Output Connector) to the negative terminal of C6 on the solder side. 2. Relabel the PCB Rev. 2.3.
MFX 273.1	ESP-RIO		**2.3**	**3**	18-Nov-98	REAR INPUT OUTPUT CARD	Noel Plummer		The ESP-RIO PCB has been redesigned. The new PCB is revision 3. It is functionally equivalent to assembly revision 2.3. On the new PCB the following has been done to reduce noise emmission affecting the nearby first AIO card. The ground planes has been moved from the top to bottom layers . Series resistors have been added to the base circuit of the four video sync driver transistors. The three box headers are now in-line, to facilitate easier cable connection inside the machine. Some redundant parts have been removed and the diode networks changed to discrete devices.	New Revision ESP-RIO Blank PCB - Rev 3 Fairlight P/N PWAEESPRIOR3 The new PCB features the following changes and enhancements: Moved ground planes to bottom layer. Added series resistors (RN3) to base of Q1, Q2, Q6 and Q7. Moved JP2, JP3 and JP4 to be inline. Deleted U3 and RN4. Changed diode networks to discrete diodes. Connected COMMSGND to shield. Connected HSSLGND to shield. Prelinked JP1. Connected FGND to GND. Changes: 273.1 Changed current revision from 2.2 to 2.3

ECNs for SYN Card as at 11/6/99

ECN Number	Assembly	New Assembly	Current Rev	New Rev	Date	Description	Name	Special Note	Reason	Details
MFX 4	ESP-SYN		**2**	**2.1**	29-Jun-94	Sync Card	Chris Alfred		Additional design features.	TSBEN driven by tri-state buffer Change U11 to 74F125 Connect U11/1 to U11/12 Connect U11/2 to U11/11 Connect U11/13 to U29/69 (XC3042) Connect R1 pin nearest U11/1 to RN2/10 and RN5/10. Additional synchronisation signals Connect U29/70 (XC3042) to JP1/45 Connect U29/67 to JP1/46 Connect U29/65 to JP1/42. *FIFO signal ringing. Connect 56R between U69/22 (IODEC) and U69/14 Leave IODEC pin 22 out of socket. U1 LED array error Align U1 pin 2 with pin 1 on PCB U1 Connect U1/1,3,5,7 to PCB U1 pin 8. Disable IACK Connect U28/41 to U32/20. Overlay error All 74HC646 should be 74AC646 U74 is 74LS122. Component change Change C1 to 10uF tantalum 16v Remove R16 Remove C22
MFX 5	ESP-MIDI		**2**	**2.1**	28-Apr-94	SYNC IO Support and MIDI	Chris Alfred		Additional synchronisation features.	MCLKIN from AES reference. Connect U23/19 (CS8411) to JP5/45. VSYNC reference Connect U5/3 (LM1881) to JP5/46 and U16/3 (74HC251). RTS/CTS for RS232 Cut component side track to U33/9 (74HC4053) Connect U33/9 to RN3/3 Cut solder side track to U18/8 (68681FN) Cut solder side track to U18/5 Connect U18/43 to U14/6 (TR1) Connect U18/42 to U20/6 (TR1) Connect U18/5 to JP2/18 Connect RN3/2 to JP2/17. V+/V1 to JP2 Connect JP2/19 to JP6/3 Connect JP2/20 to JP6/4 . Timecode readers Cut component side track to U13/5 Cut solder side track to U13/6 Cut solder side track to U12/5 Cut solder side track to U12/6 Connect U12/5 to U13/5 and JP2/14 Connect U12/6 to JP6/10 Connect U13/6 to JP6/8 Cut component side track to U20/27 Cut solder side track to plate-thru near U14/2 Connect U17/13 to U12/11 and U13/11 Connect U12/10 to U12/16 Connect U13/10 to U13/16 Connect U12/9 to U20/27 Connect U13/9 to U14/27
MFX 16	ESP-MIDI		**2.1**	**2.2**	29-Jun-94	Sync IO support and MIDI	Chris Alfred		Shift signals to allow for full RS232 implementation on ESP-IO in fututre. Once these changes have been made, SC Disagnosticssx must be Rev 1.3 or higher.	Cut solder side track to U18/40 (68681) Cut solder side track to U18/3 Cut component side track to U33/11 (74HC4053) Connect U14/5 (TR1) to U11/8 (68681) Connect U20/5 (TR1) to U11/5 Connect U33/11 to U11/30
MFX 17	ESP-SYN		**2.1**	**2.2**	12-Jul-94	Sync Card	Chris Alfred		More accurate internal sample rates.	Change crystals Y2 (8M192), Y3 (11M2783), Y4 (11M2896) and Y5 (12M288) to 50ppm accuracy. This requires modification to the bill of materials.
MFX 19	ESP-SYN		**2.2**	**2.3**	15-Jul-94	Sync Card	Chris Alfred		New Sync Card software. Required for software revisions 12.0.08 and higher. Must be done in conjunction with Change Note 18.	Change 27C512 eprom at U34 to KMON30 V9.05.

ECNs for SYN Card as at 11/6/99

ECN Number	Assembly	New Assembly	Current Rev	New Rev	Date	Description	Name	Special Note	Reason	Details
MFX 22	ESP-SYN		**2.3**	**2.4**	20-Jul-94	Sync Card	Chris Alfred		Better damping of PCLK signal. Noise on WREF signal causing shared memory errors when accessed by Waveform Supervisor. Inproved control range of VCO. This Change Note implies changes to the Bill og Materials changes marked by (*).	Change RN21 to 10R 8 pin resistor pack WREF noise Cut solder side track to edge connector pin 67A. Lift pin 1 of U40 (74AC04). Connect U40/1 to edge connector pin 67A. Change U47 to SHARE7 pal. VCO range Remove U70 (TL082 or equiv) and insert socket. Place U70 into socket leaving pins 2,3,5,6 lifted. Change R24 to 120R. Change R26 to 180R. Connect U70/2 to U71/2 (AD569). Connect U70/3 to R24 pin nearest pin 1 of U70. Connect U70/5 to R26 pin nearest pin 1 of U71. Connect U70/6 to U71/16.
MFX 29	ESP-SYN		**2.4**	**2.5**	15-Aug-94	Sync Card	Chris Alfred		Differentially buffer AES input sync. To be done in conjunction with Change Note 30.	Disconnect modification connecting U29/70 (XC3042) to JP1/45. Connect JP1/40 to U12/10 (3486). Connect JP1/38 to U12/9 (3486). Connect U12/11 to U29/70.
MFX 37	ESP-SYN		**2.5**	**2.6**	19-Oct-94	Sync Card	Chris Alfred		Modifications for installation of ESP-PLL card.	Remove modification joining U29/65 (XC3042) to JP1/42. Remove modification joining U29/67 to JP1/46. Remove modification joining U29/70 to U12/11 (3486). Cut component side track to U17/1 (3487). Cut component side track to U17/7. Lift U15 (3486) pins 9 and 10. Connect 100R across U15/9 and U15/10. Connect 100R across U12/9 and U12/10. connect JP1/42 to U15/9. Connect JP1/46 to U15/10. Connect U12/11 to U17/1. Connect U15/11 to U17/7. Connect JP1/45 to U29/70. Mark PCB as rev 2.6.
MFX 40.1	CABM7327				21-Nov-94	ESP-SYN to ESP-MIDI 60 way cable	Chris Alfred		ESP-MIDI Rev 4 PCB and above has JP5 (60way half pitch connector) re-configured. This requires that the two 30 way cables should not have a cross-over twist. ESP-MIDI revisions below 4.0 MUST use existing twisted cables Part No. CABM7328.	Cable to be manufactured without the two 30 way cables having a cross-over twist. Parts requied are; a. Connector part no. COND6102, Quantity X2 b. 34 Way flat cable part no. CABG6021 to be modified to 30 way. Length to be determined as per machine configuration.
MFX 46.1	ESP-SYN		**2.6**	**2.7**	01-Nov-94	Sync Card	Chris Alfred		Add DTACK to duart. Add A12,A13 to XILINX to allow addressable wait states to Sync IO.	Connect U28/10 (68681) to U41/3 (DSACK 22V10-15). Connect U29/67 (XC3042) to U26/8 (74ACT244). Connect U29/65 to U26/6.
MFX 87	ESP-SYN		**2.7**	**2.8**	04-Apr-95	SYNC CARD	Chris Alfred		Components no longer used to be deleted to reduce assembly costs.	Delete Crystals Y3, Y4, Y2; IC Socket SU71; cap C23; resistors R23, R24, R25, R26; ICs U70, U71, U86, U35. (Please see details as per attached sheet). This change applies to manufacturing only.
MFX 110	ESP-SYN		**3**	**3**	25-Aug-95	SYNC CARD	Noel Plummer	Applies to manufacturing only. No changes to MFX3 hardware or software required.	Components no longer used to be omitted from new revision card to reduce assembly costs.	1. Delete Crystal Oscillator X1, IC Socket at U33. 2. Omit caps C5, C6, C7, C8, C9, C10, and resistors R4, R5, R6, R7, R8, R9, and IC U35
MFX 111.1	ESP-SYN		**2.8 3.0**	**2.9 3.1**	13-Mar-96	Sync Card	Chris Alfred	Implementation of this ECN is mandatory on all machines.	Communication errors to the DIO would cause the sytem to exit to the shell with 'Error #003 Interrupt key pressed' message. The communcation errors are due to a timing error when accessing the DUART (68681 U28) on the ESP-SYN card. The error reports DIO status "J" timeout on TVTs on R&D machines.	Rev 2.0 PCB 1. Change DSACK pal at U41 to DSACK3. The pal MUST be Lattice 22V10-15LP. 2. Change IODEC pal at U69 to IODEC5. MUST be Lattice 22V10-15LP. Leave pin 22 of the pal OUT OF the socket. 3. Disconnect mod wire, added on ECN 46A, between U28/10 (68681) & U41/3 [DSACK]. 4. Connect U28/10 to RN14/5 (4k7 10 pin resistor pack) and to U41/7. 5. Update revision of card. . Rev 3.0 PCB 1. Change DSACK pal at U41 to DSACK3. The pal MUST be Lattice 22V10-15LP. 2. Change IODEC pal at U69 to IODEC5. MUST be Lattice 22V10-15LP. Leave pin 22 of the pal IN the socket. 3. Cut track, on component side, which exits between pins 8 & 9 of U32 (74HCT245). 4. Connect U28/10 to RN14/5 (4k7 10 pin resistor pack) and to U41/7. 5. Update revision of card.
MFX 114	ESP-SYN		**2.9**	**2.1**	07-Nov-95	Sync Card	Chris Alfred	Must be done in conjunction with ECN113.	Stop system hanging at 'speckled coloured screen' on power on.	1. Remove C24 (4.7uF).

ECN Number	Assembly	New Assembly	Current Rev	New Rev	Date	Description	Name	Special Note	Reason	Details
MFX 124.1	ASYMFX3SYNX 1	ASYMFX3SYNX 1E	**N/A**	**N/A**	20-Feb-96	SYNC I/O MODULE - EMC COMPLIANT	Leith Stewart	Applicable to all machines with an EMC compliance requirement. To be used in conjunction with ECN # 123.	To modify the current Sync module to meet EMC requirements.	1. Modifications to the Sync I/O module are required for EMC compliance. They are listed below by subassembly. 2. PWBMESPLTC Replace all XLR connectors with nickel plated connectors (F/Light # COND0119 female & COND0120 male). Viewing the board with P1 on the left, component side up, attach flying leads (24AWG wire) from connectors to PCB in the following manner. A: For connectors P1, P2 & P4, attach pin1 of connector to left hand hole, pin2 of connector to right hand hole & pin3 to middle hole. Earth shell of connector to pin1. B: For connectors P3 & P5, attach pin1 of connector to right hand hole, pin2 of connector to left hand hole, & pin3 to middle hole. Earth shell of connector to pin 1. 3.A PWBMESPMIDI Replace BNC connector J1 with metal shell connector (F/Light # COND6998). Ensure that the star washer is placed and that the nut is well tightened to the support panel to ensure good electrical contact. 3.B PWBMESPMIDI Replace all 5 pin DIN connectors (P1 to P4) with metal shell DIN connectors (F/Light # COND6786). Viewing board with P1 on the left, component side up, attach flying leads (24AWG wire) for each connector in the following manner. Attach pin4 of connector to bottom right hole, and attach pin5 of connector to bottom left hole. For each connector, all three holes on the PCB above the two connected holes should be left unattached. Do not earth shell of connector. Ensure pins 1, 2 & 3 of connector are not in contact with anything. Cut off excess tabs if necessary. 4.A PWBMESPPLL Replace all BNC connectors with nickel plated ones (F/Light # COND6998) in the same manner as used on the MIDI card. 4.B PWBMESPPLL Viewing the board solder side up, P1 on the left, solder the right shell mounting guide of P1 to the left shell mounting guide of P2 together using 24AWG wire. Solder another similar wire to the left hand shell mounting guide of P1 and screw the other end to the support block screw (a crimp terminator may be used). Place RFI gaskets (F/Light #GSKTD0910) between each 9 pin D connector and the support panel. . . . 5.A PWBMESP9PIN Place RFI gasket (F/Light # GSKTD0910) between each male D connector (P3 & P5) and support panel. Place RFI gasket (F/Light # GSKTD0920) between each female D connector (P1, P2, P4) and support panel. 5.B PWBMESP9PIN Viewing the board from the solder side with P3 on the left, solder a wire (24AWG) from the right hand mounting guide of P3 to the left hand mounting guide of P5. Repeat this for P5 to P4, P4 to P2, P2 to P1. Solder a wire (24AWG) to the right hand mounting guide of P1 and screw the other end to the support block screw (a crimp connector may be used). 6. SYNC MODULE Place RFI gasket (F/Light #GSKT1001-03) either side of the MFX console connector between the connector and the support panel ensuring there is good electrical connection. Place RFI gasket (F/Light #GSKT1000-05) at the top and bottom of the rear of the support panel, centralised between the mounting screws. This gasket is to ensure there is good electrical connection between the support panel and the chassis. 7. When all modifications are complete, the part number for the assembly becomes ASYMFX3SYNX1E.
MFX 134.2	ESP-SYN		**3.1**	**3.2**	30-Jun-98	Sync Card	Noel Plummer		On rev 3 PCB termination resistors were added on signals SIOSYNC+/-, LTCOUTCLK+/-, *ZTPIN+/-, M256+/-, MWORD+/- & RXD+/- Termination of RXD+/- created a problem with communications to the DIO card. Until further investigated these six new resistors are to be removed.	1. Remove resistor networks RN1 and RN3. 2. On the component side install a 100R 1/4 watt resistor beween pins 7 & 8 of RN1. Install the resistor so that it is horizontal to the PCB as there is a height problem if it is stood up on end. 3. On the component side install a 100R 1/4 watt resistor beween pins 7 & 8 of RN3. Install the resistor so that it is horizontal to the PCB as there is a height problem if it is stood up on end. Changes: 134.1 Resistors moved to component side. 134.2 Resistors installed horizontally on component side.
MFX 183	ESP-SYN		**2.10, 3.2**	**2.11, 3.3**	17-Feb-97	SYNC CARD	CHRIS ALFRED		The GAL16V8C-7LP output signals are too low. This usually results in the ESP-SYN card not being detected. GAL16V8C-7LP must not be used in the ESP-SYN.	1. U45 (CLKGEN2) is to only be GAL16V8B-7LP (PROB1096/7) or GAL16V8B-15LP (PROB1096/15).
MFX 184.1	ESP-SYN		**2.11, 3.3**	**2.11, 3.3**	16-Mar-98	SYNC CARD	CHRIS ALFRED	Correction of PLL lock explanation	Procedure for checking lock status of ESP-SYN PLL. If the PLL is not locked, then the ESP-SYN card will not be detected on startup.	When the bottom LED on the ESP-SYN card is dimly lit the PLL is in Lock 1. If the bottom LED is ON (indicates unlocked), adjust trimmer capacitor C15 until the bottom LED is dimly lit. 2. If the bottom LED is OFF (indicates unlocked), adjust trimmer capacitor C15 until the bottom LED is dimly lit. 3. Restart the system.
MFX 228.2	ESP-MIDIE		**N/C**	**N/C**	17-Mar-98	Midi and Sync Control card	Mario Paolino	Correction to Revision Number This ECN applies to Board Assembler	Installation of DIN connectors Correction of ECN 228	1. ADD: 4 x Socket COND6787 DIN 5P 45 FE15 2. Solder the flying leads to the DIN connectors as per the following diagram. 3. No Change to the Revision Number

Compliled by Noel Plummer

ECNs for SYN Card as at 11/6/99

ECN Number	Assembly	New Assembly	Current Rev	New Rev	Date	Description	Name	Special Note	Reason	Details
MFX 240	ESP-SYN				09-Nov-95	Sync Card	Erik de Castro Lopo	This is a Special ECN to enable connection to a 10Mb Ethernet network. Not for Production.	Enable 10 Mb Ethernet Functions on Sync Card	1. Place 16 pin DIL socket at U16. 2. Connect a 270R resistor from U16/7 to ground at the end of R30 nearest the motherboard edge connector. 3. Connect a 270R resistor from U16/8 to ground at the end of R30 nearest the motherboard edge connector. 4. Connect a 75R resistor from U16/1 to U16/2. 5. Connect a 75R resistor from U16/4 to U16/5. 6. Connect a wire (suggest 0.6mm/0.025" solid core) from U15/8 (ground) to U16/3. 7. Connect a wire (as above) from U24/20 (+5V) to U16/6. 8. Insert a DP83932 Sonic Ethernet chip at U33. 9. Connect the Ethernet jumper board to U16 using the header cable supplied, ensuring pin 1 of both header plugs are matched to pin 1 of their respective sockets.
MFX 243.1	ESP-SYN		**2.12** **3.4**	**2.11** **3.3**	16-Apr-98	SYNC card	chris Alfred	ECN 243 RETRACTED	ECN 243 RETRACTED	1. The Revision Number of the card reverts back to 2.11 3.3
MFX 244.1	ESP-SYN		**2.11** **3.3**	**2.11 A** **3.3A**	16-Apr-98	SYNC card	chris Alfred	Correction of Revision Number	Audio corruption on input when armed NOTE: 1. This should not be done in production. 2. Only to be done on machines which exhibit the corruption.	For Rev 2.11 cards: 1. Change 100R resistor across JP1 pins 42 and 46 to 220R 2. Change card revision as detailed above . . For Rev 3.3 cards: 1. Change 100R resistor across RN1 pins 7 and 8 to 220R 2. Change card revision as detailed above Changes : ECN 244.1 Correction of Assembly Revision Number
MFX 249.1	ESP-MIDI & ESP-MIDI-E	ESP-MIDI-C	**4.8x**	**5.0x**	20-Jul-98	Midi and Sync Control card	Noel Plummer		The ESP-MIDI PCB has been redesigned. The new PCB is revision 5. Rev 5 PCB incorporates all mods up to 4.8 therefore assembly revision 5.0 is equivalent to assembly revision 4.8. The new PCB also eliminates the need for the two version of the assembled card, the non-EMC (ESP-MIDI) and EMC (ESP-MID-E) versions. The new PCB also features the following enhancements: Allows installation of Preh locking DIN EMC type connectors. Rear panel connectors to connected to chassis ground. JP3 moved alongside JP7 to eliminate need for short cable on JP3. Pad to track clearance increased for improved reliability. Jumpers eliminated by pre-linking JP1 and JP9 on PCB. Teardropping added to all pads for improved PCB reliability.	New Revision ESP-MIDI Blank PCB - Rev 5 P/N PWAEESPMIDIR5 Part Number 1MFXPWBMIDC replaces 1MFXPWBMIDE and 1MFXPWBMIDZ Part Number MANMESPMIDC replaces MANMESPMIDIE and MANMESPMIDI Other new part numbers with related P/Ns shown in brackets: EXCMIDC (EXCMIDE and EXCMIDI) FAULTYMIDC (FAULTYMIDE and FAULTYMIDI) REPMIDC (REPMIDE and REPMIDI) WARMIDC (WARMIDE and WARMIDI) The 4 jumpers (P/N COND6747) and the 4 x 2 Header (P/N CONG5233-4) have been eliminated by pre-linking on the PCB. The re-positioning of JP3 has eliminated the need to plug the short extender cable (P/N CABM7334) into JP3, before assembling the SYNC-IO module. Changes: 249.1 Deleted line 4 of Details of Change, corrected part numbers in first three lines of Details of Change.
MFX 266	ESP-MIDI-C		**5.0x**	**6.0x**	28-Sep-98	Midi and Sync Control card	Noel Plummer		The ESP-MIDI blank PCB has been updated again to correct JP3 layout error in rev. 5. The new PCB is revision 6 which is electrical equivalent to rev. 5 PCB. Rev. 6 allows a box header to once again be used at JP3. JP8 has been moved slightly to the left, to improve alignment with the cable which comes from the LTC card. The position of mounting holes for the aluminium support blocks has been corrected. They have been moved 0.025" closer to the front panel board edge.	New Revision ESP-MIDI Blank PCB - Rev 6 P/N PWAEESPMIDIR6

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ECNs for SYN Card as at 11/6/99

ECN Number	Assembly	New Assembly	Current Rev	New Rev	Date	Description	Name	Special Note	Reason	Details
MFX 276.1	ESP-SYN		**3.3**	**4**	20-Jan-99	Sync Card	Noel Plummer		The ESP-SYN PCB has been redesigned. The new PCB is revision 4. It incorporates all mods up to 3.3, therefore assembly revision 4.0 is equivalent to assembly revision 3.3. On the rev 3 cards, the variable cap at 6.8 to 45pF, was often difficult to adjust. By using precision frequency setting components in the VCO circuitry, the value of the variable cap C15 can be substantially reduced, therefore increasing the useful adjustment range. Note that the PLL lock LED will only light now on power up OR if the PLL circuitry develops a problem. Provision has been made, on this new layout, to use 1% silver mica caps and a 11 turn tuneable inductor, if necessary. A cut-out of almost 3" has been inserted in the main edge connector. This will reduce insertion and extraction force of the PCB, into the Digital Mother Board, by about 36%.	New Revision ESP-SYN Blank PCB - Rev 4 Fairlight P/N PWAEESPSYNR4 The new PCB features the following enhancements: Removed unused components: U33,X1,U16,R4-R9,C5,C6,U35,C7-C10,JP2,JP3,JP4. Replaced: RN1 with R31, RN3 with R33, Added R32, R34, JP6, JP7 to implement ECN 244 by moving jumpers to pins 2-3. JP2 and JP3 deleted and replaced with direct connections. Modified boundary keep out to match routing drawing. Increased pad to track clearance on solder side to improve reliability. Fairlight logo on silk-screen All pads and vias teardropped for improved reliability. PCB text positioned to avoid perforation by vias. Change history to this ECN: 276.1 Expanded paragraph 2 of change reasons, corrected removed components in Details Of Change: U3 changed to U33, duplicate X1 removed, added JP2 and JP3.

ECN Number	Assembly	New Assembly	Current Rev	New Rev	Date	Description	Name	Special Note	Reason	Details
MFX 2.1	ESP-TS		**3.1**	**3.2**	17-Mar-98	Turbo SCSI	Mario Paolino	Revision Number Correction Rev 3.0 to 3.1 Ref FCN 138 5/1/94	Invert WBINT signal to active low for reliabiliy. This change must be done in conjunction with change note 1 to the Waveform Supervisor card. MFX2 and lower software will operate with these changes performed. If one change note is not performed without the other, then the system will not boot.	Change U43 to TSEXT3. Change U48 to TSCSI4. Change U40 to TSWFM15. Ensure Change note 1 has been done on Waveform Supervisor. Update revision of card.
MFX 15.3	ESP-TS		**3.2**	**3.2N, 3.2T**	17-Mar-98	Turbo SCSI card	Mario Paolino		Termination required on systems with one external SCSI connector.	For systems with ONE external SCSI connector. (e.g. MFX3 Mini & MFX3 Rack), install 220/330R 8Pin resistor packs at RN7, RN8, RN9. Add T (for terminated) suffix to revision number. For systems with TWO external SCSI connectors. (e.g. upgraded MFX2 systems), remove termination resistor packs at RN7, RN8, RN9. Add N (for Non-terminated) suffix to revision number
MFX 25.1	ESP-TS		**1.4**	**1.5**	01-Aug-94	Turbo SCSI	Chris Alfred	For old Rev 1 PCBs only (For Rev 3 PCBs, see ECN 2). This replaces ECN 25 (Revision numbers were incorrect)	Invert WBINT signal to active low for reliabiliy. This change must be done in conjunction with Waveform Supervisor change note 1 (for Rev 2 PCBs) or change note 24 (for Rev 1 PCBs). MFX2 and lower software will operate with these changes performed. If one change note is not performed without the other, then the systems will not boot. This change note is the Rev 1 PCB equivalent of Change Note 2.	Change U43 to TSEXT3. Change U48 to TSCSI4. Change U40 to TSWFM15. Ensure Change note 1 or 24 has been done on Waveform Supervisor. Update revision of card.
MFX 56.1	ESP-TS		**1.5**	**1.5N, 1.5T**	17-Mar-98	Turbo SCSI card	Mario Paolino	Correction to Revision Number	Termination required on systems with one external SCSI connector.	For systems with ONE external SCSI connector. (e.g. MFX3 Mini & MFX3 Rack) 1. Install 220R/330R 8 pin resistor packs at RN7,RN8,RN9. 2. Add T (for 'Terminated') suffix to revision number. For systems with TWO external SCSI connectors. (e.g. Upgraded MFX2 systems) 1. Remove termination resistor packs at RN7,RN8,RN9. 2. Add N (for 'Non-terminated') suffix to revision number.
MFX 88.3	ESP-TS		**1.4** **3.1**	**1.4C** **3.1C**	15-Apr-98	Turbo SCSI Card	Mario Paolino	MFX2 only Rev No incorrectly marked.	Stop CMI31 Channel Card audio corruption during disk reads in MFX2 systems. This change should only be done to MFX2 systems. The last revisions of the ESP-TS PCBs for MFX2 are 1.4C, 3.1C.	Change U40 to TSWFM16. Connect U28/10 (447-250-10) to U40/10. Change card revision as detailed above
MFX 108.1	TS1		**4**	**4**	10-Aug-95	Turbo SCSI	Noel Plummer	Change assembly name from TS1 to TSR and description from Turbo SCSI to Turbo SCSI (R). Replaces TS1 for new build MFX3. No changes to MFX3 hardware or software required. **(NB U14 changed to U12)**	Removal of the MFX2 Channel card support hardware from the TS1 card which is not required for MFX3.	1. Delete the following parts from new build Resistors: R4, R5, RN1, RN2, RN3, RN4. ICs: U1, U2, U8, U9, U10, U12, U13, U20, U23, U22, U23, U45, U55, U56. IC Sockets: U10, U20, U55. Other: C1, CN2, L1, Q1, Y1. 2. Relabel card as TSR.
MFX 157.6	ESP-TSR ESP-TS1		**4.0, 3.2N, 3.2T 1.5N, 1.5T**	**4.1, 3.3N, 3.3T 1.6N, 1.6T**	01-Dec-98	Turbo SCSI (R) and TS-1	Mario Paolino	Modification wire has been re-routed in point 4 of Details of Change. Correction of Revision Number	To enable ESP-TSR and ESP-TS1 to operate with ESP-WX for MFX3 plus.	Refer Drawing - ECN 157.5 attached. 1. Remove IC TSDRAM12 from U38. 2. Insert new GAL TSDRAM13 to U38. 3. Lift pin U48/1 (TSSCSI) out of socket. Connect the lifted pin 1 of U48 to U28/12 (447-250-10 delay line). 4. On component side, cut track going between pins 6 & 7 of U56 Ic 447-250. Connect a wire link between the PTH (isolated by the cut) to U46/4 (74ACT244). 5. Lift pin U35/7 (74HCT240). 6. Change card revision as detailed above Changes: ECN 157.6 Inclusion of reference to Rev 1.5 cards
MFX 250	TSR		**4.1**	**5**	17-Jul-98	Turbo SCSI	Noel Plummer		The ESP-TSR PCB has been redesigned. The new PCB is revision 5. Rev 5 PCB incorporates all mods up to 4.1 therefore assembly revision 5.0 is equivalent to assembly revision 4.1. The new PCB features the following enhancements: Incorporates mods in ECN 157.5 into PCB. Teardropping added to all pads for improved PCB reliability. Fairlight logo on silkscreen.	New Revision ESP-TSR Blank PCB - Rev 5 Fairlight P/N PWAEESPTSR5

ECNs for TS Card as at 11/6/99

ECN Number	Assembly	New Assembly	Current Rev	New Rev	Date	Description	Name	Special Note	Reason	Details
MFX 269.2	ESP-TSR		**4.1** **5.0**	**4.2** **5.1**	03-May-99	TSR CARD	Chris Alfred Mario Paolino	To achieve the higher transfer rates, the software installed MUST BE 14.2.25 or 15.1.05d or higher, and DIP switch 5 (disable synchronous SCSI) must be OFF. THIS ECN SUPERCEDES THE ECN # 269 AND IS VALID ONLY AFTER THE RELEASE OF 14.2.25 OR 15.1.05d SOFTWARE	To allow faster SCSI transfer speeds. Maximum SCSI data transfer rate is approx 10MB/sec.	1. Replace U47, 53C94 (Fairlight part # SIPB6511) with 53CF94-2 (Fairlight part # SIPB6512). 2. Replace X1, 20 MHz Crystal Osc Module (Fairlight part # CRYC9031), with a 40 MHz Crystal Osc Module, 14 Pin DIL, 4 Pin Package, CMOS Output, 5 ns Rise/Fall Output Time, Temperature stability +/- 100 ppm. (Fairlight part # CRYC9026) Note to Production: Modify all TSR Cards in WIP ONLY IF 14.2.25 OR 15.1.05d (or higher) software used. Re-label Rev. No as detailed above. Note to Field Service: This modification is MANDATORY if software 14.2.25 or 15.1.05d or higher installed. Re-label Rev. No as detailed above. For software revisions lower than the above specified, DO NOT modify the TSR card.
MFX 274.1	ESP-TSR				03-May-99	TSR CARD	Mario Paolino	CANCEL ECN 274	Incorporated into ECN 269.2	.

ECN Number	Assembly	New Assembly	Current Rev	New Rev	Date	Description	Name	Special Note	Reason	Details
MFX 161	ESP-WX		**2**	**2.1**	16-Oct-96	Waveform Executive	Chris Alfred	First production version of ESP-WX.	Design errors fixed. PCB overlay errors notes. C27 removed for easier SIMM insertion.	1. Connect CN1/B61 to JP5/A16 2. Connect RN22/10 (10k 10 pin resistor pack) to test point connected to U11/69. 3. Connect U41/10 to U41/15. 4. Connect U34/6 to U34/19. 5. Remove C27 (10uF tantalum). Extra Notes: 1.The overlay for U15,U19,U24,U27 should read 29F040-120. 2.The overlay for U11,U28 should read 2064-80 to allow 80MHz parts (100MHz parts may also be used). 3.The GALs are: U1 (WXDONG), U34(WXGLU1), U41(WXGLU2) 4.The Lattices are: wxcpuc12, wxdebg09, wxdram08
MFX 164	ESP-WX		**2.1**	**2.2**	11-Nov-96	Waveform Executive	Chris Alfred		New WXDEBG,WXMIXR lattice sources to enable interrupts to mixer interface.	1. New wx2.dld supplied on MASTER WX PROGRAMMING disk.
MFX 165	ESP-WX		**2.2**	**2.3**	11-Nov-96	Waveform Executive	Chris Alfred		Terminate PCLK to CPU.	1. Connect 180R across pins R9 and R10 of U29 (68040RC33). [It may be easier to use SMD resistor.] 2. Connect U29/R9 to RN19/4.
MFX 166.1	ESP-WX		**2.3**	**2.4**	27-Feb-98	Waveform Executive	Noel Plummer		ECN Withdrawn	ECN Withdrawn Changes: 166.1 ECN Withdrawn
MFX 173	ESP-WX		**2.4**	**3**	13-Dec-96	Waveform Executive	Noel Plummer		New Revision PCB.	Revision 3 of the Waveform Executive card has been manufactured. It is equivalent to ESP-WX Rev 2.4 and incorporates ECNs 161 and 165 which therefore no longer need to be implemented. Use Waveform Executive Excel BOM Rev 3.0 with this new card.
MFX 174.2	ESP-WX		**2.4, 3.0**	**2.5, 3.1**	27-Feb-98	Wavform Executive	Noel Plummer		66MHz Clock requires fast rise and fall times for 68040.	1. At position X3, 66.000MHz Oscillator Module Fairlight P/N CRYC9043 - CRYS OSC 66M000 Hz HCMOS COMPA was specified as an HCMOS Compatible module. 2. Change specification for X3 with the following; Fairlight P/N CRYC9044 - CRYS OSC 66.000MHZ HCMOS, 50% DUTY CYCLE Change : 174.1 Assembly Revision number changed to 3.1, Crystal description enhanced. 174.2 Added rev 2.x cards.
MFX 190.1	ESP-WX		**All**		27-Feb-98	Waveform Executive	CHRIS ALFRED		OMF Software option requires extra 16Mb of DRAM to be installed.	1. When OMF option is ordered, include a 16Mb SIMM (P/N SISA1001) for the ESP-WX. 2. Install the 16Mb SIMM into the SIMM socket at U4. Changes: 190.1 Changed Rev to all.
MFX 210.1	ESP-WX				17-Jun-97	Waveform Executive Card	NOEL PLUMMER		The Excel BOM up to revision 3.2 lists three alternatives (74ACT245, 74F245, 74FCT245) for the 14 74AC245 ICs. Some of these alternatives have not been entirely successful so for the time being all alternatives are being dropped. Therefore all 14 of these ICs MUST BE 74AC245.	PCB locations U16, U17, U20, U21, U30, U31, U32, U33, U35, U36, U37, U38, U39, U40 MUST be 74AC245 (Fairlight P/N SITSAC245). Changes 210.1: Removal of use of alternatives in 7 out of 14 locations.
MFX 232.1	ESP-WX		**2.5, 3.1**	**2.6, 3.2**	27-Feb-98	Waveform Executive	Noel Plummer		Wx and CG4 assembly need to be secured together to avoid disconnection during transit.	1. Use four (4) Hexagonal spacers M2.5 X 10mm P/N SPCM1019 and place them on the mounting holes of connectors at location JP5 and JP9 form the component side. 2. Mount the tested CG4 ensuring correct orientation. 3. Carefully place four (4) Nylon screws M2.5 X 10mm P/N SCRH1110 with Nylon washers P/N WASH0006 through the mounting holes in CG4 and tighten fully. 4. Turn the entire assembly over and mount four (4) more Nylon screws M2.5 X 10mm P/N SCRH1110 with Nylon washers P/N WASH0006 and tighten fully. Changes: 232.1 Added rev 2.x cards.
MFX 265.2	ESP-WX		**3.2**	**3.3**	22-Sep-98	Waveform Executive	Mario Paolino	This ECN is a clarification of the ECN #265.1 NOTE: Machines running on Rev. 14.2.25 Software WILL run with the 32M SIMMs installed, however, SIMMs will be recognised only as 16M.	32M of DRAM required for all machines using Rev 15 software. 16M SIMMs are becoming obsolete so it has been decided to install 32M SIMMs in all ESP-WX cards.	1) Remove all SIMMs installed in the SIMM sockets at U3,U4. 2) Insert a 32M SIMM (SISA1005 SIMM 32MB 72p DRAM 70nS non-edo,parity or no parity) at U3. 3) Ensure that the Lattices are loaded using download file rev 7 or higher. (WX*.dld, WXCG*.dld, WXCGPC*.dld where * is 7 or higher). Additional notes: 1) If ESP-WX is to be used with an ESP-PCI card, the ESP-WXT terminator card should be installed at U4. NOTE TO PRODUCTION: If Rev. 14.2.25 Software is used it is OK to install 32M SIMMs even though they will be recognised as 16M only. Such machines will be ready to be upgraded to Rev. 15 S/W when available.
MFX 284.1	ESP-WX		**3.3** **2.6**	**3.4** **2.7**	09-Mar-99	CPU Card	Leith Stewart	This ECN replaces ECN # 284, in order to include Rev. 2 card modifications.	Micro-monitor ICs (1232 series) may not operate correctly.	1. Add mod wire from U10/7 to U9/3. 2. Cut track between U10/7 and via on top layer (component side) of board. 4. ICs approved for operation in this function are; DS1232, DS1232L, ADM1232AN. All other 1232 ICs should work, but are subject to Concession Request and subsequent approval. Note to Production: Modify all existing WIP to Rev. 3.3 and all Rev. 2.6 repair cards to Rev. 2.7 Note to Subcontractors: Modify all existing stock of Rev. 3 PCB-s, as per modifications 1 and 2 above. Note to Field Service: Modify WX cards on the machines when being serviced. All modified cards to be re-labeled for the correct revision number.